A 4-KB 667-MHZ CMOS SRAM USING DYNAMIC THRESHOLD VOLTAGE WORDLINE TRANSISTORS[§]

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ABSTRACT

The design of a prototypical 667-MHz CMOS 6-T SRAM is presented. TSMC (Taiwan Semiconductor Manufacturing Company) 1P6M 0.18 μm CMOS process with 1.8 V power supply is employed to carry out the entire design. By taking advantage of the large current provided by low V_{TH} and low leakage provided by the high V_{TH}, the threshold voltage of the wordline controlled NMOS transistors of memory cells are variable. When the cell is in the read or write mode, the V_{TH} of the wordline controlled NMOS transistors is pulled high such that the drain current will be increased. By contrast, if it is idle in a standby mode, their bulk voltage will be reduced by shorting their bulk to a ground voltage . The proposed 4-Kb 6-T SRAM is measured to possess a 2.2 ns access time in the R/W mode, and consume 43.6 mW in the standby mode. The highest operating clock rate is 667 MHz.

Indexing terms : SRAM, dynamic threshold voltage, 6-T memory cell, dual V_{TH}

1. INTRODUCTION

The trend toward portable and small digital equipments or systems is rapidly booming [5]. Microprocessor systems as well as the SOC (system-on-chip) demand large-capacity high-speed low-power on-chip memories. Particularly, embedded SRAMs and caches. Although 4-T SRAM, [7], [6], [4], [9], and 1-T SRAM, [3], have been announced to reduce the area cost, all of these designs require either extra circuitry to resolve the weak "0" (or weak "1") problem, poor driving and retention capability, or extra process to increase the capacitance at the data node. What even worse is some of the prior designs might need extra voltage source, [4]. Not only are 6-T SRAMs [5] are easily embedded in logic LSIs owing to its compatibility with the CMOS logic process, their access time will be the shortest given same conditions [1]. In this paper, we propose a novel high-speed 6-T SRAM cell which eliminates any wordline compensation and improve the accessing time. By taking advantage of the triple-well process, the bulk voltage of the wordline-controlled transistors is variable. If the cell is in an idle mode, the bulk voltage is pulled low to increase the threshold voltage such that the leakage is reduced. On the other hand, if the cell is in the access (R/W) mode, the bulk voltage is pulled high to reduce the threshold voltage which leads to a high driving current. In short, the threshold voltage of these transistors depends on the mode of the cells.

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2. DYNAMIC V_{TH} WORDLINE-CONTROLLED MOS

According to [1], we attain the following V_{TH} formulation

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|\,2\phi_F\,| + V_{SB}} - \sqrt{|\,2\phi_F\,|}) \quad (1)$$

where V_{TH0} denotes the threshold voltage with a zero bulk bias, ϕ_F is electrostatic potential, γ is the body coefficient, and V_{SB} is the bulk bias. It is concluded that the V_{TH} is adjustable if the bulk bias is tuned.

Meanwhile, the driving capability of the cell depends on the current supplied by the wordline-controlled transistors.

$$I_D = \frac{K_p}{2}\frac{W_{eff}}{L_{eff}}(V_{GS} - V_{TH})^2 \quad (2)$$

where W_{eff} and L_{eff} respectively denotes the effective channel width and length. Thus, if the V_{TH} is pulled low, the supplied current will be increased such that the capacitive load on bitlines can be charged faster. Hence, it is desirable when the cell in an accessing R/W mode.

On the other side, if the cell is not activated, the standby current should be reduced in order to minimize the standby power as well as retain the stored

data. Basing upon the following equation, the V_{TH} should be boosted in such a scenario.

$$I_{leak} = \frac{W_{eff}}{W_0} \cdot I_0 \cdot 10^{-V_{TH}/S} \quad (3)$$

where W_0 and I_0 are the zero-biased gate width and drain current, respectively, and S is the subthreshold swing parameter which can be calculated as :

$$S \approx 2.3V_T \left[1 + \frac{C_d}{C_{ox}}\right] \quad (4)$$

where V_T is thermal voltage, C_d is the junction capacitance between source and drain.

2.1. Analysis of the optimal V_{TH}

It is well known that V_{TH0} in Eqn. 1 is expressed as follows,

$$V_{TH0} = \phi_{MS} + 2\phi_F + \frac{Q_{dep}}{C_{ox}}, \quad (5)$$

where ϕ_{MS} is the difference between the poly gate and the silicon substrate, Q_{dep} is the charge in the depletion area.

Usually, $\phi_F \in [0.25, 0.35]$ V. $\gamma = \sqrt{2q\epsilon_{Si}N_{sub}}/C_{ox}$, which is the range of $0.3 \sim 0.4$ $V^{\frac{1}{2}}$. Thus, we conclude that all of the factors in Eqn. 1 besides V_{SB} are constants. Then, since $\gamma > 0$, the minimal V_{TH} will occur at $\sqrt{\mid 2\phi_F \mid + V_{SB}} = 0$. That is, $2\phi_F = -V_{SB}$. Hence, $V_{BS} = 2 \times \phi_F = 0.5 \sim 0.7$ V will produce the minimal V_{TH}.

2.2. SRAM cell with dynamic V_{TH}

Basing on the analysis given in the previous section, we propose a 6-T SRAM cell in Fig. 1. The bulk bias of the two wordline-controlled NMOS transistors, NM11 and NM12, is coupled to V_{BS}. (Notably, $V_{BS} = -V_{SB}$.) Fig. 2 shows the simulation results when V_{BS} is varied from -1.8V to +1.8V. It is found that the largest drain current supplied by these two accessing transistors occurs at $V_{BS} = 0.7$V. The simulation result extactly matches what we expected in the previous section.

Fig. 3 further reveals the advantage of the speed performance of our design. Given the same geometry and load (0.1 pF, TT model, 25°C), the prior 6-T SRAM consumes 3.36 ns to pull the bitline up to 1.0 V. Our new cell takes only 2.08 ns. The improvement is almost 38%.

2.3. Layout of the proposed SRAM cell

Since the dynamic V_{TH} mush be carried by triple-well process, the area required by the design rules will be increased. Fig. 4 shows the layout of the proposed SRAM cell using the triple-well process.

2.4. Predischarging bitlines

The function of either precharging or predischarging the bitlines is to prevent any leftover charge thereon from causing the unwanted activation of the following sense amplifier. If the precharging scheme is adopted, slow PMOS transistors are inevitably used. Hence, we utilize a faster predischarging scheme by using NMOSs as the switches to fasten the speed.

3. SIMULATION AND IMPLEMENTATION

Fig. 5 shows that overall layout of the proposed SRAM. The chip area is $678.5 \times 1253.9\,\mu m^2$. The characteristics of the chip is tabulated the Table 1.

normal mode	clock	667 MHz
	access time	2.2 ns
	VDD	1.8 V
	avg. power	182 mW
	max/min power	848/43.6 mW
BIST mode	clock	100 MHz
	VDD	1.8 V
	avg. power	33.7 mW
	max/min power	582/0.95 mW

Table 1: Characteristics of the proposed SRAM

Fig. 6 is the worst-case post-layout simulation results given by TimeMill at 100°C, SS model, VDD = 1.6 V. The functionality as well as the speed performance is still maintained.

4. CONCLUSION

We have proposed a 4-Mb 6-T CMOS SRAM comprising wordline-controlled transistors with dynamic threshold voltages. The bulk bias of the wordline-controlled transistors depends on the mode of the cell. Hence, not only the speed performance is enhanced, the standby power dissipation is also reduced drastically.

5. REFERENCES

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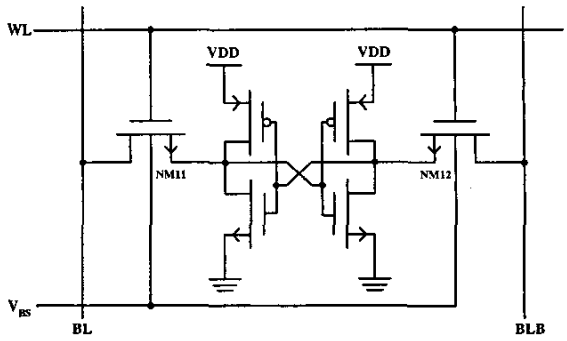

Figure 1: proposed SRAM cell

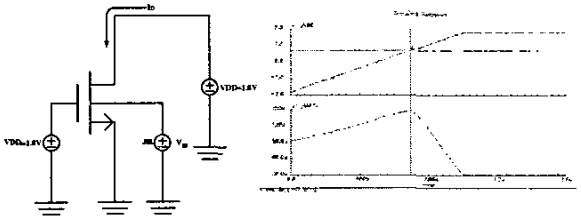

Figure 2: simulation result to find the optimal V_{TH}

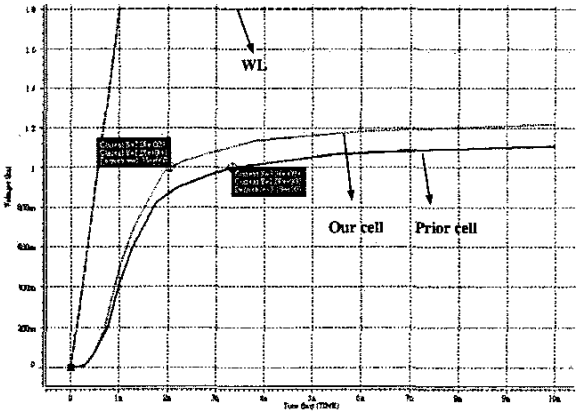

Figure 3: comparison of the proposed cell with prior cells

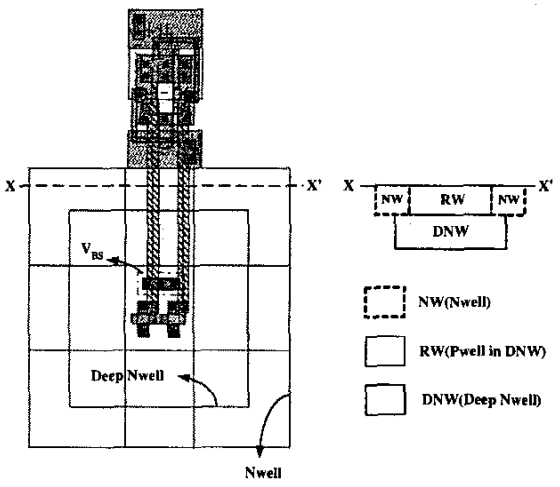

Figure 4: layout of one cell using the triple-well process

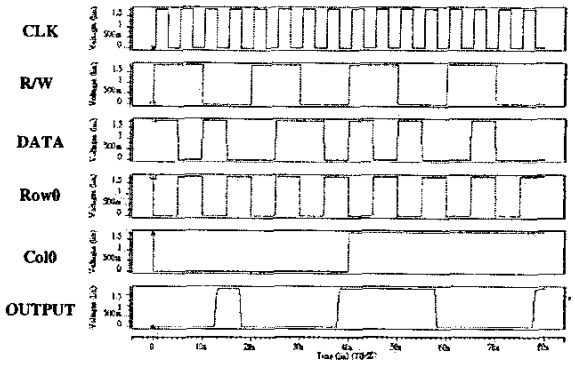

Figure 6: worst-case post-layout simulation

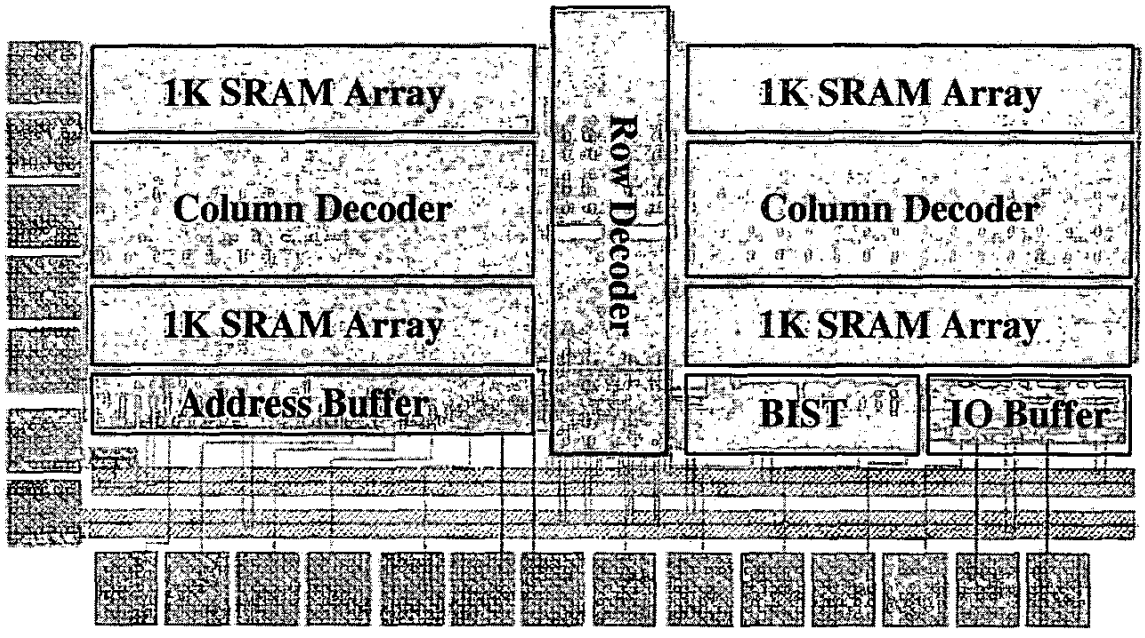

Figure 5: layout of the 4-Kb SRAM