6-T SRAM Using Dual Threshold Voltage Transistors and Low-Power Quenchers§

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ABSTRACT

Static random access memories (SRAM) are widely used in computer systems and lots of portable devices. In this paper, we proposed an SRAM cell with dual threshold voltage transistors. Low threshold voltage transistors are mainly used in driving bit lines while high threshold voltage transistors are used in latching data voltages. The advantages of dual threshold voltage transistors can be used to reduce the access time and maintain data retention at the same time. Besides, the unwanted oscillation of the output bit lines of memories caused by large currents in bit lines is reduced by adding two back-to-back quenchers therebetween. The proposed quenchers not only prevents the oscillation, but also reduces the idle power consumption when the memory cells are not activated by the word-line signal. Meanwhile, large noise margin is provided such that the gain of the sense amplifier won't be reduced to avoid the oscillation. Hence, high-speed and low-power readout operations of the SRAMs is feasible.

1. INTRODUCTION

Semiconductor memories, particularly SRAMs, are widely used in electronic systems [1], [2], [3]. Thanks to the advance of semiconductor process, e.g., TSMC 0.25 μm 1P5M CMOS process, dual threshold voltage transistors are available now. The low threshold voltage is called Native V_{th} (V_{th} = 0.21V) and the high threshold voltage is called Nominal V_{th} (V_{th} = 0.53V) in the TSMC process. Low threshold voltage transistors are capable of supplying large current while high threshold voltage transistors are good in reducing leakage current. Hence, the former is a good bit line driver while the latter is an excellent data latch candidate. If low-V_{th} transistors are used as bit line drivers and high-V_{th} transistors are the data latch components, not only can the access time be shortened, the data retention is also enhanced. Besides, the oscillation of the bit line (BL) and a complementary bit line ($\overline{BL}$) might introducing unwanted power dissipation due to the large current supplied by low-V_{th} transistors, a possible wrong reading will be produced [5]. In this work, we introduces 'quenchers' to subside the oscillation while still keep the speed of readout operations. On top of quenching the oscillation, the power saving is also verified by HSPICE simulations regardless of MOS models, temperature variations, and input signal frequency.

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2. DUAL-V_{TH} SRAM

2.1. Dual-V_{th} cell

A typical 6-transistor (6-T) SRAM cell is shown in Fig. 1. N1 and N2 are respectively the bit lines (BL, $\overline{BL}$) drivers which are controlled by word line (WL). If the threshold voltage of N1 and N2 is low, the switching time of N1 and N2 will be reduced which will in turn shorten the access time of the SRAM cell. Hence, we use Native V_{th} provided by TSMC 0.25 μm 1P5M process to implement low threshold voltage driving transistors. It will produce more driving current than normal or high-V_{th} driving transistors. By contrast, transistors with high V_{th} possess low leakage current and subthreshold current. Thus, they are very good to be cross-coupled as a data latch as shown in Fig. 1. We, then, use Nominal V_{th} transistors such as P1, P2, N3, and N4 to keep valid data. The difference between high-V_{th} transistors and low-V_{th} transistors is summarized in Table 1.

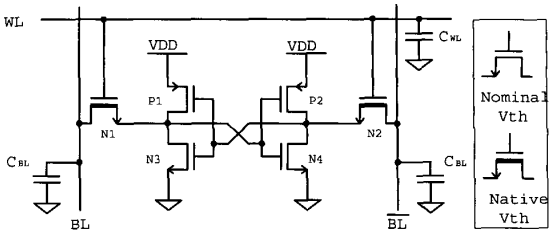


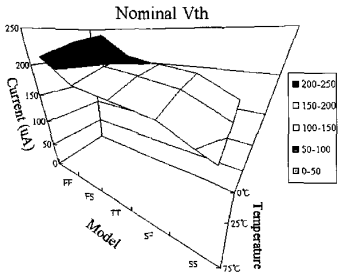
Fig. 1. Schematic View of SRAM Cell (I)

V_{th}	characteristic	advantage
Nominal (0.53 V)	low leakage current	data retention
Native (0.21 V)	high output current, fast switching time	driving capability

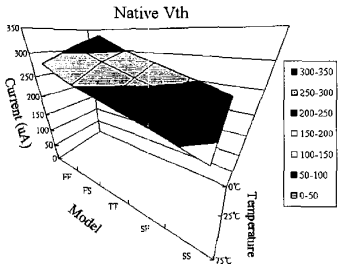
Table 1. Comparison between high and low threshold voltage transistors

2.2. Simulation

To verify the proposed cell, we perform a series of simulations under the temperature of 0°C, 25°C, and 75°C. Different transistor models, such as TT, SS, SF, FS, and FF, are all simulated. The complete simulation result is shown in Fig. 2. As we expected, the Native V_{th} in the simulations provides more driving capability, i.e., current, than Nominal V_{th}. Besides, a current comparison of Nominal V_{th} with Native V_{th} is tabulated in Table 2.



(a) Nominal V_{th}



(b) Native V_{th}

Fig. 2. Simulation with different models, temperatures, and threshold voltages

Model	Current Increase (%)		
	0°C	25°C	75°C
TT	39.70	36.13	33.33
SS	41.10	37.82	33.33
SF	33.51	30.60	26.19
FS	45.41	42.93	38.46
FF	39.42	35.34	31.31

Table 2. Current increase for Native V_{th} vs. Nominal V_{th}

According to the simulation results in Fig. 2 and Table 2, it is no doubt that Native V_{th} does provide better driving current. It will provide up to 45.41% current increase in the best case, 26.19% in the worst case. Hence, using low threshold voltage driving transistors is proven to be feasible.

3. QUENCHERS

In this section, we point out the reason of the oscillation of the SRAM bit lines [4]. Meanwhile, the resolution to squelch the oscillation is also proposed.

3.1. Oscillations on the bit lines

Referring to Fig. 3, a conventional current sense amplifier (SA) and the SRAM memory cells are shown. Basically, the datapath from a memory cell to the outputs consists of a current source enabled by the complement of a sense amplifier enable signal, $\overline{\text{SAEN}}$. A differential amplifier, an equalizer which is used to pre-equalize the bit lines, and a current sink which is also enabled by $\overline{\text{SAEN}}$. The oscillation of the readout operation is illustrated in Fig. 4. The oscillation will be significantly enlarged when the low-V_{th} NMOSs are used as bit-line drivers since they supply large currents.

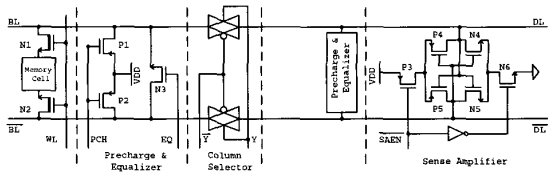


Fig. 3. Conventional memory configuration

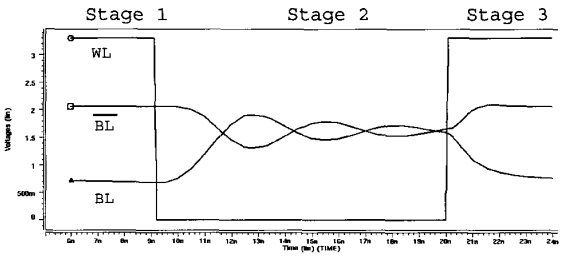


Fig. 4. Oscillation scenario

Stage 1 : WL (wordline) is enabled to activated the memory cell. $\overline{\text{SAEN}}$ is 1 at this moment. The equalizer is off. Hence, The voltages on the respective outputs of the bit lines are clearly either pulled up or pulled down.

Stage 2 : WL is disabled such that the memory cell is de-activated. Owing to the high gain of the differential amplifier, the difference of the voltages of the bit lines will be enlarged. In the meantime, the $\overline{\text{SAEN}}$ is kept to be enabled, which in turn causes the oscillation.

Stage 3 : $\overline{\text{SAEN}}$ is switched to 0. The entire datapath waits for the next valid WL = 1 and $\overline{\text{SAEN}}$ = 1.

In short, the scenario of the oscillation of the voltages on the bit lines occurs when WL does not enable the memory cell and the $\overline{\text{SAEN}}$ is activated. Particularly, the oscillation becomes very drastic if the gain of the sensor is very large which is originally intended to accelerate the readout. Not only an error might be generated, but also the unwanted power consumption occurs.

3.2. Quenchers

By a simple observation, the voltage phases of the signals on the respective bit lines are complementary when the bit lines are activated. We can simply create a unidirectional closed loop which short-circuits the bit lines at this moment in order to cancel out the out-of-phase ripples of the voltages of the fed signals. Referring to Fig. 5, two back-to-back diodes are used to form such a unidirectional loop between the bit lines. By using the identical simulation conditions as those given in Fig. 4, Fig. 6 shows a significant improvement on the squelch of the oscillation.

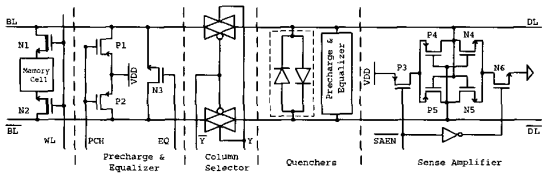


Fig. 5. Memory cells with quenchers

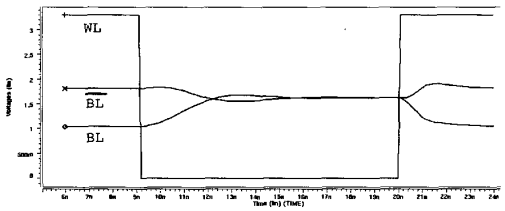


Fig. 6. Diodes as quenchers

3.3. Noise margin improvement

Another advantage of the quenchers is the improvement of the noise margin, particularly if the V_{OH} is critical [5]. Referring to Fig. 3, the values of the bit lines may oscillate when the power supply VDD is high and the gain of the amplifier is very large. Note that the gain is determined by the size of the transistors in the differential amplifier and those in the current sink. The sensing speed of the current SA increases as the gain grows. However, the output could be incorrectly sensed if the oscillation occurs and the gain is high. This possibility leads to a small noise margin, VDD - V_{OH}. By contrast, the insertion of a quencher pair suppresses the oscillation such that the noise margin is increased without the hazard of incorrect sensing. Meanwhile, the gain of the current SA is preserved so as not to slow down the readout operation in any case.

3.4. Alternatives of quenchers

Besides the diodes which is deemed as a non-linear element in a standard CMOS process, other alternatives can be used to be the quenchers. The performance of these alternatives turns out to be not worse than the diodes'.

NMOS pass transistor : NMOSs with gate voltage at full Vdd are considered as another alternative. They are easily to be designed and integrated.

PMOS pass transistor : In dual respect, PMOSs with gate voltage at GND are considered as the last alternative. They are also easily to be designed and integrated.

3.5. Simulations and Analysis

By employing the same TSMC 0.25 μm 1P5M CMOS process, we have simulated several corner conditions to attain the power performance. Note that the operating frequency of the WL is 200 MHz. Table 3 shows the comparison of average, maximum, and minimum power dissipations given different simulation conditions.

Simulation			No Quenchers			+ Quenchers			Reduction
Model	^oC	VDD	avg	min	max	avg	min	max	%
TT	25	2.5	73.76	1.710	1149	61.06	1.710	304	17.22
SS	75	2.2	35.84	0.803	209	35.33	0.803	214	1.42

Table 3. Comparison of power consumption (unit = mW)

It is noted that the proposed quenchers indeed reduce power no matter what the condition is. On top of these simulation results, Fig. 7 also shows the current variations in the conventional design and the proposed quencher design. Besides, according to all of these simulation results, NMOS pass transistors seem to possess the edge of power saving.

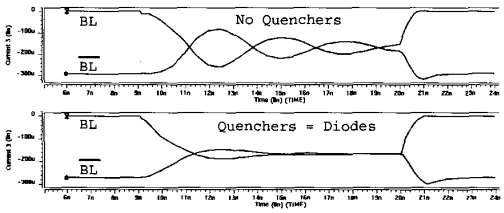


Fig. 7. Current comparison

4. IMPLEMENTATION & COMPARISON

We design and implement a 4 Kb SRAM by using the mentioned 0.25 μm process. Fig. 8 is the post-layout simulation results given by TimeMill while Fig. 9 is the die photo of the proposed 4 Kb SRAM chip. The chip is tested and veryfied using HP 1660 CP logic analyzer and IMS 200 test station [8], respectively. Fig. 10 is the BIST test using HP 1660 CP logic analyzer given a 100 MHz clock while Fig. 11 is the continuous read/write test using IMS 200 test station. The minimal access time of the SRAM is 5.0 ns and the maximum operation frequency is 100 MHz. The test results demostrate that the chip is fully functional. A performance comparison with currently commercial SRAM products is tabulated in Table 4 which proves that the proposed SRAM is faster than the other commercial products. The characteristics of the proposed SRAM chip are summarized in Table 5.

SRAM	VDD	access time	clock rate	Process
Proposed	2.5 V	5.0 ns	100 MHz	0.25 μm
[6]	2.7-3.6 V	70-85 ns	1-10 MHz	0.18 μm
[7]	3.3 V$\pm$0.3V	10 ns	100 MHz	0.18 μm

Table 4. Comparison between the proposed architecture and commercial products.

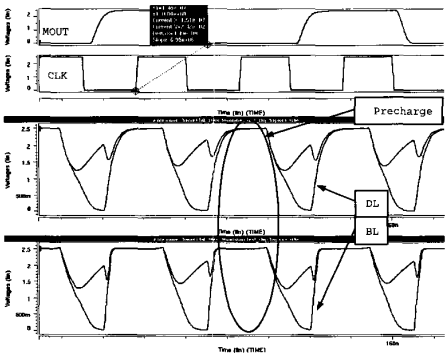


Fig. 8. Post-layout simulation waveform

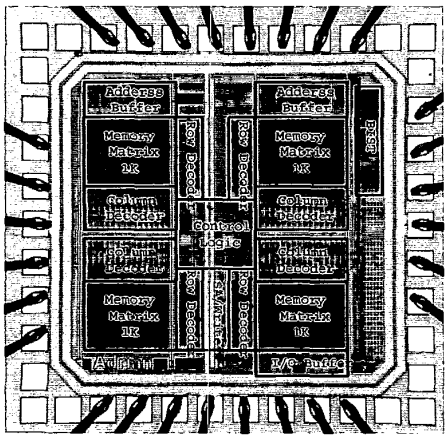


Fig. 9. Die photo of the SRAM chip

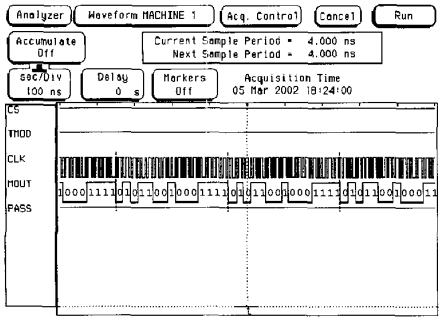


Fig. 10. BIST test using HP 1660 CP LA under 100 MHz.

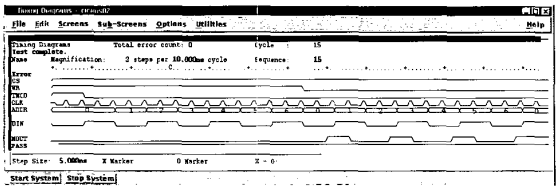


Fig. 11. Continuous read/write test using IMS 200 test station given a 100 MHz clock.

Area	1.28 × 1.25 mm^2 (with pads)
Maximum Freq.	100 MHz
Avg. Power	59.5 mW (100 MHz, 2.5V)
Access Time	5.0 ns
Standby Power	26.5 mW

Table 5. Chip summary

5. CONCLUSION

In this paper, an SRAM using dual threshold voltage transistors is proposed. The low-V_{th} transistors are used to increase driving capability and speed. The high-V_{th} transistors, by contrast, are used to construct data storage latches. Meanwhile, a novel quencher design is proposed to be added at the output bit lines of memories which will reduce unwanted oscillation and will also supress the unwanted power dissipation. According to the simulation results, NMOS pass transistors seem to be a better choice of the quenchers. A 4 Kb SRAM is implemented by using the dual threshold transistors and the quenchers. The simulation result demostrates that the proposed architecture is better than prior commercial products using the same or better technology.

6. REFERENCES

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