A POWER-EFFICIENT CLAMPING CIRCUIT FOR CHARGE PUMPS USED IN LOW VOLTAGE MEMORIES[§]

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ABSTRACT

A voltage clamping circuit composed of MOS transistors with different threshold voltages is presented in this work to resolve the output stabilization of charge pumps. The charge pumps used in low voltage memories are intended to provide high voltages in case of programming, erasing, or R/W operations. The proposed design is carried out by solely MOS transistors without any passive elements to replace common regulators at the output. Hence, neither voltage comparator nor voltage divider is needed in the proposed design. The clamped output voltage which the proposed design can provide is contained in 2.8 V to 3.6 V given VDD = 0.8 V to 1.3 V. The proposed circuit is implemented by TSMC 0.25 μm 1P5M CMOS technology. The maximum power dissipation is estimated to be 285.8 μW given 10 MHz clocks.

Indexing terms : charge pump, regulator, dual threshold voltage, feedback, gate drive

1. INTRODUCTION

Charge pumps play an important role in high voltage generators for non-volatile memories, e.g., FLASH and EEPROM [5], [8]. In addition, ultra low-voltage volatile memories, e.g., DRAM and SRAM, also demand boosted voltage generators to compensate the threshold voltage of the MOS or boosting bit line voltage to raise the speed of readout operations [2], [4]. However, since the boosting ratio of the charge pumps are mostly linear. Any overshoot or undershoot at the inputs of the charge pumps will introduce unwanted voltage spikes delivered to the core of the memories. Severe damages such as permanent defects might be resulted. Most of the prior charge pumps adopt regulators at the output to stabilize the output voltage, [1], [6], [8]. Unavoidably, voltage comparator, voltage divider or distributer, resistors and capacitors are often required. The area cost, thus, becomes unacceptable when large resisters and capacitors are used in the regulators or voltage reference generation circuitry. In this paper, we present an clamping circuit to contain the output voltage by taking advantage of MOS transistors with different V_{th}.

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2. CHARGE PUMP WITH A CLAMPING CIRCUIT

A multi-stage charge pump, e.g., a Dickson's booster [7], can be used with an effective boost ratio. However, the ratio itself from time to time is linear. Hence, for an input voltage higher than a certain value which may be introduced by noise or power supply spikes, the effective boost ratio results in an output voltage larger than required. Even though the damage might not be immediate to the chip, high output voltage which is used to boost bitlines or wordlines will cause shorter life time of the battery or core cells.

2.1. Basic theory

Referring to Fig. 1, the proposed clamping circuit (clamper) is coupled to a charge pump via a sample-and-hold (SH) circuit. The control signals fed into the clamper are ATD (address transition detection) [9] and $\overline{\text{ATD}}$ to generate a "clamped" input named V_c to the SH block. The control signals to determine the switches in the SH circuit are ATD (address transition detection) and $\overline{\text{ATD}}$ as well. The charge pump could be either a two-phase clock driven [7] or 4-phase clock driven design [3].

A simple thought to contain the output voltages is to chop the swing of the driving clocks to the charge pumps. Hence, the source of the NMOS transistors of the clock buffers in the charge pump will be coupled to the sampled output of the SH circuit, which is also the clamped voltage generated by the clamper.

2.2. Clamping circuit

The schematic of the proposed clamper is revealed in Fig. 2. Note that the swing of ATD and

$\overline{\text{ATD}}$ are VDD which is generated by the charge pump. Hence, it is assumed to be a variable.

Case 1 : ATD = low, $\overline{\text{ATD}}$ = high
V_{th5} is the threshold voltage of M5. M1 is on, while M2 is off. The gate drive to M7 and M8 are high, which in turn pulls down output, V_c. In the mean time, M4 is off, which cuts off the current source into M5. M6 turns into a forward self-biased diode with a small voltage drop $\approx$ 100 mV. Thus, M3 is turned on to keep the gate drive of M7 and M8 high. V_c is maintained by the closed feedback loop.

Case 2 : ATD = high, $\overline{\text{ATD}}$ = low, and VDD $>\mid V_{th5} \mid$
As soon as the ATD turns high, M1 is off and M2 is on. Since the gate drive of M3 is kept at 100 mV at the beginning, the gate drive of M7 and M8 can be kept high as long as the resistance of M2 is larger than that of M3. In other words, we need a "long" M2 and a "wide" M3 to keep this initial condition hold long enough. V_c, hence, is still low initially to turn on M5. On top of that, low $\overline{\text{ATD}}$ turns on M4. The gate drive of M6 is pulled high to shut off M3. The gate drive of M7 and M8 is then weakened to pull up V_c to turn off M5. Then, the oscillation cycle repeats. The steady state, V_c = VDD - $\mid V_{SG5} \mid$, will be reached.

Case 3 : ATD = high, $\overline{\text{ATD}}$ = low, and VDD $<\mid V_{th5} \mid$
The initial state is identical to that in Case 2 : When the ATD turns high, M1 is off and M2 is on. Since the gate drive of M3 is sill low at the beginning, the gate drive of M7 and M8 can be kept high as long as the resistance of M2 is larger than that of M3. V_c, hence, is still low initially to turn on M5. However, $V_{SG5} \approx \mid$ VDD $- V_c \mid < \mid V_{th5} \mid$ to make M5 stay shut off. M6 is still nothing but a forward self-biased diode with a small voltage drop $\approx$ 100 mV. Thus, M3 is turned on to keep the gate drive of M7 and M8 high. V_c is kept low.

Based upon the operation described in the above, we learn that the W/L ratio of M2 to M3 is a factor. $Z_{M2} > Z_{M3}$ is the key to success. Besides, the threshold voltage of M6 must be small to provide a low gate drive to turn on M3. Last but not least, V_{th5} determines the function of VDD vs. V_c. It should be high enough to contain the range of the output voltage. In short, the guidelines of the proposed design are as follows:
(1). $Z_{M2} > Z_{M3}$
(2). Use a native V_t (low threshold voltage) transistor to be M6.
(3). Use a nominal V_t (normal threshold voltage) transistor to be M5 of which the bulk voltage is increased to generate a high V_{th5}.

2.3. Sample and hold circuit

The SH circuit is shown in Fig. 3. Notably, the V_c is still low after a 0-to-1 transition of ATD. Two analog switches are then required to sample and hold the V_c. The capacitance of C_{SH1} andC_{SH2} must be large enough, e.g., $\geq$ 10 pF to override the current roll-back from charge pump. Meanwhile, C_{SH1} is preferably larger than C_{SH2} to avoid the charge-sharing effect. Thus, we conclude that VDD - $\mid V_{SG5} \mid = V_c \approx V_{SH1} \approx V_{SH2}$ in Case 2.

2.4. Charge Pump

A modified Dickson-like charge pump is given in Fig. 4. The output of the SH block is coupled to the source of the pull-down NMOS of the clock buffers driven by CLK1 and CLK2. The swing of the clock buffers is limited to VDD - V_{SH2}. We define it to be V_{clamp} = VDD - V_{SH2} = V_{SG5}.

The MOSs consisting the clock buffers possess medium V_t ($\approx$ 0.3 V). To ensure that every MOS in the following pumping stages can be turned on, all of the MOSs in the pumping chain are native V_t ($\approx$ 0.2 V). The output voltage of the charge pump is summarized as :

$$\begin{aligned} \text{VOUT} &= \text{VDD} + 4(\text{VDD} - V_{SH2}) - 5 \cdot 0.2 \\ &= \text{VDD} + 4 \cdot V_{clamp} - 1.0 \end{aligned} \quad (1)$$

By contrast, if the clamper is removed, the final output becomes the following result.

$$\text{VOUT} = 5 \cdot \text{VDD} - 1.0 \quad (2)$$

Therefore, the proposed circuit provides the clamping function to the charge pump to prevent any unwanted voltage spikes.

3. SIMULATION AND IMPLEMENTATION

The proposed design is carried out by using TSMC 0.25 μm 1P5M CMOS process in CADENCE EDA tools. Fig. 5 shows the simulation results of V_c given different VDDs. The oscillations occurring at Case 2 are subsided gradually due to the implicit feedback loop. It is also verified that the clamper will not work when VDD is lower than 0.8 V, since M4 is off in such a scenario. Fig. 6 shows the curve family of VOUT when VDD is changed from 0.8 V to 1.3 V. Post-layout simulation results are shown in Fig. 7 (FF model and 8 (SS model) provided that the testing conditions are 25^{o}C, and VOUT $\in [0.8, 1.3]$ V. The VOUT is contained in the range between 2.8 and 3.6 V, i.e., 3.2$\pm$0.4 V . The clamping, thus, is proven to eliminate the linear pumping ratio effect. Meanwhile, we can tell the difference between with clamping and without clamping by the curves in Fig. 9. The features of our circuit in Fig. 10 which is the layout of the proposed design is summarized as Table 1.

The comparison between our design and two prior charge pumps are shown in Table 2. Notably, Miyawaki's [5] employed two large resistors to reduce power dissipation at the expense of chip area, while

CLK1, CLK2	10.0 MHz
ATD	5.0 MHz
avg. power	0.2858 mW @ VDD=1.3 V
die area	540×563 μm^2
core area	318×324 μm^2

Table 1: The characteristics of the proposed chip (25^oC, TT models)

Calligaro's [1] tried to use a voltage divider composed of large capacitors to reduce the area cost. Both of these prior designs depend on precise passive elements which are very vulnerable to process variations.

	[5]	[1]	ours
max. power	0.4425 mW	0.4360 mW	0.2858 mW
core area	(NA)	(NA)	318×324 μm^2

Table 2: The comparison with prior designs (VDD=1.3V, VOUT=3.6V)

4. CONCLUSION

A clamping circuit utilizing an implicit feedback loop as well as MOS transistors with different threshold voltages is added to charge pumps to stabilize the output voltage. The unwanted output voltage spikes introduced by the linear pumping ratio are prevented. Not only are possible damages to the memory cores avoided, the power dissipation and chip are reduced in contrast with prior regulator methods

5. REFERENCES

[1] C. Calligaro, P. Malcovati, and G. Torelli, "Voltage multiplier with output stabilization," *2000 IEEE Asia-Pacific Conf. on Circuits & Systems (APCCAS'2000),* pp. 622-625, Dec. 2000.

[2] Y.H. Kim, J.K. Nam, Y.S. Sohn, S.C. Heo, S.H. Lee, H.J. Park, Y.S. Han, J.I. Doh, Y.J. Choi, J.H. Choi, J.S. Choi, and C.S. Park, "Two-phase boosted voltage generator [CMOS DRAMs]," *6th International Conference on VLSI and CAD (ICVC'99),* pp. 586-589, 1999.

[3] H. Lin, K.-H. Chang, and S.-C. Wong, "Novel high positive and negative pumping circuits for low supply voltage," *1999 IEEE Inter. Symp. on Circuits and Systems (ISCAS'99),* vol. 1, pp. 238-241, 1999.

[4] K.-S. Min, and J.-Y. Chung, "A fast pump-down V_{BB} generator for sub-1.5-V DRAMs," *IEEE J. Solid-State Circuits,* vol. 36, no. 7, pp. 1154-1157, July 2001.

[5] Y. Miyawaki, T. Nakayama, S.-I. Kobayashi, N. Ajika, M. Ohi, Y. Terada, H. Arima, and T. Yoshihara, "A new erasing and row decoding scheme for low supply voltage operation 16-Mb/64-Mb flash memories," *IEEE J. Solid-State Circuits,* vol. 27, no. 4, pp. 583-588, Apr. 1992.

[6] G. A. Rincon-Mora, and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator" *IEEE J. Solid-State Circuits,* vol. 33, no. 1, pp. 36-44, Jan. 1998.

[7] T. Tanzawa, and T. Tanaka, "A dynamic analysis of the Dickson charge pump circuit," *IEEE J. Solid-State Circuits,* vol. 32, no. 8, pp. 1231-1240, Aug. 1997.

[8] T. Tanzawa, and T. Tanaka, K. Takeuchi, and H. Nakamura, "Circuit techniques for a 1.8-V-only NAND flash memory," *IEEE J. Solid-State Circuits,* vol. 37, no. 1, pp. 84-89, Jan. 2002.

[9] C.-C. Wang, and J.-J. Wang, "Address transition detector with high noise immunity," *2001 The 12th VLSI Design/CAD Symposium,* C3-3, pp. 62, Aug. 2001.

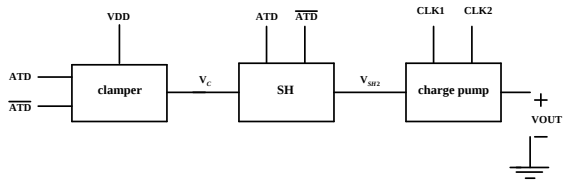

Figure 1: Proposed clamping circuit and the charge pump

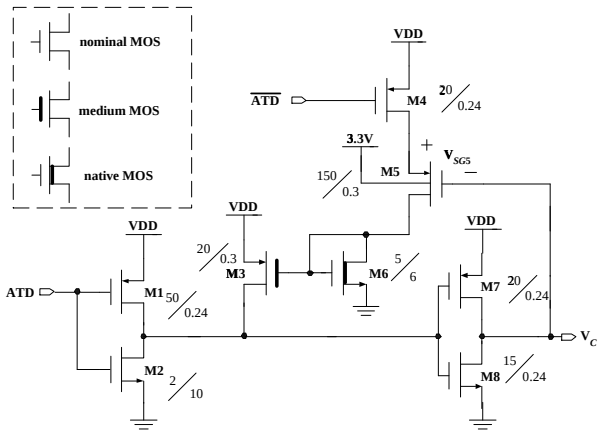

Figure 2: Schematic of the proposed clamper

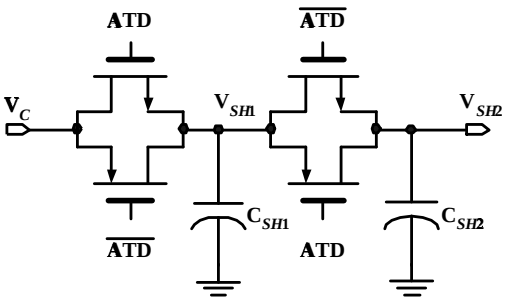

Figure 3: Schematic of the SH circuit

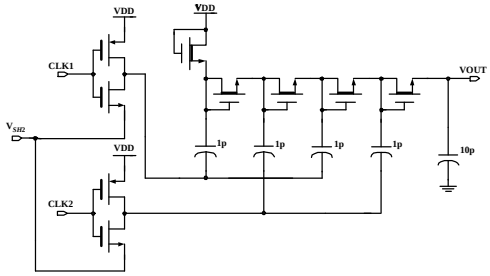

Figure 4: Charge pump

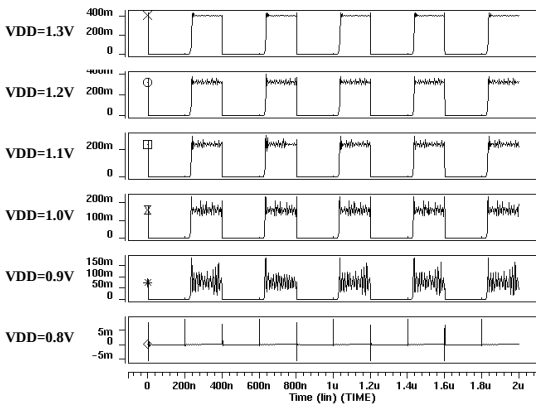

Figure 5: V_c waveforms given different VDDs

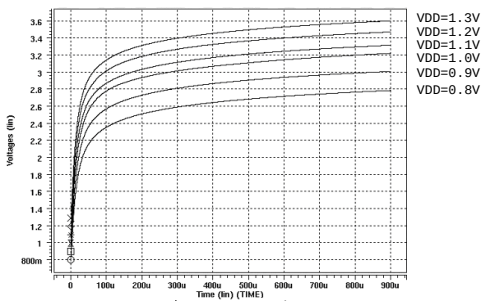

Figure 6: Curve familiy of V_c vs. VOUT given different VDDs

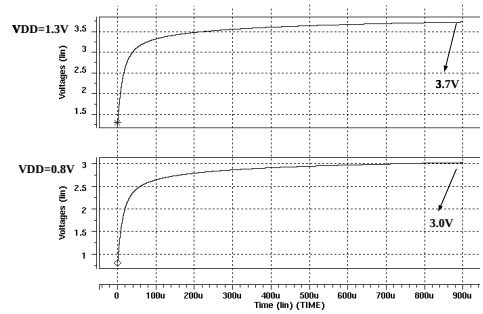

Figure 7: Post-layout simulation I (FF model)

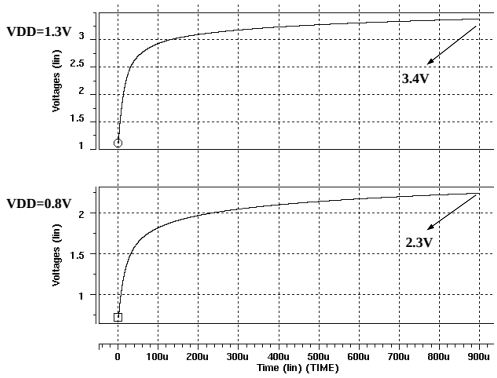

Figure 8: Post-layout simulation II (SS model)

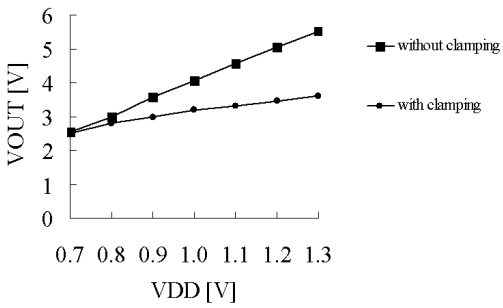

Figure 9: Comparison between with clamping and without clamping

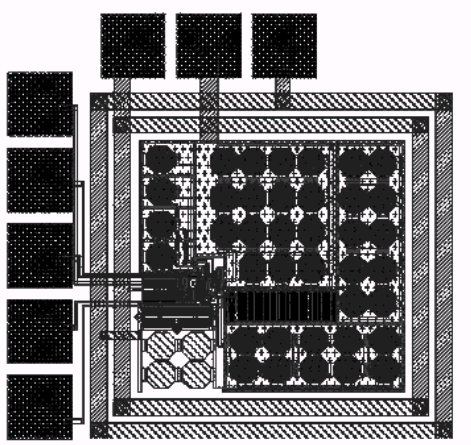

Figure 10: Layout of the proposed design