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A FAST DYNAMIC 64-BIT COMPARATOR WITH SMALL TRANSISTOR COUNT

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ABSTRACT

In this paper, we propose a 64-bit fast dynamic CMOS comparator with small transistor count. Major features of the proposed comparator are the rearrangement and re-ordering of transistors in the evaluation block of a dynamic cell, and the insertion of a weak n feedback inverter, which helps the pull-down operation to ground. The simulation results given by pre-layout tools, e.g., HSPICE, and post-layout tools, e.g., TimeMill reveal that the delay is around 2.5 ns while the operting clock rate reaches 100 MHz.

1. INTRODUCTION

High speed operation has long been a target of circuit design owing to the speed demand of super-computing, CPU, etc. One of the critical operations is the comparison of two binary data. Theoretically, the fastest comparator is made of full combinatorial logic gates. However, the gate count, the area and the fan-in will be problems when the length of the data is very large, e.g., $n = 64$. Besides, wide bit comparators are key components in the design of parallel testing, signature analyzer and built in self test (BIST) circuits etc [4]. Although high fan-in gates are useful in a number of applications, they are not practical in a single stage of static CMOS. Since the NMOS and PMOS transistors of a static CMOS gate are dual of each other, one of them will always be arranged in series. These transistors also increase the loading seen by their previous stages. When a large fan-in is required, the dynamic logic, thus, has to be used [2], [1]. Meanwhile, other prior dynamic logic design styles suffer from different difficulties. For example, domino logic [6] can not be noninverting; NORA [6] has the charge sharing problem; all-N-logic [6] and robust single phase clocking [1] cannot operate correctly under clocks with short rise time or fall time, which can not be easily integrated with other part of logic design; single-phase logic [6] and Zipper CMOS [6] contain slow P-logic blocks. In this work, we propose a fast 64-bit dynamic comparator with small transistor count.

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2. FAST 64-BIT COMPARATOR CIRCUIT

2.1. Prior comparators

Three comparator circuits have been proposed [5].

(1). The equality comparator using the combination of XNOR gates and an NAND gate is shown in Fig. 1.

(2). The comparator using a pass-gate logic structure is shown in Fig. 2.

(3). As shown in Fig. 3, another version of the comparator, using a merged XNOR/NOR gate and pseudo-nMOS FETs, is presented.

2.2. Equality comparator

An example of the proposed dynamic CMOS 4-bit equality comparator is shown in Fig. 4. In Fig. 4, when the CLK is low, Node_1 is precharged to VDD. If A<0> and B<0> are both high, then N1 and N2 are on and P1 and P2 are off. Thus no current path exists during the evaluation period, and then Node_1 will be kept high. If A<0> is high and B<0> is low, then N1 and P2 are on. Thus a current path is formed between Node_1 and ground through P2 and N1 during the evaluation period. Then Node_1 will be pulled down. The truth table is tabulated in Table 1. The operation for A<1> and B<1>, A<2> and B<2> and A<3> and B<3> is the same. In short, when any pair of A<i> and B<i> is not equal, a current path will be formed and Node_1 will be low. By contrast, if A<i> is equal to B<i> for all i, Node_1 will keep high [5]. Notably, because PMOSs are used in the discharge path, the voltage of Node_1 can only be discharged to Vtp instead of GND. Thus a latch is required to connect to Node_1. The weak n feedback is used to pull down Node_1 to ground when Node_1 is in the low state. The weak p feedback is utilized

state. Hence, the charge redistribution problem can be resolved. The pull-up time is determined only by the pull-up transistor P0, but the ground switch N0 will increase the pull-down time. Note that the ground switch may be omitted if the inputs of every pair are guaranteed at the same states during the precharge period [2], [5].

2.3. Zero/one detector

The same design methodology can be applied to another important application. That is, the zero/one detector. Notably, detecting all ones or all zeros on wide words requires large fan-in AND or OR gates. Constructing a tree of AND gates can overcome this problem, as shown in Fig. 5. Alternatively, another version of design, as shown in Fig. 6, was also proposed [5]. The zero/one detector is also employed in the parallel testing of memory, where the outputs of the arrays are compared against the expected data, as shown in Fig. 7.

The proposed circuit of a 4-bit zero/one comparator is shown in Fig. 8. When the CLK is low, Node_1 is precharged to VDD. If Ref, the reference data, is set high and D<0>, D<1>, D<2> and D<3> are all high, then N, N0, N1, N2 and N3 are on while P, P0, P1, P2 and P3 are all off. Thus no current path exists during the evaluation period, and then Node_1 will be kept high. Similarly, if Ref is low and D<0>, D<1>, D<2> and D<3> are all low, then N, N0, N1, N2 and N3 are off and P, P0, P1, P2 and P3 are all on. Thus no current path exists during the evaluation period either, and then Node_1 will be kept high, too. If any input is different from Ref, there will be some NMOS and PMOS turned on simultaneously. Then a current path will be formed between Node_1 and ground during the evaluation period. Node_1 will then be discharged to low. The truth table is tabulated in Table 2.

2.4. Transistor count & speed comparison

The total transistor count of the mentioned circuits is summarized in Table 3. Note that tiny XOR with 6 transistors is used for the traditional comparators. It is obvious that the transistor count of the proposed comparators is much less than that of the other comparators with the same functionality. Regarding the speed comparison, Because of the low input capacitance of the dynamic logic, the speed performance is better than that of other logics. The comparisons of input capacitance of different comparators are tabulated in Table 4. Notabley, the input capacitance of the proposed circuit is the minimum. Besides, there are only two stages in the proposed circuits, which make the total delay time shorter. Thus, the speed performance is expected to be better than that of the previous designs.

Following the proposed design strategy, a hierarchical design of a fast 64-bit comparator is shown in Fig. 9, which is composed of eight 8-bit equality comparator and one 8-bit zero/one comparator. The design is carried out by using UMC (United Microelectronics Company) 0.5 μm (2P2M) technology. The individual 8-bit equality comparator respectively determines the equality of one out of the eight bytes of the two input 64-bit data, and produce one output signal to the 8-bit zero/one comparator wherein the Ref is set to "0". Hence, the overall 64 bits are divided into eight bytes which are evaluated at the same time, and then the 8-bit zero/one comparator produce the final output signal. HSPICE is employed to optimized the speed. The length of all of the transistors are all set to 0.6 μm, while their widths are illustrated in Table 5.

3. SIMULATIONS AND CHIP LAYOUT

The entire 64-bit comparator simulated by HSPICE reveals a very short delay as tabulated in Table 6. The clock rate can run up to 200 MHz with 0.01 ps rise/fall time. Fig. 10 is the waveform when the clock rate is 200 MHz, which is the worst case scenario, i.e., there is only one-bit difference between the two 64-bit input data. The TimeMill simulation results indicates a 2.5 ns delay without pads and 4.5 ns with pads. The chip layout with pads is shown in Fig. 11 which occupies 1.8×1.8 mm^2 while the core is only 145×240 μm^2. The data are serially byte-wide I/Oed. We also simulate several comparator designs using different logics. Note that the adders/subtractors are also often used as comparators. The results are tabulated in Table 7.

4. CONCLUSION

Several dynamic CMOS comparators are proposed with a number of advantages. These transistor count is much less than that of the other similar designs. Although it has high fan-in, the number of series transistors is two, which in turns reduce the pull down delay. Compared with XOR-based equality comparators and deterministic comparators, the proposed is much faster. The design methodology is used to implement a fast 64-bit dynamic comparator.

5. REFERENCES

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	A<0> = = B<0>	A<0> ! = B<0>
Node_1	1	0
Output	0	1

Table 1 : Truth table of the equality comparator

	D<i> == Ref	D<i> ! = Ref
Node_1	1	0
Output	0	1

Table 2 : Truth table of the zero/one detector

Equality comparator	Transistor count
Fig. 1	6n+2n
Fig. 2	12n+5
Fig. 3	8n+1
Fig. 4 (The proposed)	4n+6

Zero/one comparator	Transistor count
Fig. 5	4(n/2)+4(n/4)+4(n/8)+..+4
Fig. 6	4(n-1)+2(n/2-1)
Fig. 7	6n+2n
Fig. 8 (The proposed)	2(n+1)+6

Table 3 : Transistor counts comparison (Note: n is the number of the input.)

Equality comparator	Input capacitance
10T XNOR	2 Cgp + 2 Cgn
4T XNOR (cross-coupled)	Cgp + Cgn + Csn
6T XOR A terminal	2 Cgp + Cgn + Csp
6T XOR B terminal	Cgp + Cgn + Csp + Csn
Fig. 2	Cgp + 3 Cgn
Fig. 3	Cgp + 2 Cgn
The proposed	Cgp + Cgn

Table 4 : Input capacitance comparison (Cg is the gate capacitance and Cs is the source capacitance)

Comparator	W in Equality	W in Zero/one
P_{clk}	10	15
N_{clk}	15	20
$P_{evaluation\ block}$	10	2.5
$N_{evaluation\ block}$	5	10
$P_{inverter}$	15	20
$N_{inverter}$	1	2
$P_{feedback}$	0.9	0.9
$N_{feedback}$	0.9	0.9

Table 5 : The transistor width used in our designs. (wire loading = 0.1 pF, unit = μm)

I/O path	Delay
clk -> output	2.126 ns
input -> output	2.120 ns

Table 6 : The delays of the proposed 64-bit comparator.

Logic	delay	# transistors
64-b PLA-ANT CLA [6]	4.0 ns	8352
32-b EMODL adder [1]	2.7 ns	1537 (gates)
8-b TSPC adder (1 μm) [3]	7.5 ns	1832
All-N-logic [3]	Failed	2062
The proposed	2.50 ns	328

Table 7 : The performance comparison of different designs

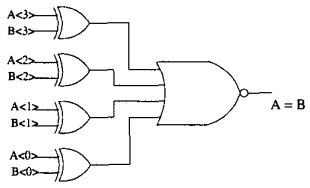

Figure 1: Prior equality comparator (a)

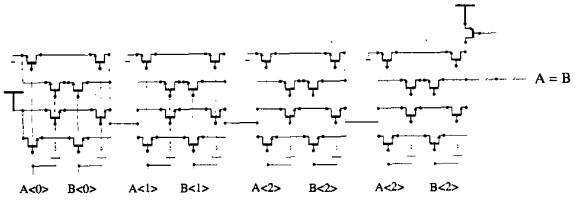

Figure 2: Prior equality comparator (b)

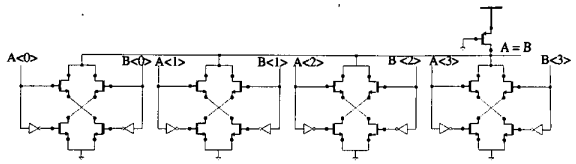

Figure 3: Prior equality comparator (c)

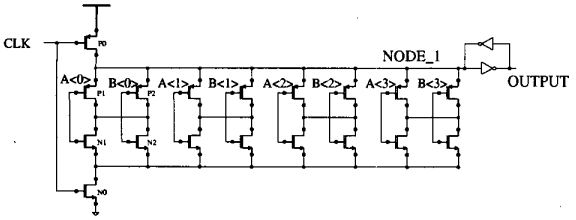

Figure 4: Proposed equality comparator

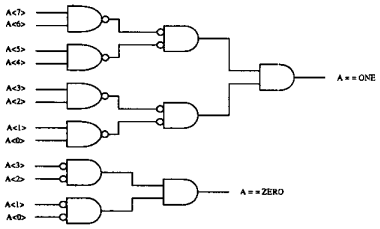

Figure 5: Prior zero/one comparator (a)

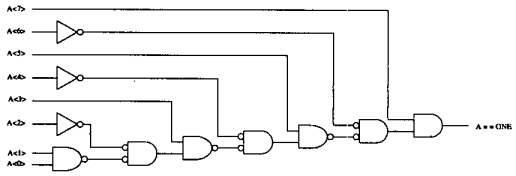

Figure 6: Prior zero/one comparator (b)

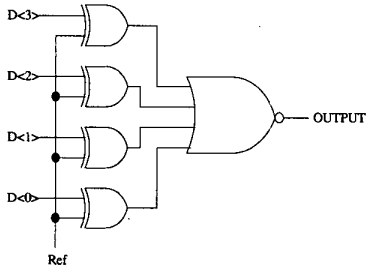

Figure 7: Prior zero/one comparator (c)

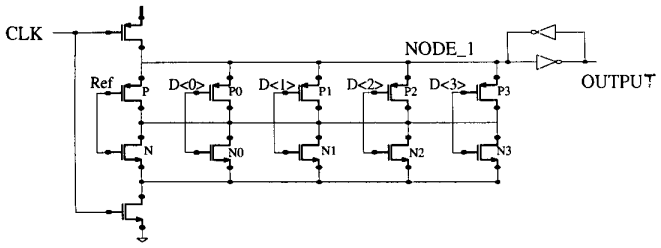

Figure 8: Proposed zero/one comparator

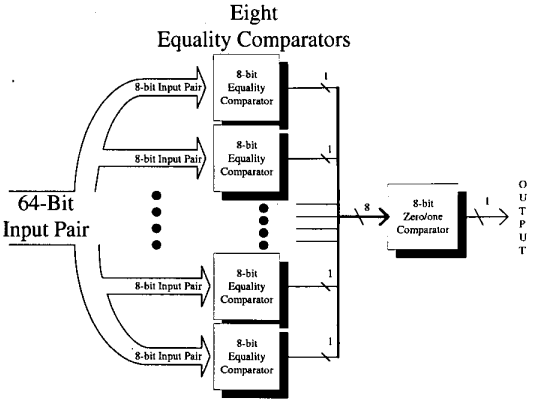

Figure 9: 64-bit comparator architecture

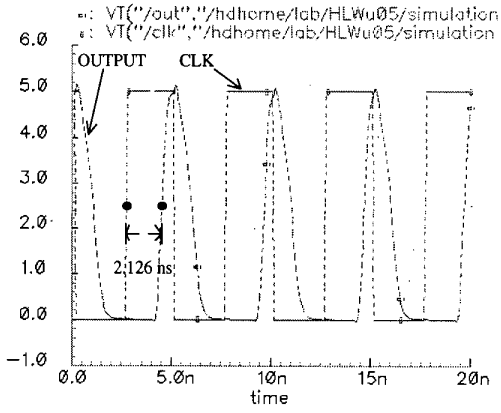

Figure 10: Simulation waveform

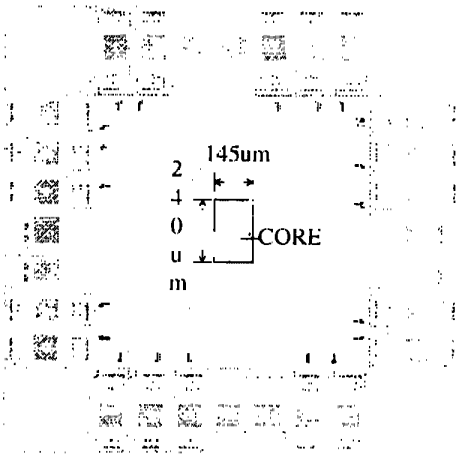

Figure 11: Chip layout