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Design of An Inter-Plane Circuit for Clocked PLAs *

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Abstract

The Programmable Logic Arrays (PLAs) have become popular devices in realization of both combinational and sequential circuits. We present a power-saving fast half-swing CMOS circuit implementation for NOR-NOR PLA implementation. An additional 1/2 VDD voltage source and buffering transmission gates are inserted between the NOR planes to erase the racing problem and shorten the rise delay as well as the fall delay of the output response such that the speed is enhanced and the dynamic power is reduced.

1 Introduction

Prior works to improve PLA circuits are mainly focused on speed and power by using many alternatives, e.g., erasing ground switch, NAND gate buffering, or reducing static current, [3], [2], [4]. An important fact which has been long ignored is that one of the largest state transition in a PLA is the switching of the load between the first plane and the second plane. Owing the large wire load induced on this inter-plane connection, many syndromes will occur in different design style for the PLAs. All of the problems result from the same reason. That is, the slow state transition at the output of the first plane and the inter-plane wire load. We introduce a novel design composed of an extra $\frac{1}{2}$ VDD source with a PMOS transistor, a transmission gate, and a NMOS transistor to resolve the aforementioned difficulty.

2 Half Swing FastPLA Design

2.1 General prior PLA circuits

Referring to Fig. 1, which is a general architecture of prior PLAs, the slow response at the output of the first plane is the major reason why the entire PLA either operates slowly or functions incorrectly. Prior works regarding the speed enhancement and power-saving, [1], [2], [3], [4], are all focused on using different gates between the two planes. Hopefully, the state transition of the inter-plane wire load can be fastened. Nevertheless, all of the mentioned improved circuits unavoidably will introduce the full swing charging time or discharging time.

2.2 Half-swing inter-plane circuit

A simple thought to reduce the state transition time at the inter-plane wire load is to precharge the output of the first plane to be $\frac{1}{2}$ VDD in the precharge (or pre-discharge) duration. Thus, technically speaking, we can approximately reduce the subsequent rise delay or fall delay in the evaluation duration to one half of the original delay. As shown in Fig. 2, an extra $\frac{1}{2}$ VDD power source is introduced accompanied with two cascaded inverters (i.e., the delay buffer) and one transmission gate. The entire operation of the proposed circuit is described as follows.

A. When $clk = 0$, node s, t, p and q, are respectively charged to VDD, GND, VDD, and $\frac{1}{2}$ VDD. Note that the voltage at node q is kept at $\frac{1}{2}$ VDD in the precharge duration is owing to the OFF state of the transmission gate, N1 and P1. The transmission gate composed of N1 and P1 is controlled by $\overline{clk}$. Hence, in the precharge (or pre-discharge) phase, the transmission is OFF such that p and q are isolated.

B. When clk turns high, the N-block-1 proceeds its own evaluation process while the N1-P1 transmission gate is turned ON. Regardless what the outcome is at the output of the first plane, the voltage at node q is either pulled up from $\frac{1}{2}$ VDD to full VDD or pulled down from $\frac{1}{2}$ VDD to GND. Obviously, the delay of the output response of the first plane will much much

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faster than any full swing dynamic logic.

C. Although the speed enhancement by the proposed half-swing circuit is achieved, another power dissipation problem must be resolved at the same time. Note that if the proposed cirucit is applied to a design style of which the second plane does not have a clock-controlled transistor, e.g., pseudo-NMOS logic, the precharged voltage at node q might result in a DC path in the second plane composed of the P3 and the N-block-2. Hence, we need to add a clock-controlled NMOS between N-block-2 and GND such that the DC current path will not be created in the precharge duration.

D. A simple observation of the proposed inter-plane half-swing circuit is that if INV1 and INV 2 are usual inverters, the circuit still functions properly However, if the evaluation result of N-block-1 is "stop," the voltage of s, t, and p stay the same, and q is pulled up to a full VDD. The response time is much faster than that of a pull down operation for q. The reason is owing to that if the evaluation result of N-block-1 is "pass," then s must be pulled down, t is pulled up, and p is pulled down. Then q will be pulled down. This simple fact reveals that the pull down of the output of the first plane is a longer process. In order to fix this problem, the sizes of INV1 and INV2 should be adjusted. A proposed size ratio is that INV1 possesses a large pull-up PMOS and a small pull-down NMOS, while INV2, on the contrary, has a small pull-up PMOS and a large pull-down NMOS, as shown in Fig. 3.

3 Simulation and Analysis

Speed (Delay) Simulations : In order to verify the proposed low-power high-speed PLA configuration, we conduct a series of different PLAs' simulations to compare with other PLA designs as shown in Fig. 4. Table 1 shows the speed performance of different PLAs at the output of the first plane. Our proposed inter-plane half-swing circuit indeed speed up the response time for all of prior PLA design approaches. Then, we need to compare the delay of the response at the output of the second plane. Note that the second plane should provide a full swing output. Hence, the delay is measured from the 50% of the input voltage to the 50% of the output voltage. Besides, the dynamic NOR-NOR and the Dhong's PLA requires a delayed clock. After several simulations, the minimal delay of such a clock is 22 ns. We, thus, add such a delayedclock in the following simulation and the speed performance of the second plane is given in Table 2.

If there is no delayed clock for dynamic NOR-NOR and Dhong's PLA, their respective simulation results are given in Table 3. The original dynamic NOR-NOR and Dhong's PLA will provide incorrect outputs, but our circuit will not. Notably, Dhong's design is a normally low operation which is different from the other designs. During the precharge period, the output of Dhong's is low. Thus, the critical delay of Dhong's design is the rising edge delay instead of the falling edge delay.

Power Dissipation Simulations : As for the power consumption comparison, we also conduct a series of simulations which employ Monte Carlo method of HSPICE. The number of sweeps is 1000, and the signal frequency is 2.50 MHz (clock period = 400 ns). The power dissipation results are tabulated in Table 4. The proposed inter-plane half-swing circuit produces less power consumption regardless what type of PLAs. These results correspond to what we expect regarding dynamic power consumption when n increases.

4 Conclusion

The proposed inter-plane half-swing circuit configuration, using one transmission gate and an extra $\frac{1}{2}$ VDD source between the product line and output line instead of a buffer or an inverter, can eliminate the ground switch, increase the response speed, and reduce power consumption. It also keeps the inputs of the second plane at a "stop status" before the evaluation phase to prevent the racing problem and the usage of delayed clocks.

References

[1] M. Afghahi, "A robust single phase clocking for low power, high-speed VLSI applications," *IEEE J. of Solid-State Circuits,* vol. 31, no. 2, pp. 247-253, Feb. 1996.

[2] G. M. Blair, "PLA design for single-clock CMOS," *IEEE J. Solid-State Circuits,* vol. 27, no. 8, Aug. 1992.

[3] Y. B. Dhong, and C. P. Tsang, "High speed CMOS POS PLA using predischarged OR array and charge sharing AND array," *IEEE Trans. on Circuits & Systems -II: Analog and Digital Signal Processing,* vol. 39, no. 8, pp. 557-564, Aug. 1992.

[4] C.-C. Wang, C.-F. Wu, R.-T. Hwang, and C.-H. Kao, "A low-power and high-speed dynmaic PLA circuit configuration for single-clock CMOS," *1997 National Computer Symposium (NCS'97),* vol. 2, pp. C-57 - C-62, Dec. 1997.

Name	Pseudo-N	NOR-NOR	Domino	Dhong's
Original	140.3	28.0	25.0	28.0
Ours	97.0	8.0	13.0	8.0

Table 1 : The average delay of the first plane output of different PLA designs. (N2 does not exist in this series of simluations; unit = ns)

	Delay (ns)	$V_{out,max}$
Pseudo-N	82.4	5.0
Pseudo-N + ours	51.1	5.0
NOR-NOR	45.4	5.0
NOR-NOR+ours	25.1	4.93
Domino	28.0	5.0
Domino+ours	16.0	4.14
Dhong's	30.0	2.50
Dhong's+ours	8.0	2.44

Table 2 : The average delay of the second plane output of different PLA designs.

	Delay (ns)	$V_{out,max}$
NOR-NOR	23.4	3.93
NOR-NOR+ours	25.1	4.93
Dhong's	10.0	1.79
Dhong's+ours	8.0	2.44

Table 3 : The average delay of the second plane output of different PLA designs without delayed clock.

	Power (μW)	Delay (ns)	$V_{out,max}$
Pseudo-N	0.5511	82.4	5.0
Pseudo-N+ours	0.4628	46.0	5.0
Domino	0.2088	28.0	5.0
Domino+ours	0.1762	22.0	4.7
NOR-NOR	0.2603	45.4	5.0
NOR-NOR+ours	0.1557	25.1	4.93
Dhong's	0.1732	30.0	2.50
Dhong's'+ours	0.1406	8.0	2.44

Table 4 : The power dissipation of different PLA designs. (N2 is added in this series of simulation.)

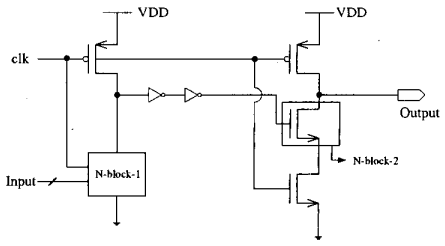


Fig. 1: Prior NOR-NOR PLA

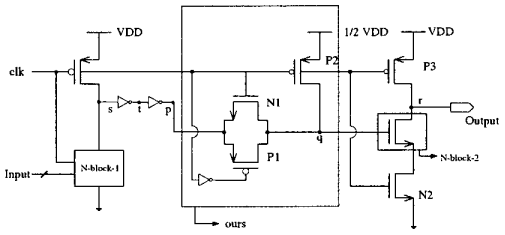


Fig. 2: Inter-plane half-swing circuit.

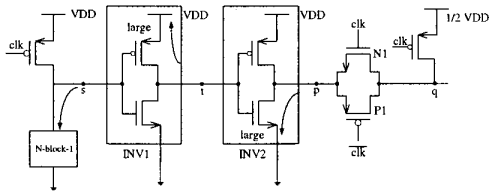
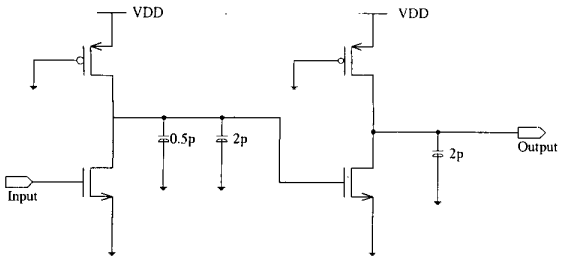
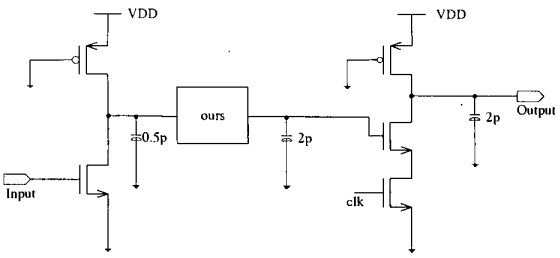


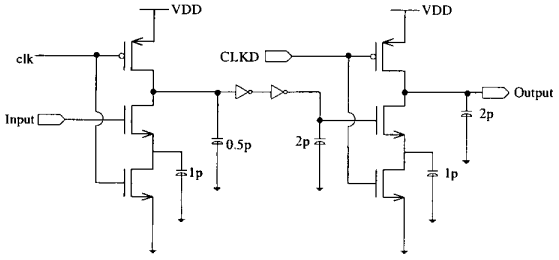
Fig. 3: Detailed schematic of the proposed circuit.



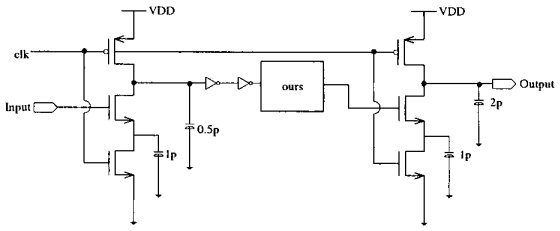
pseudo-N PLA



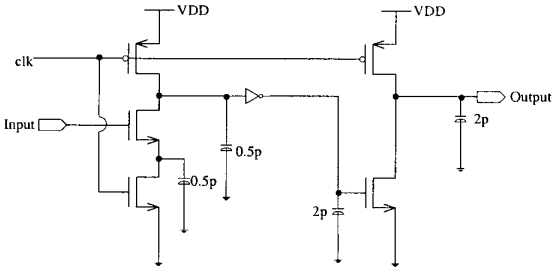
pseudo-N + ours PLA



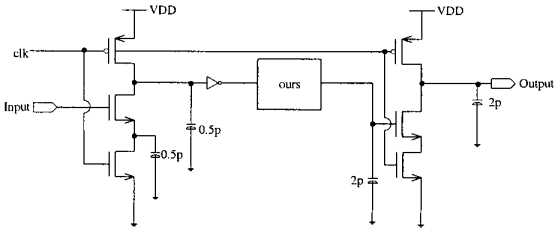
Dynamic NOR-NOR PLA



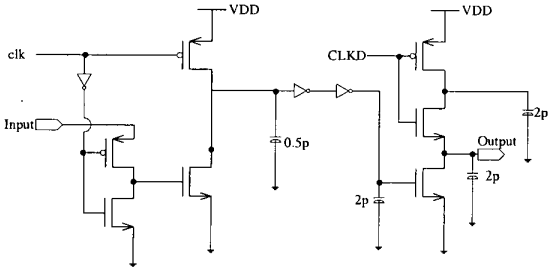
Dynamic NOR-NOR + ours PLA



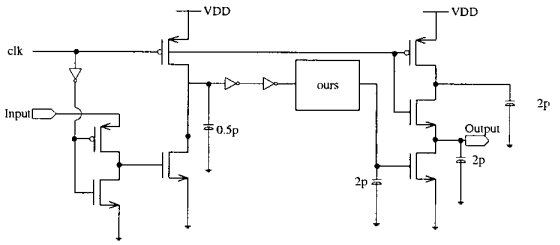
Domino PLA



Domino + ours PLA



Dhong's PLA



Dhong's + ours PLA

Fig. 4: Different PLAs for Comparison