DESIGN OF SINGLE-ENDED SRAM WITH HIGH TEST COVERAGE AND SHORT TEST TIME

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ABSTRACT

The advantages of low power dissipation and smaller chip area for single-ended SRAM are well known. In this paper we present the configuration and the test strategy of a single-ended six-transistor SRAM. The benefits of short test time, no retention test and high test coverage are verified. The goal of high quality control and short test time of full CMOS SRAM test can be achieved.

1. INTRODUCTION

Considering the requirements of low power consumption in standby mode, simple circuit design and process knowledge, and large noise immunity, the most commonly used ASIC memories is the six-transistor, cross-coupled-inverter SRAM. One of the major problems in SRAM test is to obtain full fault coverage. As SRAM density becoming larger and advanced circuit designs creating more complicated failure modes, the testing time will increase rapidly. Hence, the SRAM test cost occupies a significantly large portion of the total production cost. For the future SRAM generations, the test cost is expected to rise even higher. Therefore, SRAM testing is becoming a challenging task in terms of quality and economics [1].

Because of two I/O sides in the SRAM cell, the structure of two-ended SRAM creates lots of extra work during testing. When there is a defect at one end of the SRAM, the function of the other end can still compensate it. Hence a lot of fault models have been used to detect such a fault, e.g., the Suck-At-Fault (SAF), the Transition-Fault (TF), State-Coupling-Fault (SCF) and data retention fault. From the failure analysis results of [2], those SCF and TF are mainly caused by the two-ended structure of the six-transistor SRAM.

IDDQ test is one of the effective techniques of detecting both bridge faults and open faults in CMOS integrated circuits. Bridge faults of metal bridge, gate oxide leakage, junction leakage, parasitic transistor leakage and open faults of metal broken, blind contact to source-drain and blind via, etc., which are produced during the fabrication process, can be easily found. The open defects can be modelled by some stuck-at faults in combinational circuits. In contrast, the bridge defects cannot be modelled by stuck-at faults. Note that a defective circuit can still pass the function testing and create risks in the later field applications when the testing scheme depends on the resistance of the bridge faults [3][4]. In such cases, the IDDQ test can detect the bridge faults, stuck-on faults and break faults such as line break, Gate break, Drain break and Source break.

There have been attempts to use IDDQ test method for detecting manufacturing process defects in SRAMs. Sachdev reported [1] that his design for SRAM IDDQ testing may not cover stuck-open faults in the matrix. Moreover, since address decoders are not exhaustively toggled, multiple access faults may not be triggered for IDDQ testing. Furthermore, data retention faults may not be covered by IDDQ measurement. Thus a combination of address decoder BIST, IDDQ and functional tests are necessary to achieve high quality and low cost SRAM test.

2. CIRCUIT DESIGN AND TESTABILITY

2.1 Single bit line SRAM cell

Fig. 1 shows a single-ended five-transistor static CMOS cell which can replace the basic six transistor full CMOS cell such that a smaller array size is needed. The five-transistor CMOS cell contains one less device and one less bit line per cell than the common six-transistor cell.
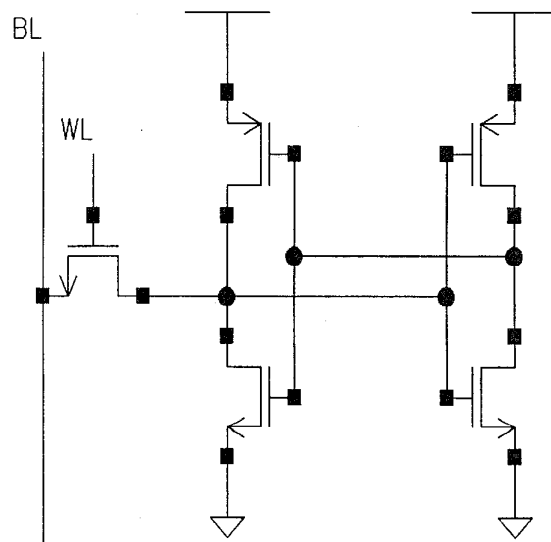

Fig. 1 Single-ended 5-transistor SRAM

It has not been widely used because of lower operating margins and difficulty in performing the WRITE operation reliably with standard power supply. Restated, there is no problem with writing a '0', while writing a '1' is difficult since data transferring from the write bit line to the flipflop is a ratio- .

type operation. The series of the write access gate and the column-enable gate has a weak transmission capability for data '1'. This makes the WRITE operation unreliable unless the word line voltage is increased above the VDD power supply. Owing to the ratio problem, the dimensions of the transistors have to be carefully designed to ensure the WRITE operation. In case it is used for the high density designs, sophisticated control of peripheral units is required to ensure the reliability of the WRITE operation of the cell. The additional circuitry for the control might increase the chip area thereby reducing the area-saving advantage given by such a memory cell design.[5]

We, therefore, propose a novel design as shown in Fig. 2. By adding a NMOS transistor WCT (write control transistor) in the latch as shown in Fig. 2 and this transistor is controlled by the WRITE_. Then the problem in executing WRITE operation will be resolved, because in the writing period the big pull-down transistor of the latch no longer exists. It becomes just like one inverter connected to a small PMOS feedback. However, because the input side of the cell is connected through a pass NMOS transistor, the high voltage can not reach full Vdd. Hence, the threshold voltage of the first inverter has to be lower than 1/2 Vdd by adjusting the W/L ratios of the transistors. Besides, noise margins then will be kept.
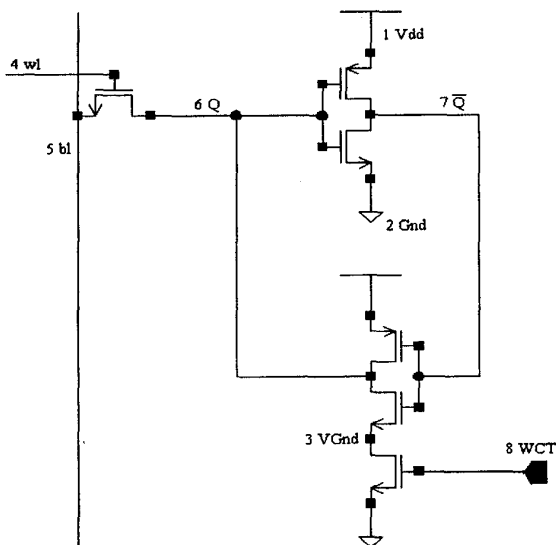

Fig. 2 Proposed single-ended 6-transistor SRAM

To avoid disturbing the unselected cells during the WRITE operation, the WCTs are only opened for the columns of the selected word when the WRITE is high and the CLK is low. As for the unselected columns, the WCTs are closed to maintain the latch function. To optimize the speed, one might set the threshold voltage of the inverter, which is used as the sense amplifier, above 1/2 VDD by adjusting the W/L ratios of the transistors. Fig. 3 is the entire schematic diagram of the proposed SRAM structure.
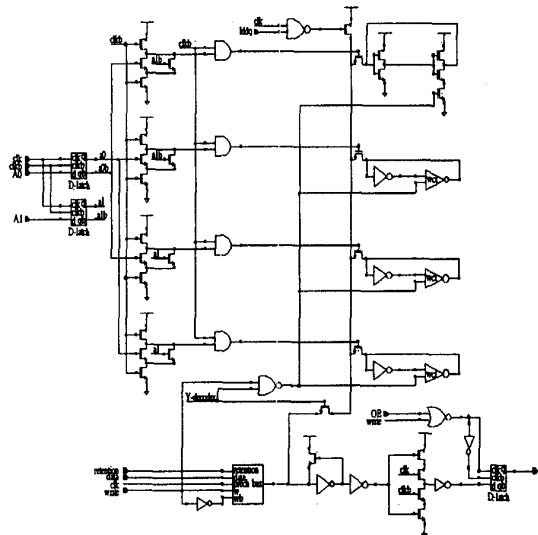

Fig.3 Entire schematic diagram of the proposed SRAM

2.2 Test strategy

The traditional IFA-9 scheme is shown in the following,[2]

{⇕(w0); ⇑(r0,w1); ⇑(r1,w0); ⇓(r0,w1); ⇓(r1,w0); delay hundreds of ms; ⇕(r0,w1); delay hundreds of ms ; ⇕(r1)}

The proposed test scheme is shown in the following,

{decoder test,⇕(w0); IDDQ; ⇑(r0,w1); IDDQ; ⇑(r1) at predischarge.; ⇕(w, checkerboard); IDDQ; ⇕(r, checkerboard)}

Here we will discuss the proposed scheme.

1.   decoder test :   The combination of decoder test and cell test will cost a lot of effort.   In the proposed scheme, the first test is decoder test, and then the decoder can be ensured to be fault free.   Thus faults of the pass transistors are the only problem to be taken care of.

2.   ⇕(w0); IDDQ :   Depending on the resistance of the short circuit, short defect in the cell may cause SAF or IDDQ fault.   If the resistance of the defect is low enough, then the SAF will be observed.   If the resistance of the defect is high but still create measurable static current, then the IDDQ fault will be observed. The open fault at the input of the inverter will cause floating gate effect and poorly defined gate voltage, then a leakage path from Vdd to Vss can be detected.   This test is to detect the IDDQ when the cell content is zero.   During this period, the BLs are pulled up to Vdd and the content of the cell is zero.   This IDDQ test can also detect the leakage between the source/drain of the pass transistors.

3.   ⇑(r0,w1) :   This test is to detect SA1 faults.

4.   IDDQ :   This test is to detect IDDQ faults when the cell retains "1".

5.   ⇑(r1) at predischarge :   This test is to detect SA0 faults.

Besides, because of the predischarge during this period, the retention faults will be detected. Thus, **no delay time is needed for the retention fault detection**.

6. ↻(w, checkerboard), IDDQ : This test is to detect the IDDQ of SCF.

7. ↻(r, checkerboard)} : This test is to detect the SCF.

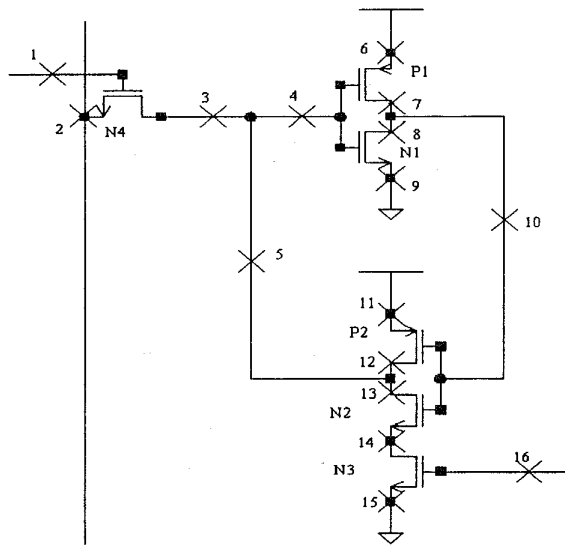The detectable defects are shown in Table 1 (short defects) and Table 2 (open defects) as in Fig. 2. and Fig. 4.

Fig. 4 Possible open faults in the proposed SRAM

3. SIMULATIONS AND EXPERIMENTS

In order to verify the proposed strategy, we conduct a series of simulations by using a TSMC 0.6 um SPDM technology. All of the faults listed in Table 1 and Table 2 are simulated by HSPICE. The open defect is simulated with a 100G Ohm resistance. It is verified that when any resistive path (5000 Ohm) exists except the short between the source/drain of the WCT can be either IDDQ or SAF detectable. The open fault at the input of the inverter will cause floating gate effect, but it's not so easy to simulate the leakage current caused by open faults. However, the open faults can be detectable by the function tests. For the retention fail caused by the open defect on the pull up transistor, because of the single-ended structure, one of the retention failure will be changed to SAF and the second retention

defect can be detectable when the predischarge of BL is used during this test period. According to the simulated results, we can either find the fault by observing the current changes from several nA of a fault free circuit to the level of mA at the presence of test vectors or find the function failed. This current difference or the function fail can be easily identified by ATE. Some of the simulation waveforms are listed in Fig. 5.

Regarding the short between the source and drain of the WCT, the purpose of WCT is to aid the "WRITE one" operation. If the WCT is stuck on, dependent on the ration the transistors, the "WRITE one" operation will be degraded at high frequency and stuck at zero. As the open at the gate of the WCT, dependent on the state of the float gate, it may cause SAF or the operation frequency will be degraded and the fault can be detected at high frequency. If the operation speed is not a major concern, by reducing the size of the pull down transistor, WCT can be eliminated. Then all of the defects can be detectable easily by the proposed scheme.

According to the results of the HSPICE simulation, our test scheme makes the test of the single-ended SARM easily implemented to detect bridge, open and retention faults.

4. CONCLUSION

A pure digital single-ended SRAM structure and its test scheme are proposed. The benefits of short test time, no retention test, and high test coverage of the proposed design are verified. The goal of high quality control and short test time of full CMOS SRAM test can be achieved.

5. REFERENCE

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[4] A. D. Singh, H. Rasheed and W. W. Weber, IDDQ Testing of CMOS Opens : An Experimental Study, *International Test Conference Proceedings*, 1995, pp. 479-489.

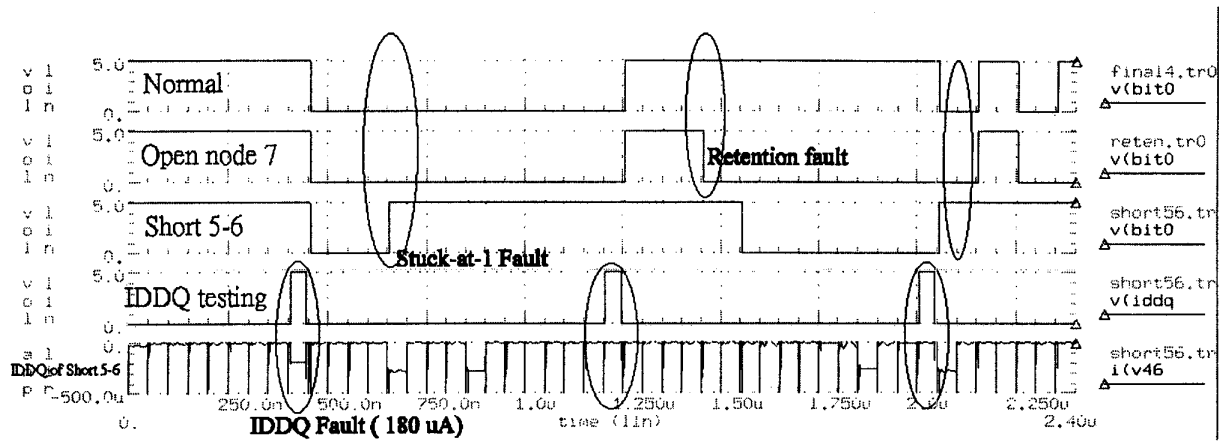[5] Betty Prince, SEMICONDUCTOR MEMORIES, John Wiley Published.

Fig. 5 Simulation waveforms of IDDQ faults and Stuck-at faults.

Short nodes	1-2	1-3	1-4	1-5	1-6	1-7	1-8	2-3	2-4	2-5	2-6	2-7	2-8	3-4
Stuck-at Fault				Yes					Yes	Yes			Yes	Yes
IDDQ and/or SA Fault	IDDQ	Yes	Yes		Yes	Yes	Degr	Degr			Yes	Yes		
Short nodes	3-5	3-6	3-7	3-8	4-5	4-6	4-7	4-8	5-6	5-7	5-8	6-7	6-8	7-8
Stuck-at Fault	Yes			Yes										
IDDQ and/or SA Fault		Yes	Yes		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table. 1 Possible short defects existing in Fig. 2

Open node	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Stuck-at Fault		Yes	Yes		Yes	Yes	Yes	Yes	Yes		Yes	Yes	Yes	Yes	Yes	Degr
IDDQ and/or SA Fault	Yes			Yes						Yes						

Table. 2 Possible open defects existing in Fig. 4