Hardware Realization of Multi-Valued Exponential Bidirectional Associative Memory Using Current-Mode Circuits *

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***Abstract*— Though the multi-valued exponential bidirectional associative memory (MV-eBAM) was verified to possess high capacity by thorough simulations, it still remains an open problem whether the hardware realization of such an architecture is feasible. In this work, we adopt current-mode VLSI circuits to implement the MV-eBAM. The key reason is the chip area will be drastically scaled down in contrast to the voltage-mode approach. Besides, the arithmetic operations needed to be realized include the absolute value and the exponential function, in addition to currnt copiers and current adders. 4-valued logic is realized in this work. Simulation results of recalling a stored 4-valued pattern pair by feeding an associated key vector are successful. Simulations also show the recall is still correct even if there are error digits in the retrieval pattern vector. This verifies the fault tolerance ability of MV-eBAM.**

1. Introduction

Since the *bidirectional associative memory* (BAM) was proposed, many researchers have invested efforts on exploring the network's properties and limitations. Due to its intrinsic architecture, the capacity of BAM is unfortunately poor. It is notable that the exponential Hopfield associative memory is motivated by the MOS transistor's exponential drain current dependence on the gate voltage in the subthreshold region such that the VLSI implementation of an exponential function is feasible. Although the impressive capacity of an eBAM was found, the data representation of BAM or eBAM is still limited to be either bipolar vectors or binary vectors. We consider that the expansion of the data range, i.e., from $\{-1,+1\}^n$ to $\{1,2,\ldots,L\}^n, L \gg 1$, is also a feasible method to enlarge the capacity.

In this paper, we basically propose a modulized architecture based on the evolution equations of the MV-eBAM. A 4-valued MV-eBAM current-mode circuit will be designed and simulated. In order to hardwarely implement the MV-eBAM by current-mode circuits, many individual circuits have to be redesigned, e.g., the exponential function and the reverberation controller. Following the presentation of each circuit module, thorough simulations will be shown which verify the recall function of the MV-eBAM.

*This research was partially supported by National Science Council under grant NSC 83-0404-E-110-014.

2. Current-Mode Circuits for MV-eBAM

Before the introduction of the hardware circuits for the multi-valued eBAM (MV-eBAM), it is necessary to show how the MV-eBAM operates theoretically. Suppose we are given M pattern pairs, which are $\{(X_1,Y_1),(X_2,Y_2),...,(X_M,Y_M)\}$, where $X_i = (x_{i1},x_{i2},...,x_{in})$, $Y_i = (y_{i1},y_{i2},...,y_{ip})$, where n is assumed to be smaller than or equal to p without any loss of generality. Hence, the evolution equations of the MV-eBAM are shown as

$$\begin{aligned} y_k &= H\left(\frac{\sum_{i=1}^{M} y_{ik} b^{-\sum_{j=1}^{n}|x_{ij}-x_j|}}{\sum_{i=1}^{M} b^{-\sum_{j=1}^{n}|x_{ij}-x_j|}}\right) \\ x_k &= H\left(\frac{\sum_{i=1}^{M} x_{ik} b^{-\sum_{j=1}^{p}|y_{ij}-y_j|}}{\sum_{i=1}^{M} b^{-\sum_{j=1}^{p}|y_{ij}-y_j|}}\right) \end{aligned} \quad (1)$$

where X and Y are input key patterns, b is a positive number, called the radix, $b > 1$, x_k and x_{ik} are the kth digits of X and the X_i, respectively, y_k and y_{ik} are for Y and the Y_i, respectively, and $H(\cdot)$ is a staircase function shown as the following equation,

$$H(x) = \begin{cases} l, & (l-0.5)\times\frac{D}{L} \le x < (l+0.5)\times\frac{D}{L} \\ 1, & x < 1.5\times\frac{D}{L} \\ L, & x \ge D \end{cases} \quad (2)$$

where $l = 1,2,\ldots,L$, L is the number of finite levels, and D is the finite interval of the staircase function. The reason why the staircase function is used is the argument

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in $H(\cdot)$ in Eqn.(2) is supposed to be assigned to the nearest integer. The capacity of the MV-eBAM can be shown to be very close to the maximum number of combinations of the input vector, i.e. $M_{\max} \approx L^n$ when b is large enough. Hence, the MV-eBAM indeed possesses a high capacity.

2.1 Functional Modules of MV-eBAM

Considering the compatibility with the binary digital system and the practical usage, we choose $L = 4$ in the implementation of the MV-eBAM. Thus, each component of the stored patterns is denoted by two bits in the memory plane. Our chip is dedicated to store and retrieve 8-digit data where each digit is in $\{0, 1, 2, 3\}$. Since the memory planes contains only binary bits, we need two interfaces to convert between the binary voltage data and the quaternary current data, i.e., the 2-to-4 encoder and the 4-to-2 decoder.

After the binary data of the stored pattern and the retrieval pattern have been transformed into quaternary current data by the encoders, these currents are fed into the recall function block as shown in Fig. 1. Note that though the recall function block in Fig. 1 is used for the $X \rightarrow Y$ recall process, it can be used in the $Y \rightarrow X$ recall process. The modules employed in the recall function block is based on the evolution functions in Eqn.(1). According to Eqn.1), the current-mode circuits required in the function block include absolute value of subtraction circuits (ASC), current adders (CA), approximately exponential decay function circuit (EDC), current multipliers and current dividers. Each module will be introduced in the following text.

absolute value of subtraction circuits (ASC) : The term, $\mid x_{ij} - x_i \mid$, is the first function we have to resolve in the evolution functions. The x_{ij} and x_i are from the output of the 2-to-4 encoder. We design the following circuit to achieve such a ASC, as shown in Fig. 2. The current copier is a current mirror to duplicate the x_{ij} and x_i respectively. Then, the current subtractors produce $x_{ij} - x_i$ and $x_i - x_{ij}$ which will be selected by the maximum circuit. The reason that we have to prepare two sets of current copiers and subtractors is we don't know which current will be larger beforehand. Hence, we have to consider both possibilities and use the maximum circuit to generate the absolute value of the difference of these two currents.

current adders : Current adders are needed to complete the function, $\sum_{j=1}^{n} \mid x_{ij} - x_j \mid$, in the evolution functions.

exponential decay function circuit (EDC) : The exponential function is the core of MV-eBAM which improves the signal-to-noise ratio in the recall processes. The traditional implementation of such an exponential function is either utilizing the I-V curve of the diode or the subthreshold region of a MOS transistor. They both are essentially a voltage-to-current transform which is hard to be coped in a pure current-mode circuit design. A better option is the current-to-current exponential function which is easier to be integrated in the current-mode approach. Hence, an approximately exponential decay function circuit is adopted as shown in Fig. 3. The characteristic curve operates from the cutoff region to the linear region for a MOS transistor.

current multipliers : Referring to Eqn.(1), the term, $y_{ik} \cdot b^{-\sum_{j=1}^{n} |x_{ij} - x_j|}$, implies the necessity of current multipliers because $y_{ik} \in \{0, 1, 2, 3\}$. We have to double or triple the amount of certain currents before sum them up accordingly. y_{ik0} and y_{ik1} are the bits of y_{ik}. These two bits are used to be the gate voltage to determine how many times of current $b^{-\sum_{j=1}^{n} |x_{ij} - x_j|}$ will be produced and delivered to the next stage. As for the copy of $b^{-\sum_{j=1}^{n} |x_{ij} - x_j|}$ at the righthanded end of the circuit will be used to generate the denominator of the argument of $H(\cdot)$ in the evolution functions.

current quantizers : After all of the single currents are summed respectively for the nominator and the denominator for the argument of $H(\cdot)$ in the evolution functions by current adders, a current quantizer is required to determine what the integer ratio is between the nominator and the denominator. That is, a current quantizer is basically to generate an integer value. In Fig. 4, a current quantizer integrated with a CMOS logic circuit is shown. For instance, if $\sum y_{ik} \cdot b^{-\sum_{j=1}^{n} |x_{ij} - x_j|}$ is two times of $\sum b^{-\sum_{j=1}^{n} |x_{ij} - x_j|}$, then we will find that

1). $I > I_1$, then I_A is negative and logically 0;

2). $I > I_2$, then I_B is negative and logically 0;

3). $I < I_3$, then I_C is positive and logically 1.

Then, $A = 0, B = 0, C = 1$ are fed into the CMOS logic circuit to produce a pair of bits 10 indicating the integer 2.

2.2 Architecture of MV-eBAM

Our work is dedicated to the 8-digit 4-valued system. Nevertheless, the pattern vectors have to be stored in a binary memory. Hence, 16 bits are required for 8 4-valued digits. The entire MV-eBAM is demonstrated in the diagram in Fig. 5, including the memory planes which store the data pattern pairs and the functional modules for the exponential function recall process.

phase controller : Since the recall of such a network is composed of two stages, $X \rightarrow Y$ and $Y \rightarrow X$, data flow

control units are required in order to save some area. Otherwise, simply double the area of one phase might cause too much overhead. However, because the eBAM is a bidirectional recall process, there are 4 phases basically in a single recall,

$$X \rightarrow Y, \Rightarrow Y \rightarrow X', \Rightarrow X' \rightarrow Y', \Rightarrow Y' \rightarrow X"$$

Most of the cases, if there is a correct recall, the associated pattern pair would be retrieved in these four steps. That is, $Y' = Y$ and $X' = X"$. Hence, we design **clock frequency dividers** in order to adjust the appropriate timing of the recall procedure. The phase controller is composed of a ripple counter and 3 D flip-flops. The PRESET of the ripple counter is connected to READ. When READ is low, phase 1 then will be asserted high. Phase 2 won't be asserted until the first positive edge after the READ. The number of the cells in the counter depends on the dimension of the stored pattern. Usually, we empirically make the duration of each phase long enough to complete the task.

The signals, phase 1, 2, 3, 4, generated from the phase controller are used to control transmission gates, 1, 2, 3, 4, respectively, as shown in Fig. 6, such that the correct phase of each recall will be executed in the evolution function block. If a stop signal is fed from checkers, then transmission gate 0 will be on and the pattern pair will then be placed at the output bus.

checkers : Four regristers are utilized to store vectors, X, X', Y, Y'. The function of the checker block is to examine whether there is a match between X and X', which is only activated during Phase 2 and 4. In contrast, another checker will be employed to check Y and Y' in Phase 1 and 3. If a pattern pair is found, then the stop signal will be delivered and the output will be latched properly.

3. Simulation Analysis

In order to verify the correctness and the performance of the current-mode implementation of the MV-eBAM design, we integrate all of the modules which are arranged as shown in Fig. 5. Without any loss of robustness, we store 4 pairs of 4-valued 8-digit pattern vectors, $(X_1, Y_1), \ldots (X_4, Y_4)$, in the MV-eBAM, which are shown in the following Table 1.

Pattern Pair	X	Y
Pair 1	00 01 01 10 11 10 01 01	01 01 10 11 10 01 01 00
Pair 2	01 11 10 01 00 01 10 11	11 10 01 00 01 10 11 01
Pair 3	10 00 00 11 01 11 00 10	10 00 11 01 11 00 00 10
Pair 4	11 10 11 00 10 00 11 00	00 11 00 10 00 11 10 11

Table 1 : The stored pattern pairs

We, thus, choose the X vector of the first pair trying to recall its associated Y vector and then proceed a few simulations :

correct X :
That is, the input retrieval vector X = (00 01 01 10 11 10 01 01). Referring to Fig. 7, it shows all of the waveforms of the 16 output lines of Y vector. The stable Y vector is (01 01 10 11 10 01 01 00), which is correctly recalled. The duration for the output to be stablized is $500 - 410 = 90$ ns.

X with 3 error digits :
That is, the input retrieval vector X = (10 11 11 10 11 10 01 01). The Manhattan distance between the wrong X and X_1 is 3 in this case. Referring to Fig. 8, it shows all of the waveforms of the 16 output lines of Y vector. It takes 135 ns to reach the stabilized correct recall.

X with 2 error digits :
That is, the input retrieval vector X = (01 00 01 10 11 10 01 01). Note that the Manhattan distance between the wrong X and X_1 is 4 in this case because the first two digits of the retrieval pattern are two unit distance away from the first two digits of X_1, respectively. It takes 2 phases to reach the stabilized correct recall. In the first phase, the output is Y = (01 01 10 01 10 01 01 10) which is Manhattan distance 3 away from Y_1. 240 ns is needed to be stabilized. While in the second phase, the X' = (00 01 01 10 11 10 01 01) = X_1 is stabilized after 120 ns.

4. Conclusion

The MV-eBAM has been theoretically proved to be a high capacity associative memory which is worth of hardware implementation. This paper presents a current-mode circuit implementation of such a network. Besides the verification of the eBAM theory, other practical problems have been encountered and resolved, e.g. the current mode exponential function, multi-valued encoder and decoder. The current-mode scheme is proved to be a feasible approach to realize such a complicated neural network.

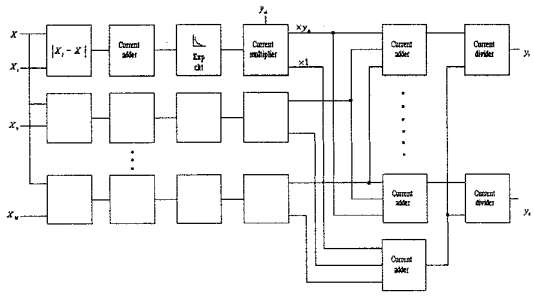

Fig. 1 ： Recall function block

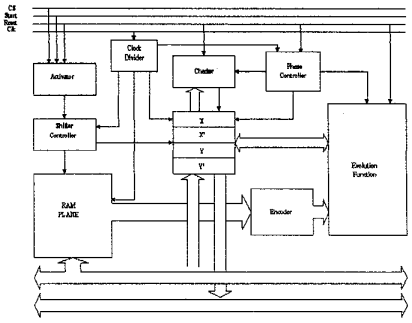

Fig. 5 ： Architecture of MV-eBAM

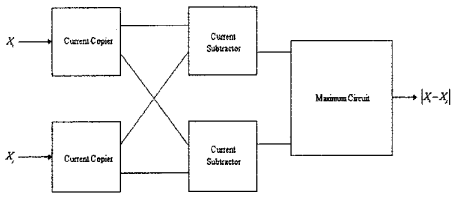

Fig. 2 ： absolute value of substraction ckts

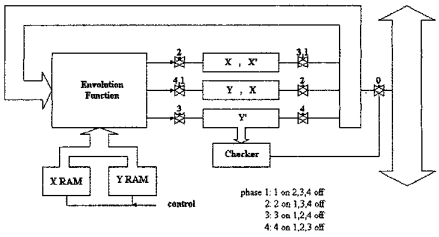

Fig. 6 ： phase controller

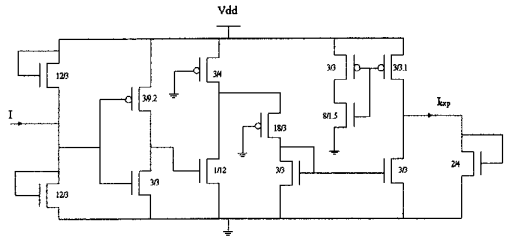

Fig. 3 ： approximately exponential decay function ckt

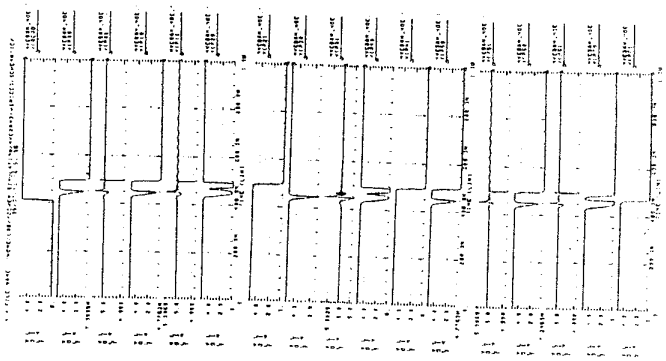

Fig. 7 ： simulation result of MV-eBAM for correct X

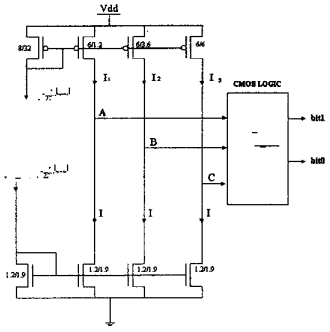

Fig 4 ： current quantizer

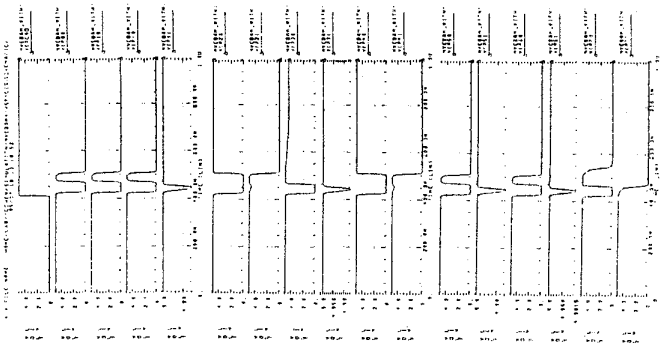

Fig. 8 ： simulation result from X with 3 error digits