Analysis and Current-Mode Implementation of Asymptotically Stable Exponential Bidirectional Associative Memory *

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***Abstract*— The asymptotical stability of exponential birdirectional associative memory (eBAM) has been proved basing on the systematic stability of the exponential correlation associative memory (ECAM). Although the eBAM has also been proved to possess high capacity, the hardware realization still remains an issue mainly due to the implementation of the necessary exponential function. Considering the practical problems, we employ the current-mode implementation using the exponential I-V characteristic of the diode circuit to realize the eBAM. The proposed architecture for the implementation turns out to be a scalable, regular, and dense design.**

I. Introduction

Chiueh and Goodman [1] proposed an exponential Hopfield associative memory motivated by the MOS transistor's exponential drain current dependence on the gate voltage in the subthreshold region such that the VLSI implementation of an exponential function is feasible. Chiueh also proposed an exponential correlation associative memory (ECAM) which is an autocorrelator utilizing the mentioned exponential function of VLSI circuits to enlarge the correlation between stored pattern pairs. However, the complete design of the network is remained unclear. Besides, some practical problems in the implementation are unsolved, i.e., the non-ideal exponential function of the subthreshold region. Based upon the concept of Chiueh's exponential Hopfield associative memory, Jeng *et al.* proposed one kind of exponential BAM [3]. However, the energy function proposed in [3] can not guarantee that every stored pattern pair will have a local minimum on the energy surface. Moreover, there is no capacity analysis given in [3].

Although we have estimated the impressive capacity of an eBAM [5], it becomes very interesting to explore the possibility of the hardware realization of such a neural network. Many factors have to be taken into consideration. Though the neural networks implemented with MOS operating in the subthreshold region have the advantages of low power and compatibility with VLSI circuits, [2], the dimension of the pattern vector is limited due to the fixed dynamic range of the VLSI exponential circuits operating in the subthreshold region pointed out by Chiueh [2], and Mead [4]. The non-linear and non-ideal the exponential function given by the MOS circuit might result in incorrect recall of stored data. In order to reduce these undesirable factors, the exponential I-V characteristic curve of an diode is utilized to implement the eBAM. Current-mode (CM) circuits are used in current adder, current comparator, bias circuits, current mirrors, etc.

II. Theory of Exponential BAM

Before proceeding the hardware implementation of the eBAM, we have to restate the framework of the eBAM neural network as a background knowledge [5].

A. Evolution Equations

Suppose we are given M bipolar pattern pairs, which are $\{(X_1, Y_1), (X_2, Y_2), ..., (X_M, Y_M)\}$, where $X_i = (x_{i1}, x_{i2}, ..., x_{in})$, $Y_i = (y_{i1}, y_{i2}, ..., y_{ip})$, $X_i \neq X_j$, $i \neq j$, and $Y_i \neq Y_j$, $i \neq j$. We use the following evolution equations in the recall process of the eBAM :

$$y_k = \begin{cases} 1, & \text{if } \sum_{i=1}^{M} y_{ik} b^{X_i \cdot X} \geq 0 \\ -1, & \text{if } \sum_{i=1}^{M} y_{ik} b^{X_i \cdot X} < 0 \end{cases}$$

$$x_k = \begin{cases} 1, & \text{if } \sum_{i=1}^{M} x_{ik} b^{Y_i \cdot Y} \geq 0 \\ -1, & \text{if } \sum_{i=1}^{M} x_{ik} b^{Y_i \cdot Y} < 0 \end{cases} \quad (1)$$

where b is a positive number, $b > 1$, "$\cdot$" represents the inner product operator, x_k and x_{ik} are the kth bits of X and the X_i, respectively, and y_k and y_{ik} are for Y and the Y_i, respectively. The reasons for using an exponential scheme are to enlarge the attraction radius of every stored pattern pair and to augment the desired pattern in the recall reverberation process.

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We adopt the SNR approach to compute the capacity of the exponential BAM [5], $SNR_{eBAM} = \frac{2^{n-1}b^4}{2(M-1)(1+b^{-4})^{n-1}}$ where n is assumed to the $\min(n,p)$ without any loss of generality.

Chiueh [2], and Mead [4] pointed out that a transistor operating in the subthreshold region working as an exponentiation circuit has a dynamic range of approximate 10^5 to 10^7. In the realization of eBAM by VLSI circuit, hence, the dimension, n, and the amount of stored pattern pairs, M, must also be limited.

III. Current-Mode Circuits Using Diode Exponential Scheme

The implementation of the eBAM is roughly divided into two parts, the digital storage unit and clocking control unit, and the analog current-mode units. The former is dedicated to the pattern vectors storage cells and recall reverberation process control. The latter is focused on the realization of the exponenatial function.

A. *Architechture of the Recall Phases*

For the sake of clearness, we illustrate the operation of the eBAM by discussing the $X \rightarrow Y$ phase only. As shown in Fig. 1, $X_1, \ldots X_4$, are stored patterns, and X is the retrieval pattern. The XNOR generates the match or the mismatch signal of x_i and x_{ji} for $i = 1, \ldots, n$. Then the Encoder and the Decoder units compute the number of matched bits and the mismatched bits. The result was presented to the V_{gen} unit, which is an D/A converter with a refernece voltage source.

Reference Voltage Source

Referring to Fig. 2, transistors, M03, M04, M05, M06, are used to produce different resistances in order to generate necessary V_{ref} at M02. Note that M03 - M06 are self-biased NMOS transistors.

Diode Exponenatial Circuit

As shown in Fig. 3, when the gate and the drain of a NMOS transistor are short-circuited, the junction of gate to source is a diode junction. The transistor then is in the saturation region. Therefore, there is an exponential function between the V and I.

$$I = A_d I_s \left\{ \exp(\frac{qV}{kmt}) - 1 \right\} \qquad (2)$$

where

A_d : area of the diode, I_s :the unit saturation current

q : electronic charge, k : Boltzmann's constant

t : temperature, m : a constant $\in$ [1,2]

The I-V characteristic curve is shown in Fig. 4. Directly using the input voltage to achieve the exponential function required by the eBAM is not a feasible method due to the very small amount of current when the input voltage is small. We propose a **voltage mapping** approach which will be discussed more detailedly in Section B.1.

Current Adder

The addition of the current plays an important role of the recall processs. In short, we use I_+ to denote the positive current, and I_- for the negative current. I_{sum+} is the summation of the total positive current, while I_{sum-} is for the total negative current. Note that we exclude the operational amplifier (OP AMP) from the current addition design. The reason is the OP AMP will consume too much area and power.

Referring to Fig. 5, the current mirror technique is employed to achieve the addition of the current. If the size of the transistors are the same, the transistors will operate in the saturation region and the input current will be the same as the output current. The y_i controls the flow of the I_{sum+} and the I_{sum-}. If y_i is high, then I_i is added to the I_{sum+}; else to the I_{sum-}.

Current Comparator

The current adders provide us two currents, I_{sum+} and I_{sum-}. If $I_{sum+} > I_{sum-}$, then the output bit should be $+1$ according to the evolution equations of the eBAM, vice versa. Therefore, a current comparator is needed to decide which is larger and generate the output digital voltage. Fig. 6 shows the current comparator and its characteristic I-V curve.

B. *Practical Implementation Problems*

Since the exponential function provided by the diode scheme, Eqn.(2), or the subthreshold region scheme [1], [2], can not really provide an exactly correct and precise exponential function, $\exp(\cdot), b = e$, as needed in Eqn.(1), some current compensation design is necessary in order to produce the correct result. Hence, two practical problems must be taken care of, i.e., the bias current and the voltage mapping.

B.1. Voltage mapping

Obviously, we can not directly utilize the input voltage to the diode as the radix of the eBAM. Besides, V_{in} must be less than the breakdown voltage of the MOS diode. Hence, when a large radix is needed to operate the recall, scaling down the radix basing upon the dimension of the pattern vector and the working range of the diode. This is called **voltage mapping**. After we use SPICE to simulate the diode, we find that the input voltage must be larger than 2.5 V and the currrent must be large than

10 nA to make the diode function properly. Hence, the minimum voltage for voltage mapping should be 2.5 V.

On the other hand, the area of the rerference voltage sources will be too large to be pratically used when the desired voltage is larger than 3.8 V. Thus, we set the maximum voltage of the voltage mapping is 3.8 V. In summary, the range of the voltage mapping is $[2.5, 3.8]$.

Assume the eBAM is designed for dimension $n = 8$ pattern vectors. Then the exponent of the evolution equations, e.g., $X \cot X_i$, can be one of the following nine integers, $-8, -6, -4, -2, 0, +2, +4, +6, +8$. However, the negative integers only generate very small amount of current, which is negligible compared to the current caused by the positive integers. Therefore, we divide the region suitable for voltage mapping into 6 parts, which are $+8, +6, +4, +2, 0$ and negtive intergers, instead of 9 parts. Under these conditions, the reference voltages are $3.6, 3.35, 3.1, 2.85, 2.6, 2.5$ V, respectively.

B.2. Bias Current Elimination

Although the voltage mapping has resolved the radix representation problem in the implementation of the eBAM, another factor which is very likely to result in incorrect recall of pattern pairs is the **bias current** caused by the non-linearity of the exponential circuitry. Hence, we adopt the current compensation approach. For example, if there is a non-negative current added to I_{sum+}, then a current generated by 2.45 V applied to the diode, i.e., the bias current, is added to the I_{sum-} such that the bias current part will be crossed out in the current comparator. The same techniqe is also applied to the case the other way around. The compensation design is shown in Fig. 7.

C. Data Flow Control

Since the recall of such a network is composed of two phases, $X \rightarrow Y$ and $Y \rightarrow X$, data flow control units are required in order to save some area. Otherwise, simply double the area of one phase might cause two much overhead. However, because the eBAM is a bidirectional recall process, there are 4 phase basically in a single recall.

C.1. Phase control

Referring to Fig. 8, 4 regristers are utilized to store vectors, X, X', Y, Y'. The function of the checker block is to examine whether there is a match between X and X', which is only activated during Phase 1 and 3. If a pattern pair is found, then the stop signal will be delivered and the output will be lateched properly. As for the phase control, we design **clock frequency dividers** in order to adjust the speed of the recall procedure. The phasic clockers are composed of ripple counters. The number of the cells in the counters depends on the dimention of the stored pattern. Usually, we empirically make the duration of each phase long enough to complete the task.

C.2. Bus communication

As shown in Fig. 9, the entire chip of the eBAM is arranged to consume the least number of pins such that the area is optimally small. The chip layout is shown in Fig. 10.

IV. Simulation Analysis

After thorough simluations by SPICE, the total power consumption of the chip is approximately 15 mW. The time elapse of the recall of a pattern in $X \rightarrow Y$ or $Y \rightarrow X$ phase is 150 ns, which consists of 100 ns in digital units and 50 ns in analog units. The chip area is 880×1280 μm.

V. Conclusion

The eBAM has been theoretically proved to be a high capacity associative memory which is worth of hardware implementation. This paper presents a hybrid implementation of such a network. Besides the verification of the eBAM theory, other practical problems have been discovered and resolved. The MOS diode scheme is proved to be a good approach to generate the exponential function needed by the eBAM, which is more reliable than the exponential function provided in the subthreshold region.

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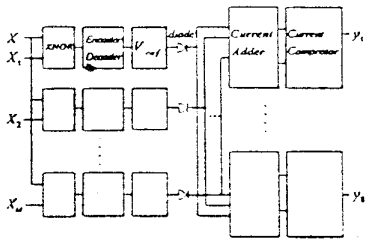


Fig. 1 Architecture of eBAM design

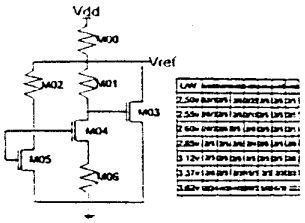


Fig. 2 Reference voltage source

Fig. 3 Diode exponential circuit

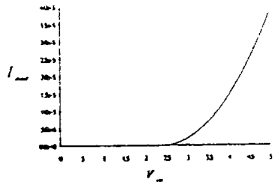


Fig. 4 I-V curve of diode exponential circuit

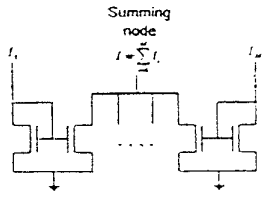


Fig. 5 Current adder

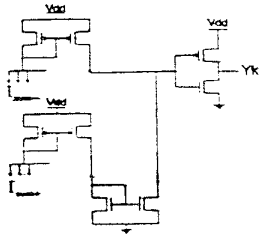
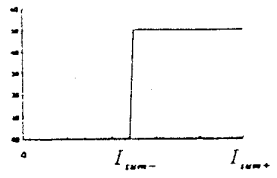


Fig. 6 (a) Current comparator



(b) I-V curve of current comparator

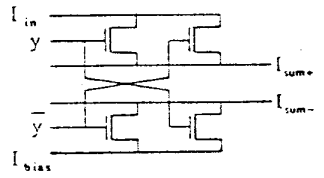


Fig. 7 Bias current compensation circuit

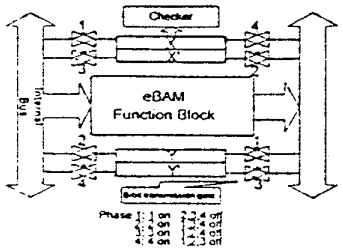


Fig. 8 Phase control circuit

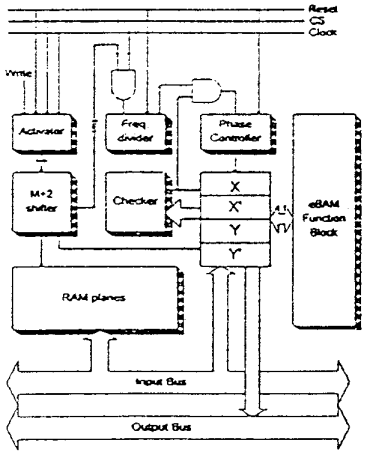


Fig. 9 Floor plan of entire design

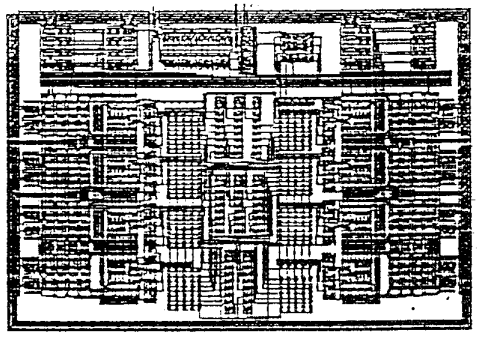


Fig. 10 Chip layout