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A single-chip PFM-controlled LED driver with 0.5% illuminance variation

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ABSTRACT

A high-efficiency LED driver with the pulse frequency modulation (PFM) control method to generate nearly consistent illuminance is demonstrated in this investigation. The illuminance consistency is achieved by sensing the feedback voltage and the temperature to modulate the on time of power devices such that automatic illuminance regulation is carried out. The recommended LED driver using the PFM control method is featured with an up-and-coming illuminance equalizer. Thus, it does not need any compensation circuit. Utilizing a 0.5-μm High Voltage CMOS process, the prototype has successfully fabricated, occupying 3.2 mm^2 of chip area. The measurement outcomes of the chip demonstrate that the current error remains within 1% when the LED output current set at 20 mA. Moreover, the variation in illuminance is exceptionally low, measuring a mere 0.5%. Furthermore, the efficiency reaches 91% verified by the measurement results.

1. Introduction

Since the 1990s, LED has been advancing at an astonishing rate. Compared to traditional light bulbs, which are prone to burnout and significant heat loss, LEDs provide attributes including low energy usage, compact volume, and durability. LEDs are a great light source that adheres to current trends and can help lower energy usage and heat waste. LEDs are now often made up of semiconductors utilizing the advantage of the combination of electrons and holes. Driven by metaverse issues in recent years, penetrating augmented reality glasses (AR glasses) have also become another highly anticipated incubation hotbed for LED technology usage. The display specifications of AR glasses focus on small area, high resolution, high luminous efficiency, full color, and wafer integration. A favorable LED system, however, requires high conversion efficiency and high LED luminous efficiency, e.g., [1–8]. As illustrated in Fig. 1 the forward current is linearly proportional to the LED illuminance [8]. Additionally, the brightness of the LED is proportionate to its current. As depicted in Fig. 1, a 5 mA current difference results in the not acceptable illuminance variation which is up to 30~40 Lux, which is considered not acceptable for instruments of biomedical usage. Apparently, the illuminance is extremely responsive to the forward current of LED. In other words, a stable current source is necessary for an effective LED driver design to generate a constant brightness.

Fig. 2 shows a measurement result where the temperature variations have a significant impact on the LED's I_d-V_d curve [9]. The curve will shift to the left when the temperature (T_{High}) is higher than the original temperature (T), and vice versa. Hence, the fluctuation in temperature (T) leads to a corresponding fluctuation in voltage (V_d). Moreover, the driving current (I_d) remains unchanged. This phenomenon causes a fact that the temperature of the LED rises as the working time increases. Moreover, the high temperature will affect the illuminance. Besides, the unstable illuminance still happens, even though supplying a high precision current is specially aimed for the design of the LED driver.

LED driver design is a field that is always evolving, with researchers working towards the goal of achieving higher performance, lower size, and wider applicability. Recent works are examined to highlight major trends and promising methodologies in areas such as current accuracy, efficiency, and power factor.

A significant emphasis is placed on striking a balance between the current accuracy and efficiency, which frequently present competing demands. Over the course of several studies, novel approaches to addressing this difficulty have been proposed. An explanation of a SAR control method is provided [10], whereas an offset calibration is implemented [11]. Over a broad spectrum of operations, both reach a high level of accuracy (with an error rate of less than 5%). Adaptive timing difference compensation is another idea that is presented [12],

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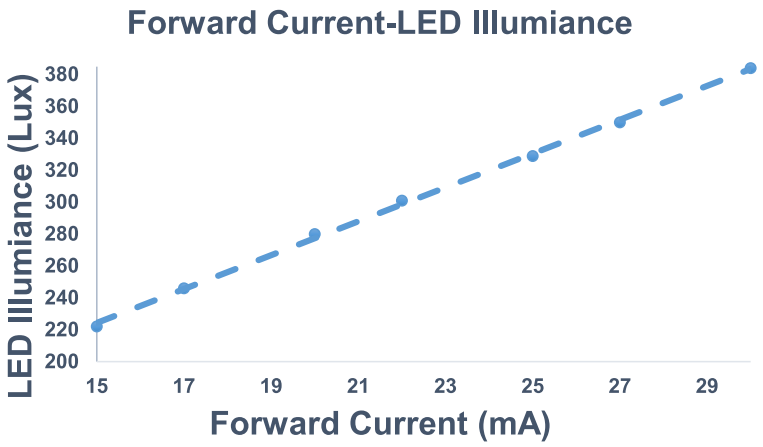

Fig. 1. Forward Current vs LED Illuminance Curve [8].

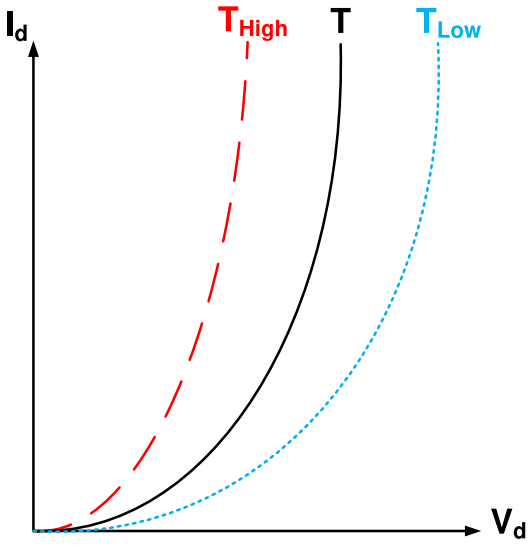

Fig. 2. I_d-V_d curve of LED at various temperatures [9].

while feedforward synchronous current control was discussed [13]. The use of these technologies demonstrates the possibility of simultaneously obtaining great levels of accuracy and efficiency.

Another important field of LED drivers is the study of high efficiency. There are a few designs that have an emphasis on maintaining an efficiency that is greater than 90%. This is accomplished, in some cases, by utilizing cutting-edge components such as GaN FETs [14] or by utilizing synchronous rectification techniques [12]. On the other hand, these designs frequently need compromises among many other aspects, like the precision of the current or the size of the components.

The process of miniaturization is essential for applications that are portable and have limited space. Adaptive delay compensation methods are proposed for these approaches [14,15]. These methods allow for good current accuracy even with small inductors, which ultimately results in designs with a lower profile. A substantial step forward for situations in which size is a major restriction is represented by this development.

In addition, several drivers can support extensive input voltage ranges (for example, 5-100V), which makes them useful for a wide variety of applications. It is possible to maintain constant performance across the whole range with the assistance of techniques such as feedforward control [13] and adaptive delay compensation [14]. These LED drivers have a wider range of potential applications because of their adaptability.

Certain reports address specialized functionality such as dimming [12, 16], multi-channel control [16–18], and automotive applications [19, 20]. These functionalities go beyond the core performance measures that are typically discussed. These designs illustrate how LED driver technology may be effectively adapted to meet a wide range of illumination requirements.

In this investigation, an LED driver is proposed that leverages a pulse frequency modulation (PFM) control method to achieve exceptionally consistent illuminance. A unique feature is its built-in illuminance equalizer, eliminating the need for separate compensation circuits, leading to simpler design and potentially lower cost. This results in high efficiency of 91%, while maintaining a low current error of only 1% at 20-mA LED output current. Additionally, the driver boasts an impressive illuminance variation of just 0.5%, demonstrating excellent consistency in light output. This feature is highly appreciated in many light sensitive medical detectors. Furthermore, its compact size, achieved through a 0.5-μm High Voltage CMOS process, occupies a mere 3.2 mm^2 chip area, making it suitable for area-constrained applications.

To attain the LED (BLL-BBZZDD33VV44VV-MM3366) illuminance stability, the recommended LED driver takes advantage of an Illuminance Equalizer to sense temperature with Temperature Detector and the pulse frequency modulation (PFM) control method to auto-adjust the output current for stabilizing illuminance in time.

2. Consistent illuminance with high-efficiency LED driver

The proposed PFM-controlled LED driver's block diagram is depicted in Fig. 3. The proposed system consists of a PFM Control Circuit, an Illumination Equalizer, LED string, High Level Shifter, Temperature Detector, power PMOS, Clock Generator, Zero Current Detector (ZCD), power NMOS, and Delay Cell String. Our novel contributions include the proposed Illumination Equalizer, Zero Current Detector (ZCD), and Delay Cell String. The operating principle of this system is outlined as follows:

- Using the Temperature Detector, the temperature of the LED string is detected. The Temperature Detector comprises a bandgap circuit featured with PTAT, such that the temperature variations are converted into a voltage V_{rt}.
- The detected voltage V_{rt} passes through a Voltage Limiter to prevent excessive voltage from damaging the chip. The relationship between the temperature and the output voltage is confirmed by comparing the temperature detection voltage V_{rt} with the feedback voltage V_{fb} in a comparator.
- A triangular wave and a Clock Generator generate a fixed-frequency clock signal clk, which serves as the basic frequency for pulse frequency modulation (PFM) generator.

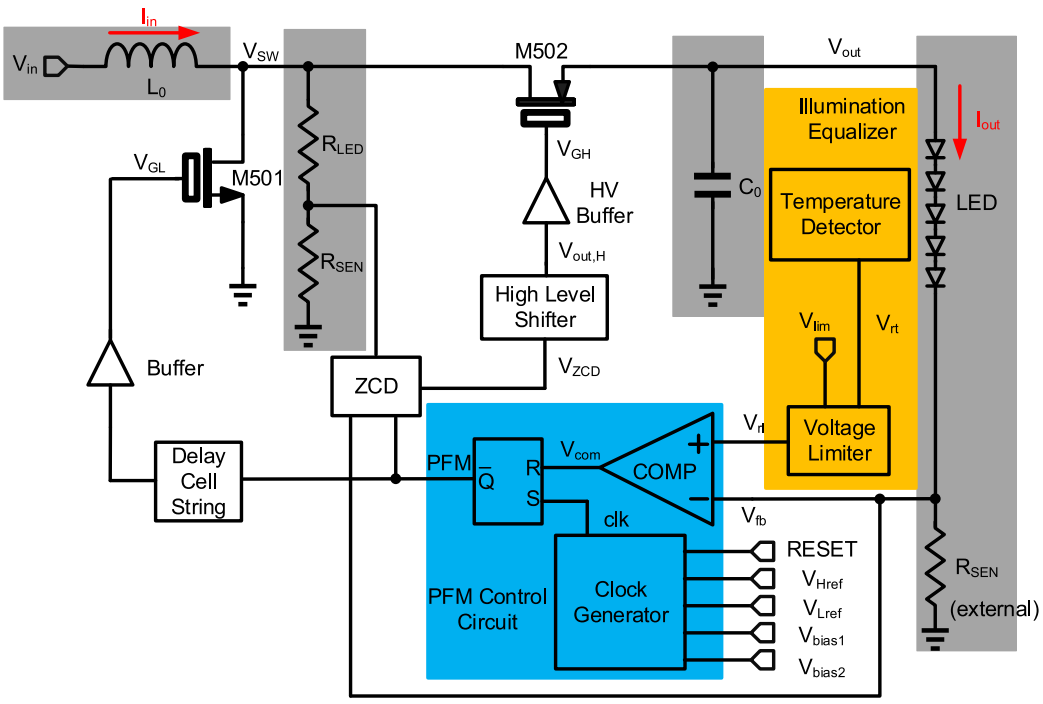

Fig. 3. Block diagram of LED driver.

- The output of the comparator is fed into an RS flip-flop along with the clk signal to generate the PFM wave.

Additionally, a zero-current detector (ZCD) prevents reverse current from P-type power transistors, reducing power consumption. A High Level Shifter increases the voltage level of the switching signal, ensuring better conduction of P-type power transistors. A Delay Cell String offsets the conduction time of P-type and N-type power transistors to avoid significant losses in conversion efficiency. The following text describes each sub-circuit in detail.

2.1. Illumination equalizer

Illumination Equalizer in Fig. 3 composed of Temperature Detector and Voltage Limiter. Temperature Detector detects the temperature of the LED string. The variation of temperature is converted into V_{rt} which is coupled to Voltage Limiter for further conversion into V_{rl}.

2.2. Voltage limiter

The schematic of the proposed Voltage Limiter is shown in Fig. 4. The current starts to increase when LEDs are turned on. Thus, the temperature of the LED will rise as well. A limiting circuit is then needed to avoid over-heating. Voltage Limiter consists of two transmission gates and a comparator. V_{rt} will be the output of Voltage Limiter if V_{rt} does not exceed the limit (V_{lim}). Otherwise, V_{lim} will be chosen as the output instead. The PFM Control Circuit's V_{fb} is coupled to the output of the voltage limiter. Function diagram of the proposed Voltage Limiter is illustrated in Fig. 5.

In this investigation, for 1 mA, 10.6 Lux is the illuminance's tuning. Referring to Fig. 3, V_{com} is used to reset the PFM output, which is governed by the following equation.

$$V_{com} = \begin{cases} 0, & \text{if } V_{fb} > V_{rt} \\ 1, & \text{if } V_{rt} > V_{fb} \end{cases} \quad (1)$$

2.3. Temperature detector

Temperature Detector senses LED string's temperature with a bandgap circuit featured with proportional to absolute temperature (PTAT), as shown in Fig. 6. Transistors M507 to M512 form a current mirror to provide the same amount of currents to two BJTs (D1 and D2). Due to the resistance R_{b1} in Fig. 6, the emitter–collector voltages of D1 and D2 are different even if $I_{D1} = I_{D2}$. The voltage difference of D1 and D2 produces a current proportional to the absolute temperature, and R_{b2} is used to convert the current into the voltage V_{rt}. Eq. (2) expresses the function of V_{rt}, where L is the ratio of R_{b2} to R_{b1}, K represents the ratio of D2 to D1, k represents Boltzmann's constant (1.38×10^{-23} J/K), q represents the charge of the electron (1.602×10^{-19} C), T represents the temperature, n represents the ideality factor of the diode. Referring to Eq. (2), a highly linear temperature-to-voltage relationship can be designed by adjusting the ratio between the two BJTs (D1 and D2) and the resistance (R_{b1} and R_{b2}) with the matched current mirrors, respectively [21].

$$V_{rt}(L,K,T) = I_{temp} \cdot L \cdot R_{b1} = \frac{nk \cdot L \cdot \ln(K)}{q} \cdot T \quad (2)$$

Typical numbers in Eq. (2) using the HV CMOS process that we utilize in this study at room temperature are as follows:

$$D2 = 10 \cdot D1,\ K = 10,$$

$$5T = 20\ ^{\circ}C = 293.15\ ^{\circ}K,$$

$$L = 8.174955,\ n = 1,\ R_{b1} = 600\ k\Omega$$

2.4. PFM control circuit

The PFM Control Circuit in Fig. 3 consisting of a comparator (COMP), a Clock Generator, and a RS latch. PFM is in charge of tuning LED illuminance. The switching power converter needs a switching signal to control on/off of the power transistor (namely, M501 and M502 in Fig. 3). The Clock Generator generates a stable square wave signal clk with a fixed frequency and sends it to "S" terminal of RS flip-flop as the highest frequency of the system. The output feedback signal V_{fb} is compared with the temperature sensed voltage V_{rl}. When V_{fb} is

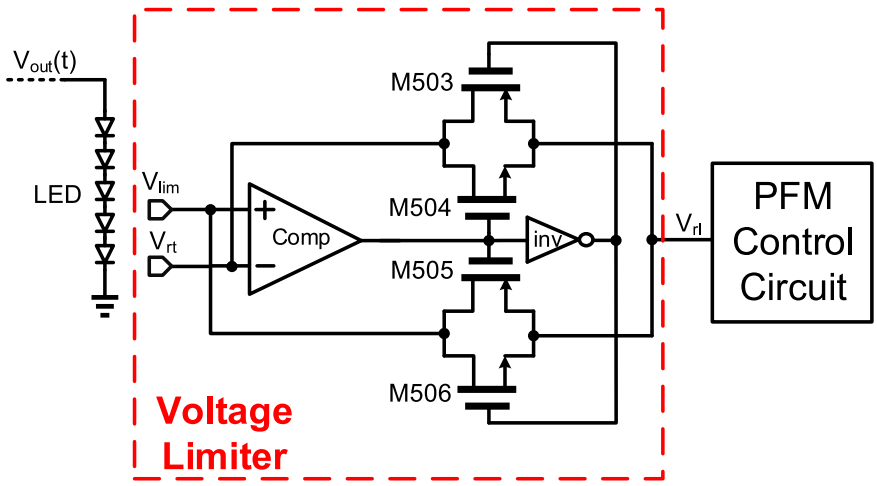

Fig. 4. Schematic of Voltage Limiter.

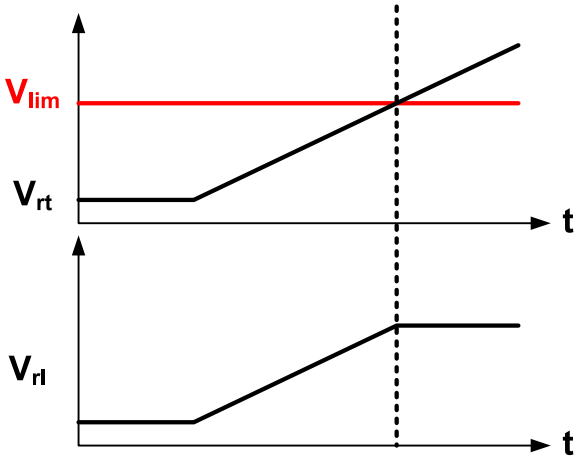

Fig. 5. Function diagram of the proposed Voltage Limiter.

higher than V_{rl}, the COMP outputs logic 0, and the RS flip-flop is reset to reduce the PFM frequency. If V_{fb} is lower than V_{rl}, the COMP outputs logic 1, and the RS flip-flop outputs the highest frequency. During off time, PFM adjusts the duty cycle. I_{in} and V_{out} shown in Fig. 3 would also be increased at a period during the increase in PFM's duty cycle and vice versa. The relational formula between I_{in}, V_{out}, and duty cycle is mentioned in Eq. (3).

$$\text{Duty cycle} = \frac{I_{in} - I_{out}}{I_{in}} = \frac{V_{out} - V_{in}}{V_{out}} \tag{3}$$

Fig. 7 shows the timing diagram of the proposed PFM Control Circuit. Referring to Eq. (4), PFM is known as a pulse signal when the on time is much less than the off time in an extreme state.

$$\begin{aligned} &\text{PFM(t)} = \delta(t) \\ &\mathcal{L}\{\text{PFM(t)}\} = 1 \end{aligned} \tag{4}$$

For all s, the Laplace Transform is said to be converged in Eq. (4). PFM is known as a unit step function in Eq. (5) when the off time is much less than the on time in the other extreme state.

$$\begin{aligned} &PFM(t) = u(t) \\ &\mathcal{L}\{PFM(t)\} = \frac{1}{s} \end{aligned} \tag{5}$$

In Eq. (5), the Laplace Transform is said to be converged when $\Re(s)>0$. This indicated that PFM(t) can be considered to be stable based on the formula mentioned above. Therefore, the proposed LED driver has the capability to maintain a consistent level of illuminance.

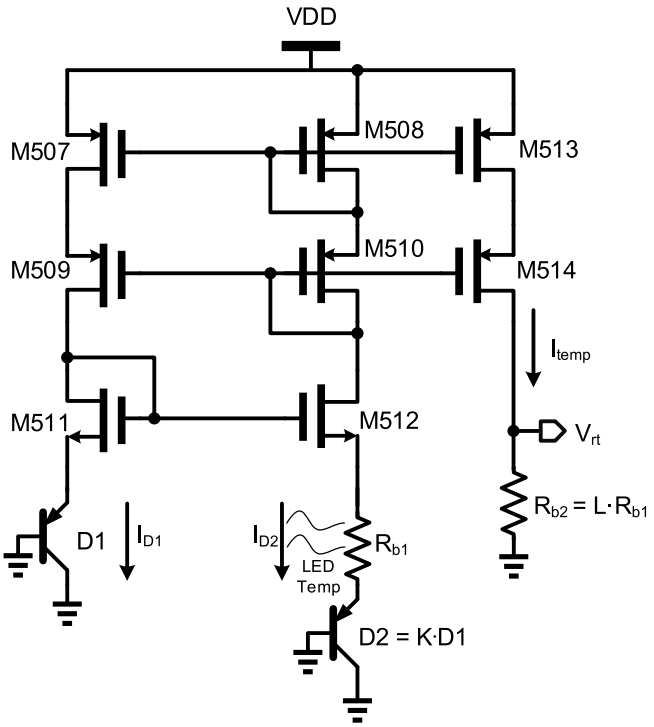

Fig. 6. Schematic of PTAT Circuit.

2.5. Clock generator

Fig. 8 shows the schematic of the Clock Generator in Fig. 3, which is used to generate a fixed frequency clock signal to provide the clock signal (clk) required by the PFM Control Circuit. The input signals, RESET, V_{Href}, V_{Lref}, V_{bias1}, and V_{bias2}, are provided externally. Thus, it works as follows:

- In the initial state, V_{ramp} is 0, clk is also 0, and transistor M516 is turned on.
- The bias current I_{b1} generated by the bias circuit flows into the capacitor (C_{ramp}) to charge it until V_{ramp} is the same as V_{Href}. Then, the Comp_H outputs logic 0 and clk becomes logic 1.

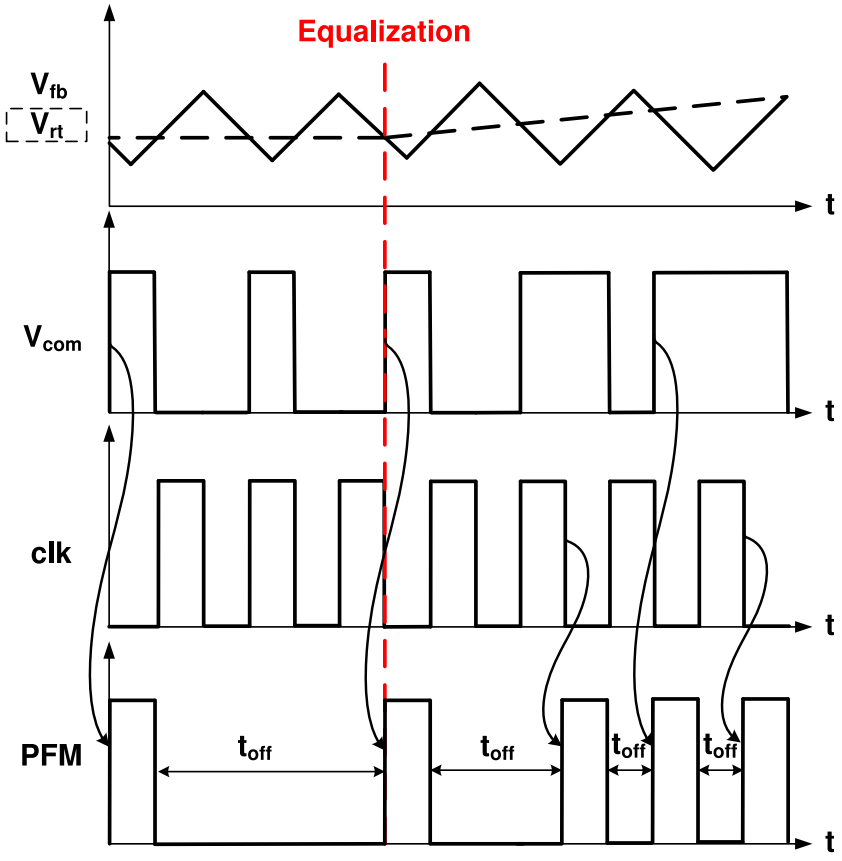

Fig. 7. Timing diagram of PFM Control Circuit.

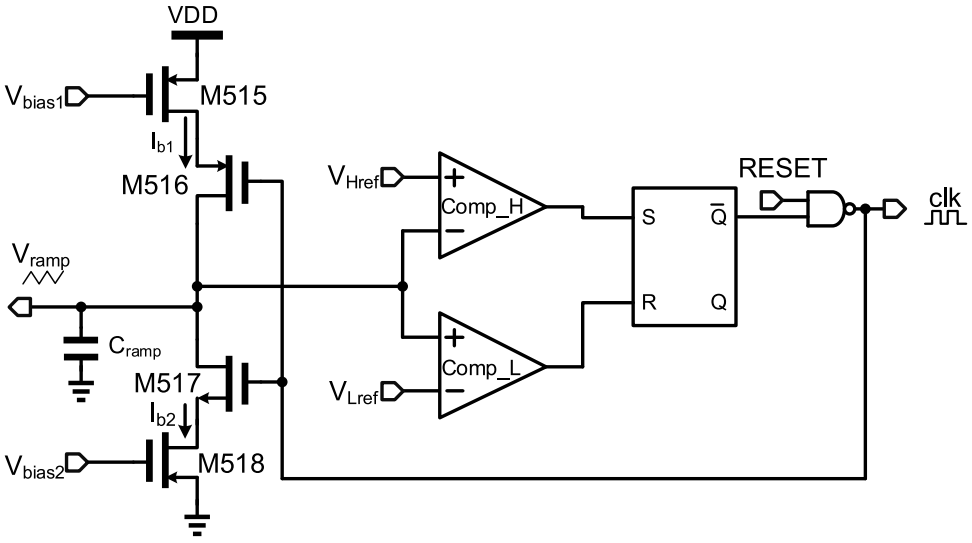

Fig. 8. Schematic of Clock Generator.

- Transistor M517 in Fig. 8 is turned on by clk, and I_{b2} discharges the capacitor C_{ramp} quickly. After the V_{ramp} drops below V_{Lref}, Comp_L outputs logic 0, and clk becomes logic 0 again.
- Repeat the above cycles to complete the generation of the fixed frequency clock signal, namely clk, as shown in Fig. 9.
- Referring to Eq. (6), the charging speed of the capacitor C_{ramp} is governed by the current I_{b1} and the discharging speed is determined by I_{b2}. Thus, the duty cycle which required by clk can be achieved by adjusting the ratio of the currents I_{b1} and I_{b2}. Fig. 9 is a timing diagram of Clock Generator.

$$\mathrm{Period}_{clk} = \frac{C_{ramp} \cdot (V_{Href} - V_{Lref})}{I_{b1}} + \frac{C_{ramp} \cdot (V_{Href} - V_{Lref})}{I_{b2}} \tag{6}$$

2.6. Zero current detector (ZCD)

Fig. 10 shows schematic of the ZCD in Fig. 3. A detection circuit is needed to protect the power PMOS from reverse bias which is one of the major causes of power loss. ZCD will cutoff power PMOS M502

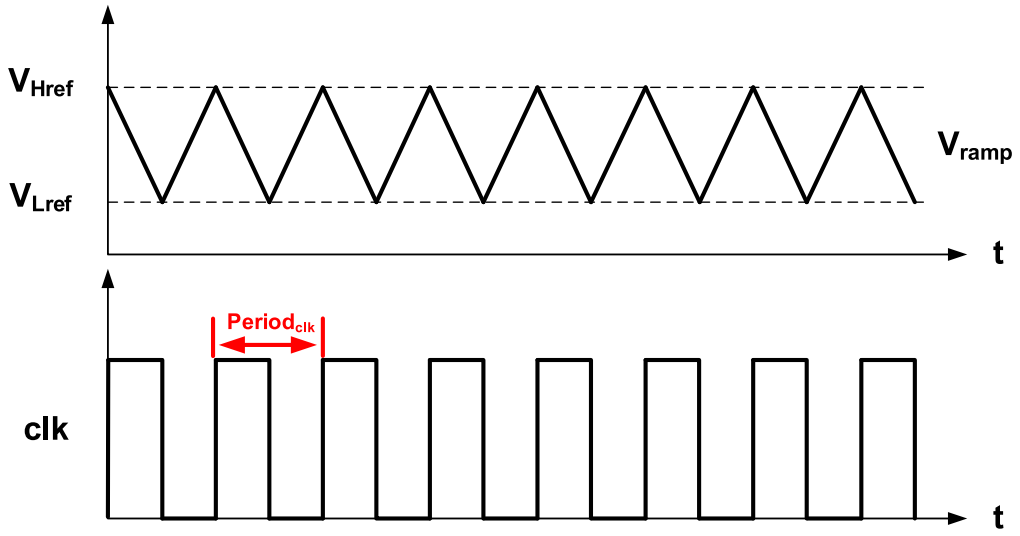

Fig. 9. Timing diagram of Clock Generator.

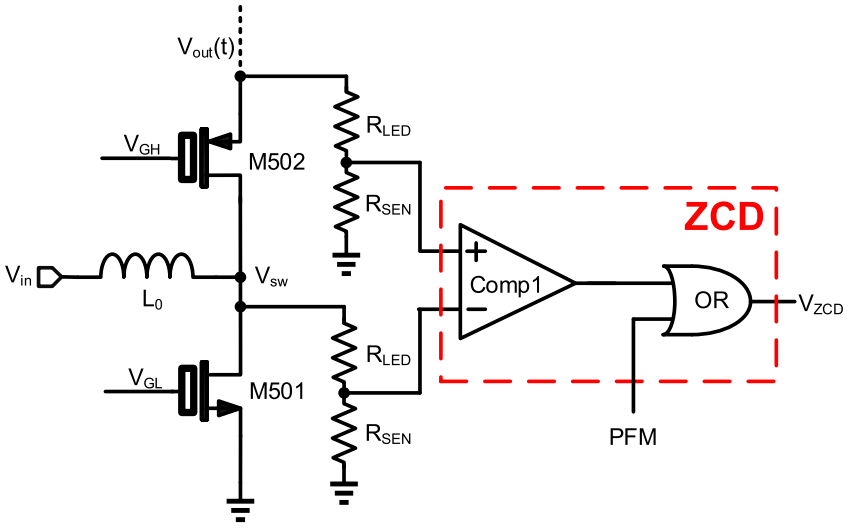

Fig. 10. Schematic of the ZCD.

when ZCD senses the reverse current from M502. Notably, R_{LED} is the equivalent resistance for the LED.

The ZCD as shown in Fig. 10 is typically used for PFM modulation and the inductor current operates in discontinuous conduction mode (DCM). If the P-type power transistor has a reverse current, it will increase power consumption and reduce conversion efficiency. Therefore, we need to detect the condition of the P-type power transistor current. When the current is zero, immediately turn off the P-type power transistor. The circuit part uses a comparator (Comp1) and an OR gate. The higher voltage $V_{out}(t)$ and V_{SW} must be divided by resistors in the same proportion to be within the working range of the comparator. If $V_{out}(t)$ is greater than V_{SW}, it means that there will be a reverse current, and the comparator output is Logic 1, turns off the P-type power transistor through the OR gate, preventing reverse current from passing through the P-type power transistor. When $V_{out}(t)$ is less than V_{SW}, the comparator output is Logic 0 such that it does not affect the signal output.

The flowchart in Fig. 11 outlines the steps involved in the ZCD operation. It starts with measuring $V_{out}(t)$, then comparing it with a reference voltage V_{SW}. If $V_{out}(t)$ is greater than V_{SW}, indicating the presence of reverse current, so that the output is set to 1 and the P-type power transistor is turned off. Otherwise, if $V_{out}(t)$ is less than or equal to V_{SW}, no action is taken, and the process ends.

2.7. High level shifter

Fig. 12 is the schematic diagram of High Level Shifter in Fig. 3. If the input signal V_{ZCD} is logic 1, M520 is turned on. The gate of the transistor M521 receives the signal logic 0 and starts to be turned on at the same time. The output signal $V_{out,H}$ will then be elevated to V_{DD_H}.

2.8. Delay cell string

Fig. 13 is the schematic diagram of Delay Cell String. The V_{Delay} is PFM delayed by N stages of buffers. It means to enhance the conversion efficiency and reduce the power consumption caused by power transistors. During the complete deactivation of Power NMOS after the activation of Power PMOS, loss in efficiency and LED driver's critical damage will occur due to the flow of large DC current towards GND. Hence, the power NMOS should be turned on faster than the power PMOS, so as to protect the LED driver from the large DC current.

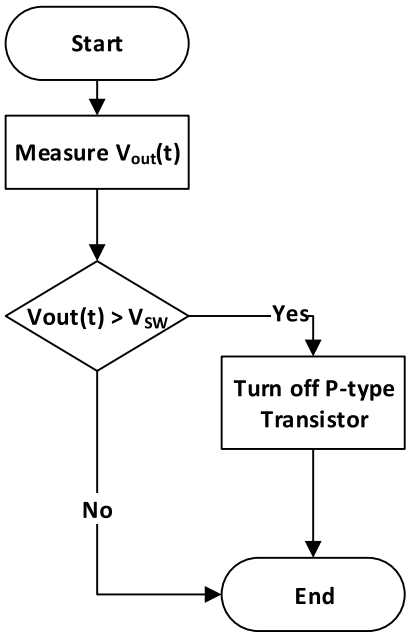

Fig. 11. Flowchart of the ZCD operation.

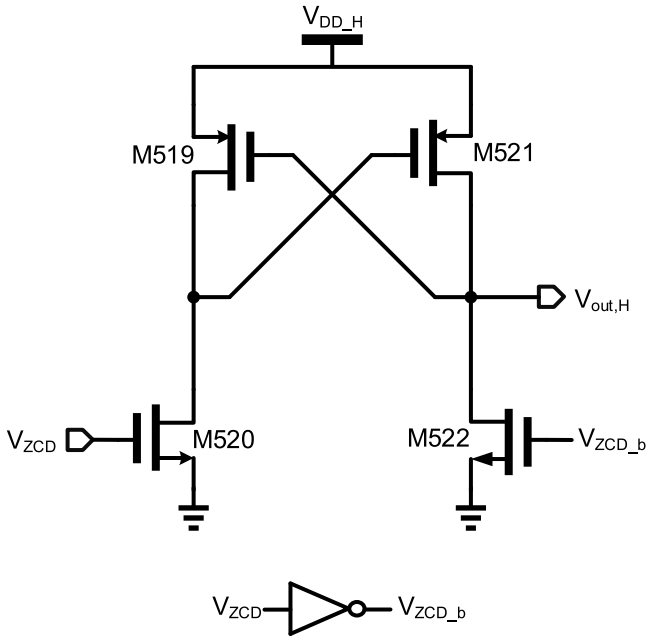

Fig. 12. Schematic of High Level Shifter.

3. Verification and measurement

3.1. System simulation

Using TSMC 0.5-μm High Voltage CMOS process, this proposed LED driver is realized. Fig. 14 shows the various-PVT-corner post-layout simulation result. The various-PVT-corner simulations are carried out at process (SS, TT, FF), voltage (VDD-10%, VDD, VDD+10%), and temperature (100 °C, 25 °C, 0 °C). The supply voltage, VDD, is 5 V.

The proposed LED driver starts without illuminance equalization in the initial state. The activation of equalization of illuminance occurs when V_{rt} senses the temperature over the limit of the LEDs. The temperature increases as the frequency of the PFM increases. The LEDs' illuminance is adjusted when the output current (I_{out}) and voltage (V_{out}) begin. Ultimately, for the equalization to be stopped (V_{out}) will be restricted. The post-layout simulation at worst case (FF, 5 V, 0 °C) is shown in Fig. 15. After the equalization, 21 mA is the expected I_{out}. I_{out} is 21.2 mA as shown by simulation results, which is 1% error from the target current.

3.2. Chip and system measurement

Fig. 16(a) and (b) show the layout and die photo of the proposed LED driver, respectively, where the core area is 1120×677.2 μm^2, and the total chip area is 2084 × 1578 μm^2.

Fig. 17 shows the chip measurement setup of the proposed LED driver. For the noise to be reduced, the chip/die is bonded on the PCB. The needed chip's voltages are provided by the Keysight 33600 Power supply. Using the Arduino and BH1750 illuminance sensor module in a dark box sense the illuminance of the LED string. For the output waveform to be observed and functionality of the circuit to be checked, we utilized the WaveRunner610Zi oscilloscope. For the reliability to be verified, 20 times of measurement per chip is implemented for 5 chips. For the LED's initial temperature to be the same as the room temperature at least 15 min should be interval between the each measurement.

The measurement results show that this chip can boost the input voltage V_{in} to a stable output voltage V_{out}, and can drive five 5-mm LEDs string. The measurement readings are summarized in Table 1, where the beginning output voltage is 9.1 V, and the beginning illuminance is 228 lux. Due to the self-heating of the chip, the temperature and sensing voltage rise continuously, respectively. Thus, it causes the output voltage rising continuously. At the 90th second, the output voltage increased to 9.2 V and started to equalize the illuminance of the LED string. Then, the output voltage is raised to the limit of 9.6 V at 420th second, and then the illuminance is fixed. This measurement result confirms that the illuminance equalizer can achieve the function of stabilizing the illuminance through the control circuit with the changing of temperature. Fig. 18 shows the waveform of the clk. The measurement result is consistent with the post-layout simulation. Thus, it can generate a clock signal with fixed frequency and duty cycle. The best performance in the measurement is at 350 kHz.

Fig. 19 shows the measurement waveform of the output signals of PFM Control Circuit. It shows that the output of comparator is 0, and the off time of PFM is reduced about 130 μs in the steady state. When the temperature rises, the comparator output is 1, the off time of PFM extends to about 2.65 μs, which is used to increase V_{out}. Therefore, the correctness of PFM Control Circuit is proved by the measurement result.

Fig. 20 shows the measurement waveforms of Power MOS control signals V_{GH} and V_{GL}. V_{GH} and V_{GL} are not interleaved so that the power transistors are not turned on at the same time. The High Level Shifter also works normally, boosting V_{GH} high potential to 11 V.

Fig. 21 shows the measurement of V_{out}. After the illuminance is stabilized, the chip generates the maximum output voltage of 9.1 V, and the biggest error is 1% compared with the prediction given by the post-layout simulation. Fig. 22 is the LED demo photo, which proves that this chip drives five 5-mm LEDs (BLL–BBZZDD33VV44VV–MM3366).

A comparison of the proposed design with various recent LED driver works is presented in Table 2. The findings demonstrate that our design outperforms all other LED driver works in terms of accuracy and Figure of Merit (FOM) from 2012 to 2022. Moreover, our LED driver showcases the smallest normalized chip area. Furthermore, Fig. 23 illustrates the technology roadmap of LED drivers.

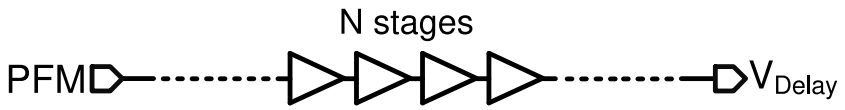

Fig. 13. Delay Cell String.

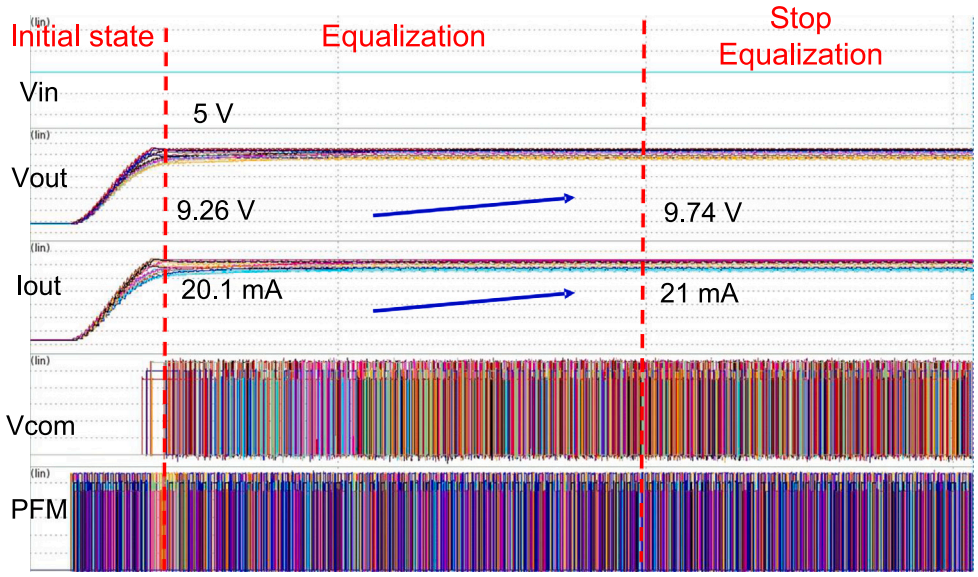

Fig. 14. Various-PVT-corner post-layout simulation result of proposed LED driver.

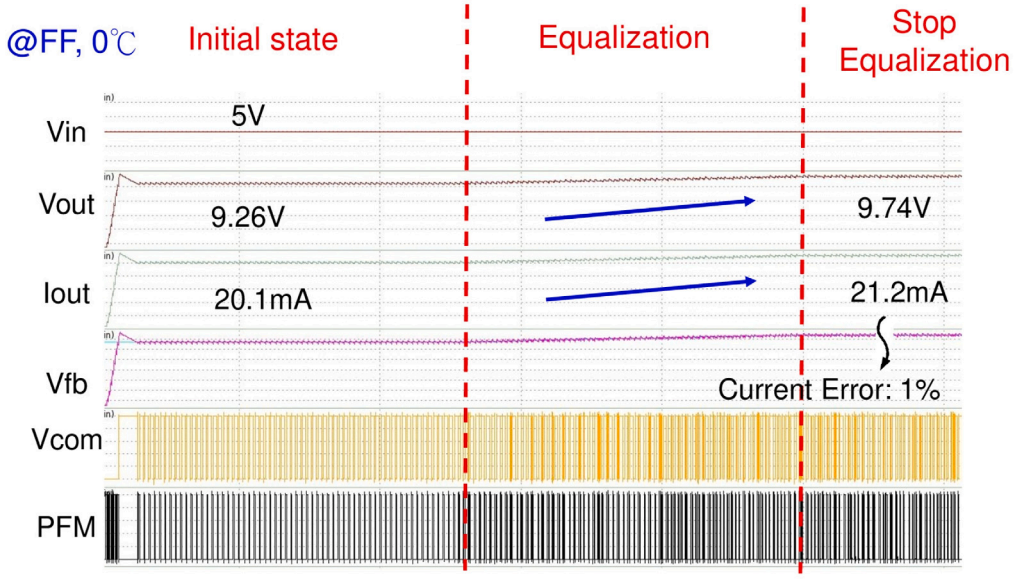

Fig. 15. Worst case post-layout simulation.

4. Conclusion

The proposed LED driver incorporates a high-precision illuminance equalization mechanism and a PFM Control Circuit, resulting in an energy-efficient solution. Through all-PVT-corner post-layout simulation, the LED driver achieves an impressive efficiency of 93%. Furthermore, measurement results confirm an efficiency of 91%. Silicon measurements demonstrate a current error of only 1% at an LED output

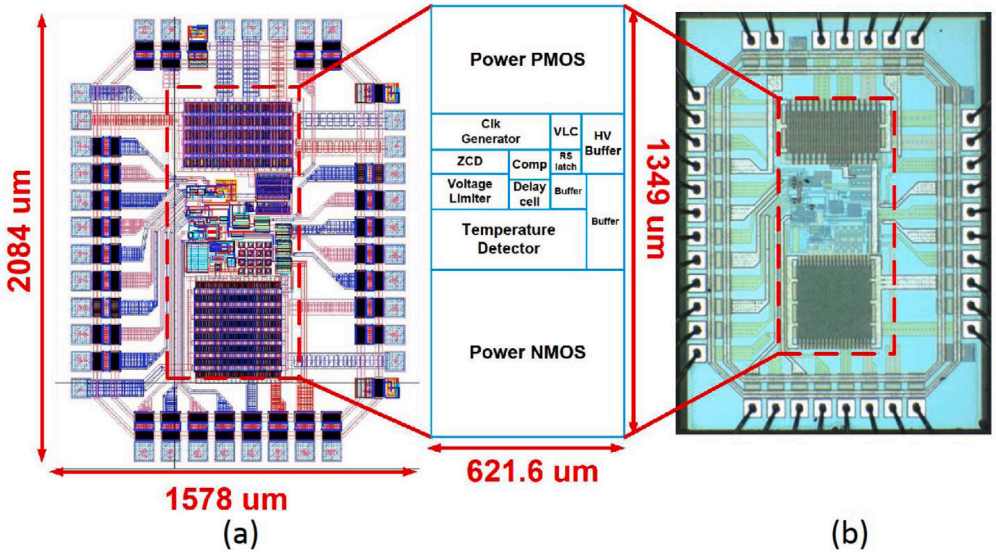

Fig. 16. (a) LED driver layout; (b) LED driver die photo.

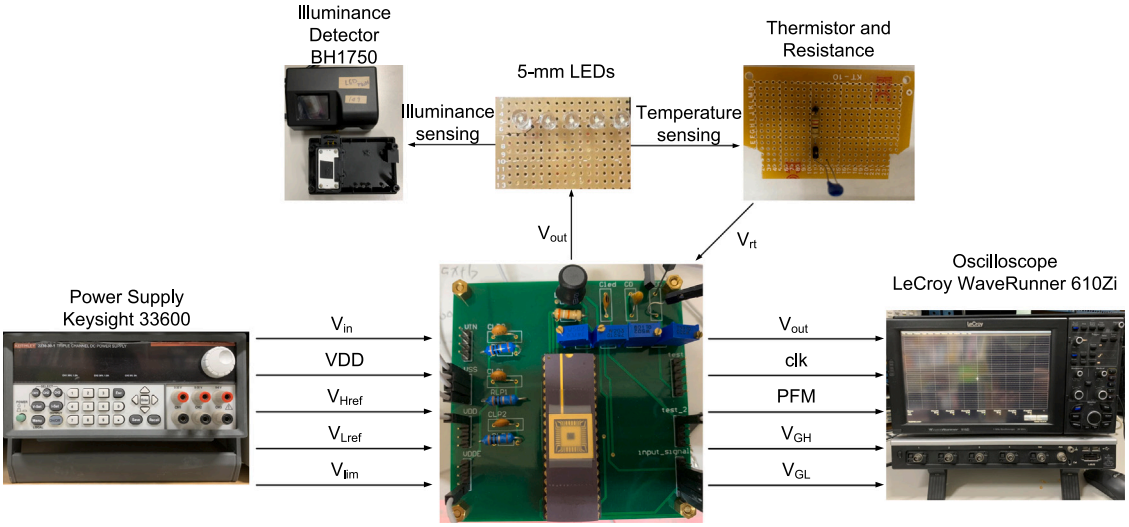

Fig. 17. Measurement setup and equipment.

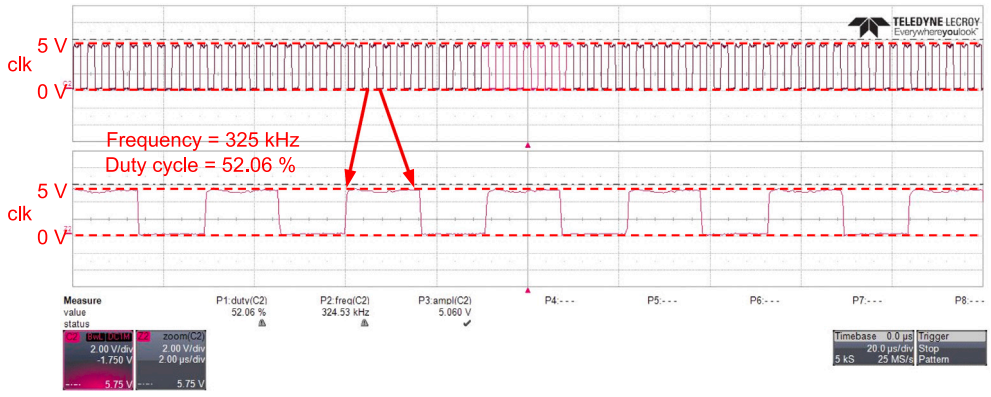

Fig. 18. Measurement of the clk.

Fig. 19. Measurement result of PFM Control Circuit.

Fig. 20. Measurement result of V_{GH} and V_{GL}.

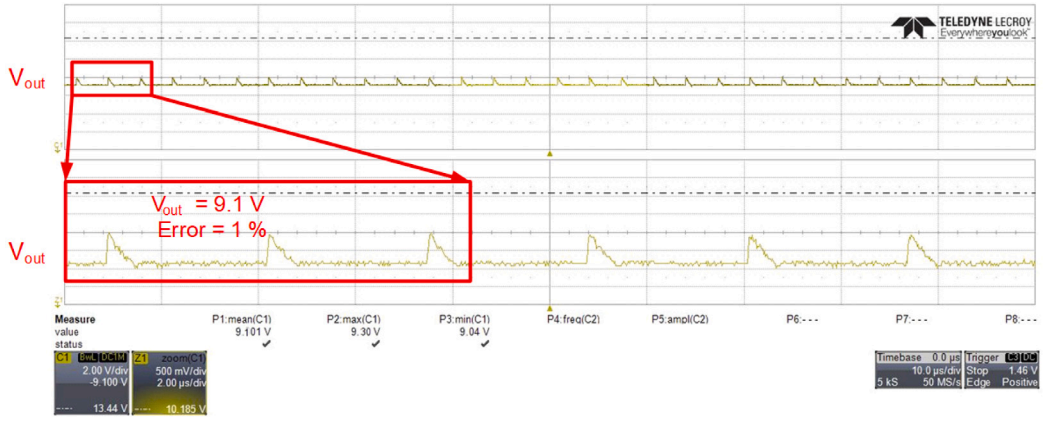

Fig. 21. The measurement result of V_{out}.

Table 1
Measurement readings of the proposed LED driver.

Time (s)	Illuminance (lux) with equalization	Illuminance (lux) without equalization	V_{out} (V)	Temperature (°C)
0	228	228	9.1	25
30	224	224	9.1	29.5
60	222	222	9.2	32.1
90	220	221	9.2	34.3
120	225	219	9.3	35.1
180	224	218	9.3	37.8
240	225	218	9.3	38.9
300	226	216	9.4	41
360	226	215	9.5	42.9
420	227	215	9.6	42.3
Error Avg.$^{\Theta}$	0.5%	3%		

$^{\Theta}\text{Error Average} = \frac{\sum |\text{Illuminance} - \text{Average Illuminance}|}{\text{The total Number of data} \times \text{Average Illuminance}}$.

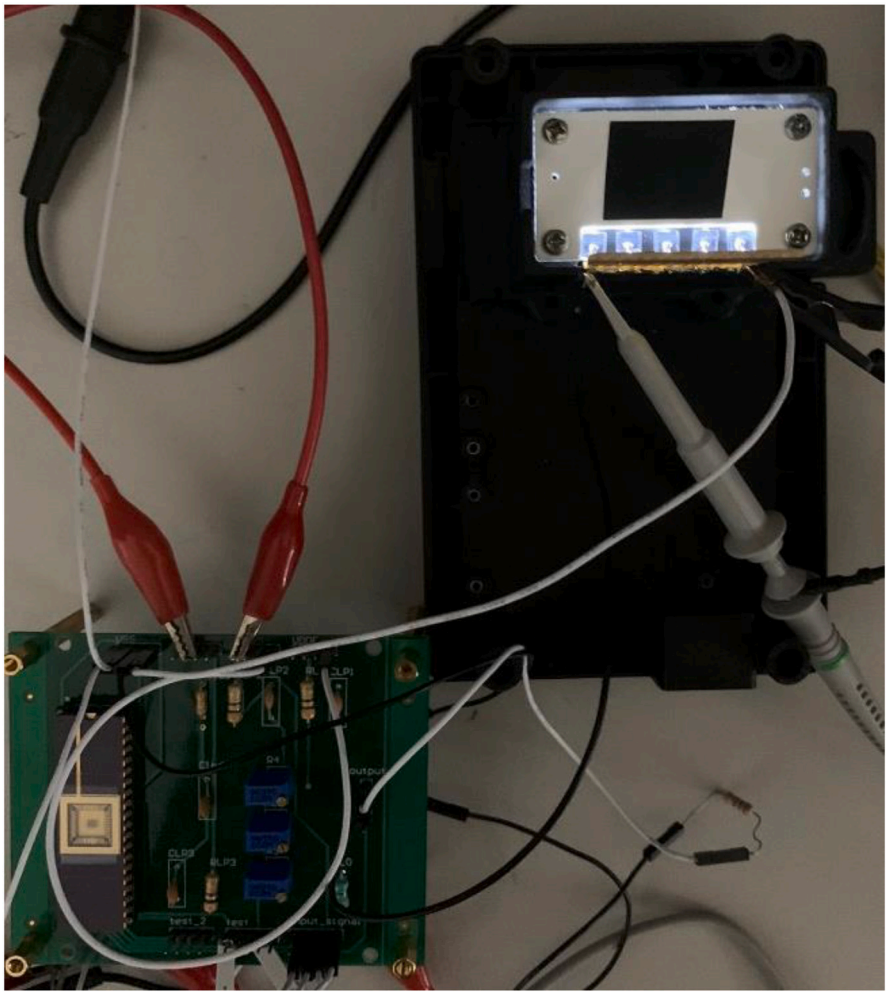

Fig. 22. The photo of the LED string driven by the proposed chip.

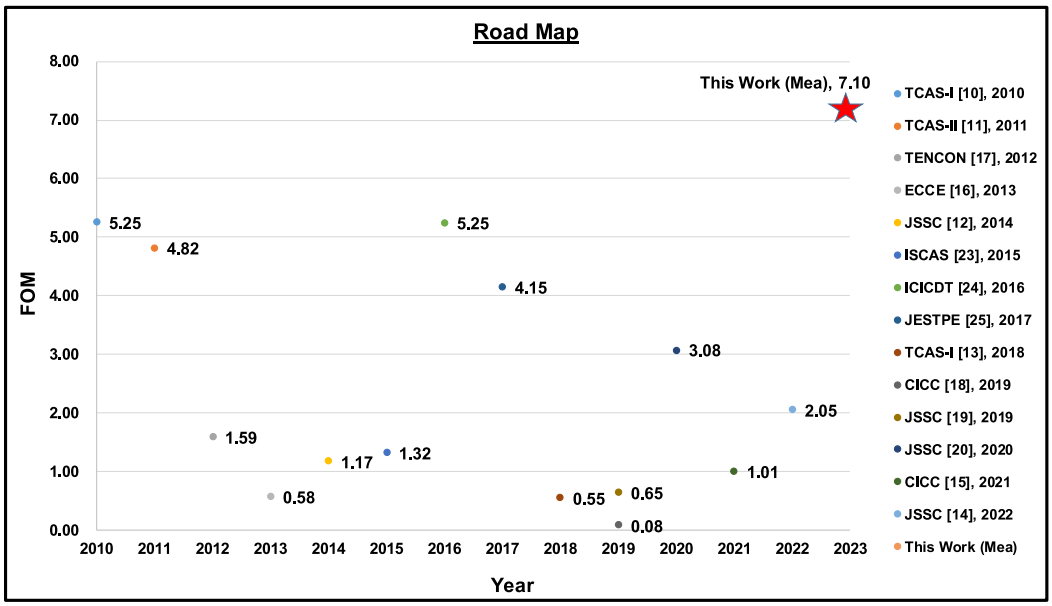

Fig. 23. Technology Roadmap of LED drivers.

Table 2
Performance comparison with prior works.

	TENCON [17]	JSSC [12]	TCSI [13]	CICC [18]	JSSC [14]	This work
Year	2012	2014	2018	2019	2022	2023
Process (nm)	350	350	500	130	500	500
Control Method	Boost	Buck	Buck	I^2V^2	ADCHC	Boost and PFM
Switch Frequency (kHz)	600	1000	2200	1500	1800	350
Illuminance Uniformity [4]	N/A	N/A	N/A	N/A	N/A	0.85
Input Voltage(V)	2.7~4.2	10~40	5~115	5~30	5~100	4.5~6
Output Current (mA)	27	345	350	3200	350	20~21
Current Error (%)	1.2	2.8	2.7	2.5	3.2	**1.0**
Efficiency (%)	85	93	92.6	92.7	91.7	91
Chip Area (mm^2)	5.45	3.47	7	7.5	3.49	**3.2**
Chip Area (Normalization)	44.49	28.34	28	443.7	13.96	**12.8**
FOM*	1.59	1.17	1.22	0.08	2.05	**7.10**

[4] $\text{Illuminance Uniformity} = \left(\frac{\text{Min. Illuminance}}{\text{Avg. Illuminance}}\right)$ [22].

* $\text{FOM} = \left(\frac{\text{Efficiency}}{\text{Current Error} * \text{Normalized Chip Area}}\right)$

current of 20 mA. Additionally, the illuminance variation is verified to be 0.5% through the same measurements. Both post-layout simulations and measurements support the claim that the illuminance equalization mechanism achieves an accuracy of up to 99%.

CRediT authorship contribution statement

Chua-Chin Wang: Conceptualization, Methodology, Resources, Writing – review & editing, Supervision, Project administration, Funding acquisition. **L S S Pavan Kumar Chodisetti:** Formal analysis, Writing – original draft, Visualization. **Pang-Yen Lou:** Methodology, Validation, Investigation, Writing – original draft. **Chen-Cheng-Hung Hung:** Conceptualization, Methodology, Software, Validation, Formal analysis, Investigation. **Pradyumna Vellanki:** Writing – original draft, Visualization. **Ralph Gerard B. Sangalang:** Methodology, Writing – review & editing. **Lean Karlo S. Tolentino:** Methodology, Writing – review & editing. **Tirso A. Ronquillo:** Conceptualization, Methodology.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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