A 6.25-MHz 3.4-mW Single Clock DPWM Technique Using Matrix Shift Array

Oliver Lexter July A. Jose, Venkata Naveen Kolakaluri, Ralph Gerard B. Sangalang, Lean Karlo S. Tolentino, and Chua-Chin Wang

***Abstract*— Recent digital pulsewidth modulation (DPWM) researches use multiple clock inputs and long D flip-flop (DFF) arrays, which makes scaling to different DPWM frequencies challenging. This brief demonstrates a DPWM that utilizes a single clock and a Matrix shift array, allowing it to be scaled to any frequency and reducing the effects of clock skew. It has a clock gating technique that selects a specific row of DFFs based on the required % duty cycle. The DPWM design has a dead time generator to prevent shoot-throughs. The DPWM has been fabricated using UMC 180-nm CMOS process. The performance and functionality of the DPWM have been verified through the measured comparisons of % duty ratio, dead time (T_{dt}), and output frequency (f_{out}) at input clock frequency ($f_{\text{clk}_{\text{in}}}$) equal to 10∼100 MHz. The DPWM design has a maximum % duty ratio of 90.6%, $T_{dt} = 1.8$ ns, and $f_{\text{out}} = 6.25$ MHz with 3.4-mW power consumption at $f_{\text{clk}_{\text{in}}} = 100$ MHz.**

***Index Terms*— Dead time, digital pulsewidth modulation (DPWM), high efficiency, matrix shift array, single clock.**

I. Introduction

Due to the growth of IoT demand, a decrease in the size and weight of the power supply used in electronic devices has become a necessity [1]. Digital controllers become an attractive candidate for low-power high-frequency power supply applications because of their advantages; programmability, low sensitivity, etc., [2]. digital pulsewidth modulation (DPWM) is one type of digital controller that can operate on a low quiescent current with a low voltage supply, making it ideal for low-power applications [3]. Though analog PWM (APWM) generates an accurate output, it is difficult to use in low-voltage applications due to analog circuit headroom challenges [4]. An additional circuit to compensate for the low power dissipation of APWM compared to DPWM will not resolve the analog headroom issues, because it depends on the MOS characteristics. By contrast, DPWM requires a high-frequency clock signal to deal with the control process. Because DPWM has no headroom limitations, it can be easily adapted to the advanced CMOS processes.

Manuscript received 31 July 2023; revised 8 December 2023 and 12 January 2024; accepted 7 February 2024. This work was supported in part by the National Science and Technology Council (NSTC) under Grant NSTC 205 111-2623-E-110-002 and Grant NSTC 110-2221-E-110-063-MY2. *(Corresponding author: Chua-Chin Wang.)*

Oliver Lexter July A. Jose and Venkata Naveen Kolakaluri are with the Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung 80424, Taiwan.

Ralph Gerard B. Sangalang is with the Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung 80424, Taiwan, and also with the Department of Electronics Engineering, Batangas State University, The National Engineering University, Batangas 4200, Philippines.

Lean Karlo S. Tolentino is with the Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung 80424, Taiwan, and also with the Department of Electronics Engineering, Technological University of the Philippines, Manila 1106, Philippines.

Chua-Chin Wang is with the Department of Electrical Engineering and the Institute of Undersea Technology, National Sun Yat-sen University, Kaohsiung 80424, Taiwan, and also with the Vel Tech High Tech Dr.Rangarajan Dr.Sakunthala Engineering College, Chennai 600062, India (e-mail: ccwang@ee.nsysu.edu.tw).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TVLSI.2024.3367300.

Digital Object Identifier 10.1109/TVLSI.2024.3367300

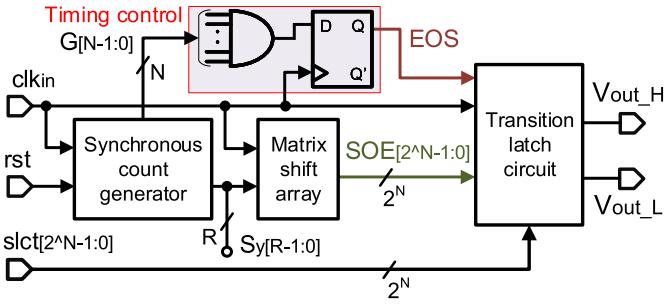

Fig. 1. Proposed DPWM block diagram.

A DPWM controller takes advantage of a current source selector for high resolution with lower clock frequency requirements [5]. Even though it operates at high resolution, the current source selector is prone to Process, Voltage, Temperature (PVT) and capacitance variation.

A prior study used two multi-phase clock arrays and a time-inserting method to generate the PWM [6]. Different input clock frequencies and multiple phases make scaling to different DPWM frequencies infeasible. In addition, this can be only implemented in FPGAs, which consume a large area, power, and cost.

A DPWM implemented in 40-nm CMOS utilized a long chain of D flip-flops (DFFs) for low-power PWM buck converters was reported [7]. The controller improves the power efficiency of the buck converter through the automatic selection of discontinuous conduction mode (DCM) or continuous conduction mode (CCM). However, it has three clock inputs, making it difficult to synchronize and operate at different frequencies. Another research used a long chain of DFF for a low-power PWM buck converter design [8]. Though it only uses two clock inputs, it is still prone to instability [9].

This research presents a DPWM technique that uses a single clock input. A single clock will not require additional signal timing and an extra circuit to synchronize all the clock inputs [10]. It implements a Matrix shift array in which the DFF-based chain can be grouped into several rows and columns to minimize the effect of clock skew. The DPWM Dead time generator prevents shoot-throughs during any operation. In addition, the dual-edge clocking mechanism reduces the glitches generated by shift registers. The functionality and stability have been verified through physical chip measurement.

II. Matrix Shift Array-Based DPWM

Fig. 1 shows the block diagram of the proposed DPWM. Synchronous count generator converts clk_{in} pulses into distinct timing positions. The Matrix shift array contains 2^N DFF chains arranged into a 4×4 matrix ($N = 4$ in this work). The configuration of the matrix reduces the clock skew of the DPWM. The Transition latch circuit produced the standard DPWM signals ($V_{\text{out\_}H}$ and $V_{\text{out\_}L}$). In addition, it generates a single clk_{in} cycle as the dead time to avoid shoot-throughs [11]. Finally, the Timing control of the proposed DPWM ensures that $T_{\text{PWM}} = 2^N \times T_{\text{clk}_{\text{in}}}$.

The timing diagram for the proposed DPWM is shown in Fig. 2. Signal $S_{y[R-1:0]}$, where R is the number of DFF rows in the matrix

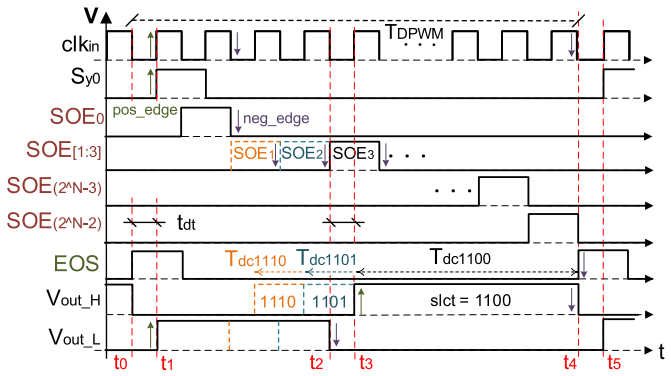

Fig. 2. Timing diagram of the proposed DPWM.

shift array, is a positive edge-triggered single clock pulse that provides coarse timing for start-of-sequence (SOE) generation and repeats every 2^N clock cycle (T_{PWM}). SOE marks the position where the Q of the SR latch in the Transition latch circuit starts to rise. SOE signals are negative edge-triggered and have a half-clock cycle delay from $S_{y[R-1:0]}$ for sustaining the read and write margins of DFFs. SOE position is varied depending on input $\text{slct}_{[2^N-1:0]}$ to modulate the duty cycle. For example, when $\text{slct}_{[2^N-1:0]} = 1100$, SOE = SOE_3, while the modulated duty cycle is T_{dc1100}. In contrast, the position of end-of-sequence (EOS) is fixed for all SOEs. EOS marks the end of the T_{PWM} and ensures that it is equal to $2^N \times T_{\text{clk}_{\text{in}}}$. $V_{\text{out\_}H}$ and $V_{\text{out\_}L}$ is delayed by T_{dt} with respect to SOE to avoid shoot-throughs. The maximum output voltage (V_{o_max}) is given by the following equation:

$$V_{o\_\text{max}} = \left[\frac{(2^N - 1) \cdot T_{\text{clk}_{\text{in}}} - T_{dt}}{2^N \cdot T_{\text{clk}_{\text{in}}}} \cdot 100\% \right] \cdot V_{\text{in}} \tag{1}$$

where T_{dt} is the dead time and N is the DPWM resolution. The maximum % duty cycle for $N = 3$, 4, 5, and 6 are 75%, 90.6%, 96.1%, and 98.24%, respectively. As N increases, the number of DFF and area (limited by the CMOS process) will also increase. However, the additional % duty cycle is dropping. Therefore, choosing $N = 4$ will provide a high % output duty cycle with a smaller area.

A. Synchronous Count Generator

A positive-edge triggered Synchronous count generator shown in Fig. 3 provides timing control for the DPWM. It converts clk_{in} pulses to binary numbers based on the resolution of the DPWM, which state changes at the positive edge of the clock. The N-bit counter pulse-pipelining-based architecture converts each binary equivalent into distinct pulses that indicate specific clock position ($G_{[N-1:0]}$). The number of Synchronous count generator outputs (R) is determined by the arrangement of the DFFs in the Matrix shift array. Regarding the selection of proper "R," it is up to how the DFF is arranged on the silicon. The prior works mainly used a single straight line format [7], [8]. We, on the other hand, propose to arrange DFFs into a 2-D format, namely a matrix array. If $N = 4$, then the number of DFFs = 16. The possible arrangement of DFFs are 1×16 ($R = 1$), 2×8 ($R = 2$), 4×4 ($R = 4$), 8×2 ($R = 8$), and 16×1 ($R = 16$). Apparently, the 4×4 matrix array will most likely to generate equal delays for each path from input to output.

B. Matrix Shift Array

The matrix shift array in Fig. 4 consists of DFF arrays that can be re-arranged into a matrix architecture, where $A = (2^N/R) - 1$, $B = (2^N/C) - 1$, C is the number of columns and R is the number of

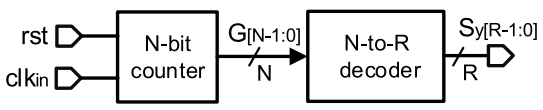

Fig. 3. Synchronous count generator block diagram.

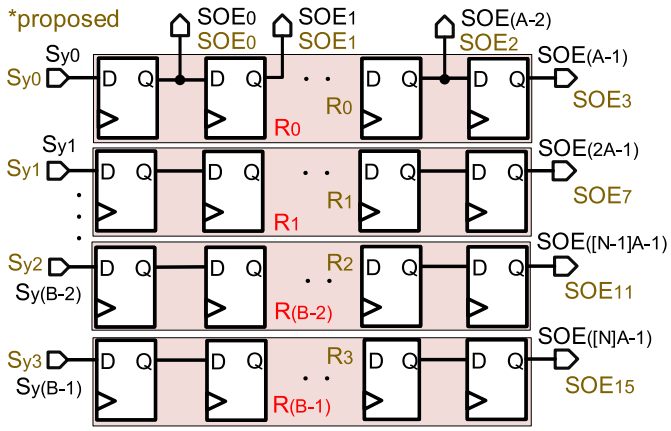

Fig. 4. Matrix shift array schematic (*proposed; $N = 4$, $R = 4$, and $C = 4$).

rows. For example, as R increases with respect to C, the DPWM is less prone to clock skew. However, the size of the N-to-R decoder in the Synchronous count generator will increase as shown by the following equation:

$$R \propto \frac{\text{Area}_{\text{N-to-R decoder}}}{\text{clock skew}}; \quad R > C. \tag{2}$$

By varying the number of columns and rows, it will minimize the clock skew of the DPWM [12]. The square matrix structure offers an optimal trade-off between the number of Synchronous count generator outputs and clock skew, which can be arranged using the following equation:

$$R(\text{Rows}) \cdot C(\text{Columns}) = 2^N. \tag{3}$$

Referring to Fig. 4, which is our example, the proposed DPWM has $N = 4$ used DFF arrayed in a 4×4 matrix. It consists of 16 SOEs, including $\text{SOE}_{[0:3]}$ in R_0, $\text{SOE}_{[4:7]}$ in R_1, $\text{SOE}_{[8:11]}$ in R_2, and $\text{SOE}_{[12:15]}$ in R_3. Matrix shift array number of inputs may vary with the number of R in the DFF arrays, so as the output of the Synchronous count generator. In addition, a half clk_{in} delay between the Synchronous count generator and Matrix shift array eliminates false triggering.

To reduce any redundant clock switches in the DFF array, a clock gating technique is utilized to reduce the power consumption of the Matrix shift array [13]. The Transition latch circuit MUX will trigger specific R in the DFF array based on input $\text{slct}_{[2^N-1:0]}$. For example, R_0, R_1, R_2, and R_3 are triggered when $\text{slct}_{[2^N-1:0]}$ is 11XX, 10XX, 01XX, and 00XX, respectively.

C. Timing Control

The Timing control in Fig. 1 ensures that $V_{\text{out\_}H}$ and $V_{\text{out\_}L}$ will complete a $2^N \times \text{clk}_{\text{in}}$ period for every complete cycle. Its main function is to send a reset pulse in the Transition latch circuit for every T_{PWM}. When the output of the N-bit counter ($G_{[0:N-1]}$) in the Synchronous count generator is all high, a logic high EOS is generated that resets $V_{\text{out\_}H}$ and $V_{\text{out\_}L}$ every T_{PWM}. The Timing control ensures the stability of the DPWM.

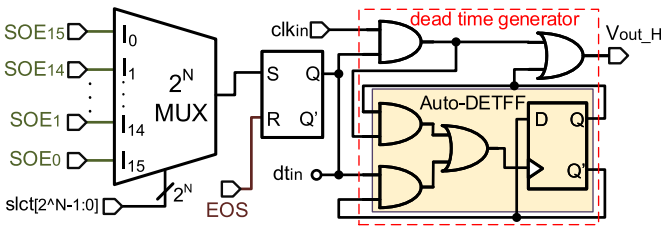

Fig. 5. Transition latch circuit of the proposed DPWM.

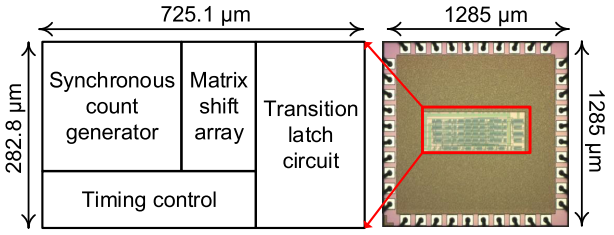

Fig. 6. Floor plan and die photo of the proposed DPWM.

TABLE I

IDEAL AND MEASURED T_{dt}, f_{OUT}, AND % DUTY CYCLE COMPARISON

	T_{dt} (ns)		f_{out} (MHz)		Duty ratio (%)	
f_{clkin} (MHz)	ideal	meas.	ideal	meas.	ideal	meas.
10	50.00	47.00	0.625	0.625	90.6	90.7
20	25.00	21.92	1.250	1.250		90.8
30	16.67	13.74	1.875	1.875		90.8
40	12.50	9.50	2.500	2.500		91.0
50	10.00	6.84	3.125	3.125		90.8
60	8.33	5.73	3.750	3.750		90.9
70	7.14	4.17	4.375	4.375		90.9
80	6.25	3.23	5.000	5.000		91.1
90	5.56	2.54	5.625	5.625		91.3
100	5.00	1.80	6.250	6.250		91.9

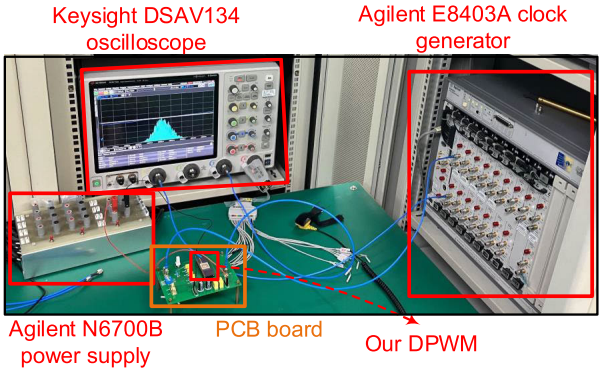

Fig. 7. Measurement set-up of the proposed DPWM technique.

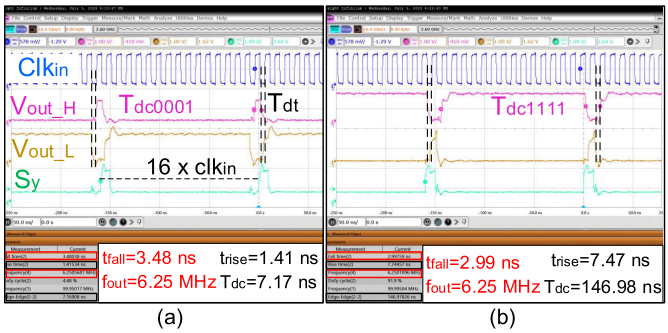

Fig. 8. Waveforms of $V_{\text{out\_}H}$ showing its t_{rise}, t_{fall}, f_{out}, and T_{dc} at $\text{slct}_{[2^N-1:0]}$ = (a) 0001. (b) 1111.

D. Transition Latch Circuit

The Transition latch circuit in Fig. 5 generates the modulated PWM $V_{\text{out\_}H}$ and $V_{\text{out\_}L}$. The SR latch and MUX generates a positive edge PWM signal with a fixed falling edge and a modulated rising edge. The MUX selector determines the position of SOE relative to EOS and generates the corresponding modulated pulsewidth. The MUX is updated at the positive edge of EOS during the transition of selection inputs. A new SOE signal is generated once if EOS ends. Since the MUX output transition is independent of the current $\text{slct}_{[2^N-1:0]}$ input, false triggering is eliminated during the operations. The $\text{slct}_{[2^N-1:0]}$ is refreshed every $2^N \times \text{clk}_{\text{in}}$. Equation (4) defines the $V_{\text{out\_}H}$ effective pulsewidth (turn-on time) for a specific SOE position ($\text{SOE}_{[2^N-1:0]}$) in the DFF array

$$T_{\text{eff}} = \left[(2^N - 1) - \text{SOE}_{[2^N-1:0]}\right] \cdot T_{\text{clk}_{\text{in}}} - T_{dt}. \tag{4}$$

When $\text{SOE}_{[2^N-1:0]} = 2^N - 1$, the SR latch provides an invalid output. To avoid this, the MUX's I_0 input is connected to the GND, resulting in a desired output of $V_{\text{out\_}H}$ = low for $\text{slct}_{[2^N-1:0]} = 0000$.

The dead time generator uses auto dual edge triggering flip-flop (Auto-DETFF) that generates T_{dt} delay between $V_{\text{out\_}H}$ and $V_{\text{out\_}L}$ in reference with DFF output q and q', to prevent shoot-throughs. $V_{\text{out\_}L}$ can be generated by connecting the input of the dead time generator dt_{in} to the Q' of the SR latch. It then generates one clock cycle of dead time from $2^N \times \text{clk}_{\text{in}}$ cycles. A single T_{dt} can be calculated using the following equation:

$$T_{dt} = \frac{1}{2 \cdot f_{\text{out}} \cdot 2^N}. \tag{5}$$

III. IMPLEMENTATION AND MEASUREMENT

Fig. 6 shows the proposed DPWM design fabricated on silicon using a UMC 180-nm CMOS technology. The chip has an overall area of 1285 × 1285 μm^2 and a core area of 725.1 × 282.8 μm^2, respectively.

The measurement set-up for this study is illustrated in Fig. 7. Power supply Agilent N6700B provides 1.8 V V_{DD} and Agilent E8403A for the clock input of the DPWM. Keysight DSAV134 high-frequency oscilloscope is used to observe the DPWM output waveforms.

Fig. 8(a) and (b) shows the rise time (t_{rise}), fall time (t_{fall}), output frequency (f_{out}), and modulated duty cycle (T_{dc}) for $\text{slct}_{[2^N-1:0]}$ input equal to 0001, and 1111, respectively, at C_{load} (probe capacitance) = 30 pF. The ideal modulated frequency ($f_{\text{out(ideal)}}$) can be calculated using (6). The value of $f_{\text{out(ideal)}}$ = 6.25 MHz at $f_{\text{clk}_{\text{in}}}$ of 100 MHz, which is the same for all measurements, demonstrating the DPWM's accuracy. The complementary signals $V_{\text{out\_}H}$ and $V_{\text{out\_}L}$ (including T_{dt}) and $S_{y[R-1:0]}$ (generated every 16 cycles) also show the DPWM functionality

$$f_{\text{out(ideal)}} = \frac{f_{\text{clk}_{\text{in}}}}{2^N}. \tag{6}$$

Illustrated in Fig. 9 is the comparison of ideal (T_{dc}(ideal)) and measured (T_{dc}(meas.)) for all $\text{slct}_{[2^N-1:0]}$ inputs at $f_{\text{clk}_{\text{in}}}$ = 100 MHz. Notice that both lines almost overlapped. The highest variation occurs at $\text{slct}_{[2^N-1:0]} = 0001$ with values of 2.17 ns. The average error of the DPWM is 1.9 ns, which is close to the highest value. At $\text{slct}_{[2^N-1:0]} = 1111$, T_{dc}(ideal) = 145 ns and T_{dc}(meas.) = 146.98 ns, a negligible error of 1.98 ns is derived. The DPWM is less affected by clock skew, which is verified by the linear relationship between T_{dc} and $\text{slct}_{[2^N-1:0]}$ input. Notice also in Fig. 9 that as the

TABLE II
DPWM DESIGN PERFORMANCE COMPARISON

	[7]	[14]	[8]	[15]	this work
Year	2014	2019	2019	2021	2023
Publication	JSSC	ICCE-TW	ICEIC	AICSP	
Technology	40-nm	180-nm	180-nm	65-nm	180-nm
Verification	Meas.	Post-sim	Post-sim	Meas.	Meas.
V_{supply} (V)	0.6 $\sim$ 1.1	1.8	0.6	1.3	1.8
V_{out} (V)	0.3 $\sim$ 0.55	N/A	0.1 $\sim$ 0.5	0.4 $\sim$ 0.9	0.05 $\sim$ 1.6
Output frequency (MHz)	0.1	1	1	1.5 $\sim$ 2	0.625 $\sim$ 6.25
Resolution (bits)	6	6	6	5	4
No. of clk input	3	3	2	2	1
Load	220 μH	-	4.7 μH	2.2 μH & 10 μF	30 pF
Duty ratio range (measured)	0$\sim$50 %	4$\sim$50 %	0 $\sim$ 50 %	30 $\sim$ 70 %	**0 $\sim$ 90.6 %**
Core area (mm^2)	31.43	-	31.73	2.25	**0.205**
Power diss. (mW)	0.038	-	0.180	17.8	3.400
FOM	1.12*	-	0.23*	0.085*	**5.40**

*Computed based on the V_o/I_o and efficiency relationship.

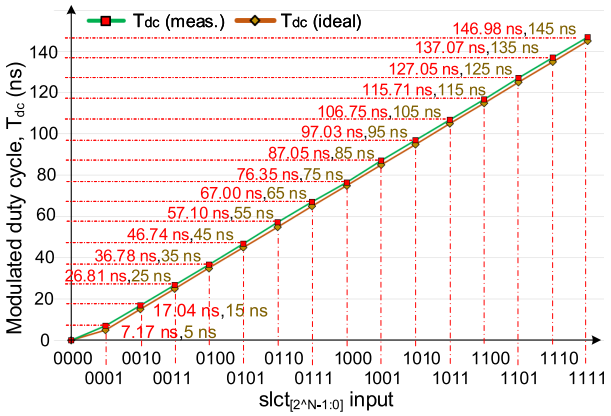

Fig. 9. Modulated duty cycle comparison between $T_{\rm dc}$(ideal) and $T_{\rm dc}$(meas).

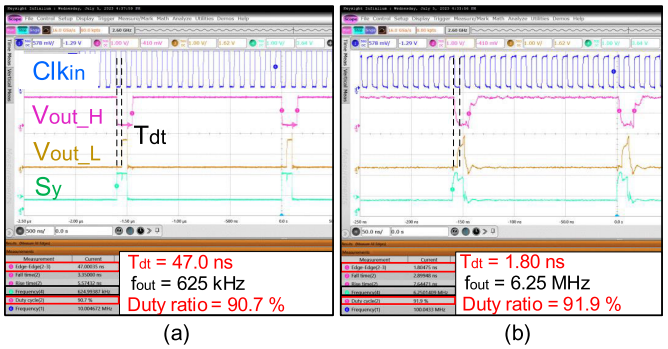

Fig. 10. Waveforms of $V_{\rm out\_H}$ showing its T_{dt}, $f_{\rm out}$, and % duty cycle at $f_{\rm clk_{in}}$ = (a) 10 and (b) 100 MHz.

binary equivalent of input slct$_{[2^N-1:0]}$ increases, the $T_{\rm DPWM}$ also increases. For slct$_{[2^N-1:0]}$ = 0001 and 1111, the $T_{\rm DPWM}$ = 7.17 and 146.98 ns, respectively. The user may vary slct$_{[2^N-1:0]}$ input depends on the required % duty cycle.

Fig. 10(a) and (b) shows the T_{dt}, $f_{\rm out}$, and % duty cycle measurement for clk$_{\rm in}$ frequency equal to 10, and 100 MHz, respectively. As the $f_{\rm clk_{in}}$ rises, it becomes more distorted, resulting in a slight variation between ideal and measured $T_{\rm dc}$ and % duty cycle. In addition, this also affects $V_{\rm out\_H}$ and $V_{\rm out\_L}$ waveforms.

Table I summarizes the comparison between ideal and measured $T_{\rm dc}$, $f_{\rm out}$, and % duty cycle for clk$_{\rm in}$ frequency of 10 to 100 MHz in decade increments. The highest variation of dead time and % duty cycle occurs at the highest clk$_{\rm in}$ frequency with a low variation

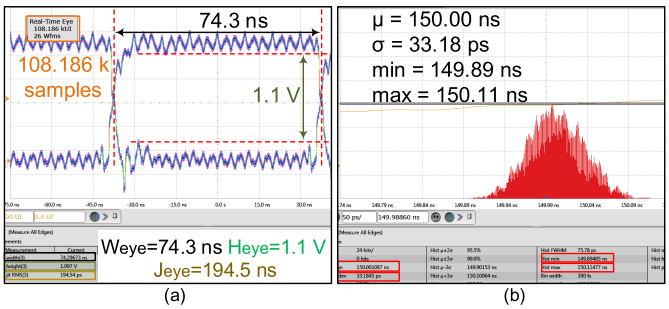

Fig. 11. Proposed DPWM's. (a) Eye diagram. (b) Jitter histogram.

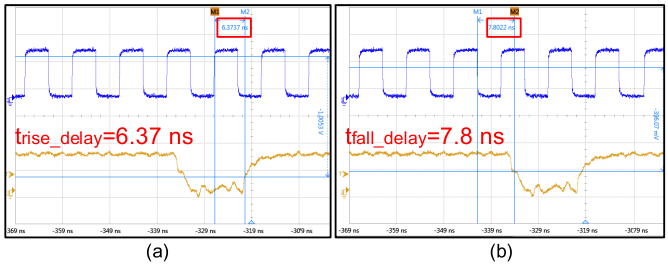

Fig. 12. DPWM's $V_{\rm out\_H}$ showing its (a) $t_{\rm rise\_delay}$ and (b) $t_{\rm fall\_delay}$ measurement at slct$_{[2^N-1:0]}$ = 1111 and $f_{\rm clk_{in}}$ = 100 MHz.

range of up to 3.2 ns and 1.3%, respectively. Notably, the modulated frequency for both ideal and measured cases is the same, showing that the propagation delay is not affecting the DPWM performance.

The eye diagram measurement for the proposed DPWM is shown in Fig. 11(a). The eye diagram has a height of 1.1 V, a width of 74.3 ns, and 194.5 ps jitter for 108.186 k samples. The eye is more relaxed and has a wide open area indicating that it can operate in the presence of interference and has a high signal-to-noise ratio (SNR). It also features a smaller slope, showing the design is less affected by timing error. The $V_{\rm out\_H}$ jitter histogram for the proposed DPWM is shown in Fig. 11(b). It follows the normal distribution curve generated by random activity, with a mean (μ) = 150 ns and a deviation (σ) = 33.18 ps.

The propagation delay can be determined using Fig. 12(a) and (b), with a value of 7.085 ns at slct$_{[2^N-1:0]}$ = 1111 and $f_{\rm clk_{in}}$ = 100 MHz.

The performance comparison with prior DPWM designs is tabulated in Table II. Compared to [7] and [8], our DPWM employs a single clock and is tested in different $f_{\rm clkinput}$, demonstrating

a wide range of scalability. The proposed DPWM also attained the highest output frequency of 6.25 MHz and an actual % duty cycle of 90.6%. At 6.25-MHz frequency with power dissipation of 3 mW, the proposed DPWM can be implemented into a dc–dc buck converter for IoT applications [16]. The Matrix shift array resolves the issue [7] and [8] long-chain DFF array and has been validated through the linear relationship between $\text{slct}_{[2^N-1:0]}$ input and modulated frequency. Using the following equation, our work achieves the highest FOM:

$$\text{FOM} = \frac{V_{\text{DD}}^2(V) \times f_{\text{out\_max}}(\text{MHz}) \times \%\text{duty\_cylce}}{\text{Power\_diss.(mW)} \times \text{No.\_of\_clk}}. \quad (7)$$

IV. Conclusion

This research demonstrates a DPWM technique that utilizes a single clock and Matrix Shift Array fabricated using UMC 180-nm CMOS process. The DPWM technique reduces the effect of clock skew and can be implemented in different input clock frequencies. A 1.8 ns dead time prevents shoot-throughs during operations. The linear relationship between % duty cycle and $\text{slct}_{[2^N-1:0]}$ input proves the design resistance from clock skew. It attains a maximum duty cycle of 90.6% and an f_{out} equal to 6.25 MHz at $f_{\text{clk}_{\text{in}}} = 100$ MHz.

References

[1] Y. Furukawa, H. Nakamura, H. Eto, and F. Kurokawa, "Fine resolution DPWM circuit for high frequency digital control DC–DC converter," in *Proc. Int. Symp. Power Electron., Electr. Drives, Autom. Motion (SPEEDAM)*, Jun. 2018, pp. 491–496.

[2] S. Guo, Y. Gao, Y. Xu, X. Lin-Shi, and B. Allard, "Digital PWM controller for high-frequency low-power DC–DC switching mode power supply," in *Proc. IEEE 6th Int. Power Electron. Motion Control Conf.*, May 2009, pp. 1340–1346.

[3] P. Chen, C. Wu, and K. Lin, "A 50 nW-to-10 mW output power tri-mode digital buck converter with self-tracking zero current detection for photovoltaic energy harvesting," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 523–532, Feb. 2016.

[4] C.-C. Wang, O. L. J. A. Jose, P.-Y. Lou, C.-J. Hsu, L. K. S. Tolentino, and R. G. B. Sangalang, "Single-chip DC–DC buck converter design based on PWM with high-efficiency in light load," *Int. J. Electron. Lett.*, vol. 11, no. 3, pp. 1–12, May 2022.

[5] H.-C. Chen, "A high-resolution digital PWM controller using capacitor integration," in *Proc. Int. Symp. Next Gener. Electron.*, Nov. 2010, pp. 166–169.

[6] C. Xiao, W. Tingcun, and C. Nan, "A novel DPWM structure with high time resolution and low clock frequency," in *Proc. 5th Int. Conf. Intell. Control Inf. Process.*, Aug. 2014, pp. 386–389.

[7] X. Zhang et al., "A 0.6 V input CCM/DCM operating digital buck converter in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2377–2386, Nov. 2014.

[8] T.-H. Kim, D.-J. Kim, H.-S. Shin, S.-H. Lee, J.-W. Suh, and B.-D. Yang, "Low power digital PWM buck converter with a clock-gating shift-register," in *Proc. Int. Conf. Electron., Inf., Commun. (ICEIC)*, Jan. 2019, pp. 1–3.

[9] X. Chen, D. Li, J. Wan, and N. Zhou, "A clock synchronization method for EtherCAT master," *Microprocessors Microsyst.*, vol. 46, pp. 211–218, Oct. 2016.

[10] Texas Instruments. (Dec. 2019). *Multi-Clock Synchronization*. [Online]. Available: https://www.ti.com/lit/an/snaa294/snaa294.pdf

[11] L. Xin-Jun, L. Yun-Lian, and W. Tie-Bin, "Dead-time compensation strategy based on SVPWM," in *Proc. Int. Conf. Comput. Syst., Electron. Control (ICCSEC)*, Dec. 2017, pp. 1751–1755.

[12] C. Sitik, L. Filippini, E. Salman, and B. Taskin, "High performance low swing clock tree synthesis with custom D flip-flop design," in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI*, Jul. 2014, pp. 498–503.

[13] G. S. R. Srivatsava, P. Singh, S. Gaggar, and S. K. Vishvakarma, "Dynamic power reduction through clock gating technique for low power memory applications," in *Proc. IEEE Int. Conf. Electr., Comput. Commun. Technol. (ICECCT)*, Mar. 2015, pp. 1–6.

[14] C.-J. Yang, M.-J. Li, C.-Y. Liu, M.-H. Sheu, and C.-C. Sun, "Low-power counter-based delay line design for DPWM," in *Proc. IEEE Int. Conf. Consum. Electron.-Taiwan (ICCE-TW)*, May 2019, pp. 1–2.

[15] H.-R. Yang and K. S. Yoon, "Digitally controlled PWM buck converter employing counter and VCOs," *Anal. Integr. Circuits Signal Process.*, vol. 109, no. 2, pp. 261–269, Sep. 2021.

[16] S.-Y. Kim et al., "Design of a high efficiency DC–DC buck converter with two-step digital PWM and low power self-tracking zero current detector for IoT applications," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1428–1439, Feb. 2018.