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A 13.73 ns Input Time Range TDA Design Based on Adjustable Current Sources Using 40-nm CMOS Process

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Abstract
This study presents a time-difference amplifier (TDA) based on adjustable current sources. The proposed amplifier uses a phase detection circuit, delay element, and current source architecture for time-difference (i.e., delay) amplification. It includes a reset circuit that prevents the capacitors in the current sources from charging and discharging simultaneously. In addition, an adjustable current source control increases the range of input time difference. The TDA design is implemented in TSMC 40-nm technology with $964.24 \times 961.81\,\mu m^2$ overall chip area and $209.42 \times 84.76\,\mu m^2$ core area. The TDA achieves the widest time-difference input range of $\pm$ 13,730 ps, less than 4% gain error, the lowest supply voltage, and the highest FOM compared to prior TDAs.

Keywords Time-difference amplifier (TDA) · Adjustable current sources · Wide input time difference · High variable gain

1 Introduction

As CMOS process technology advances into the single-digital nanometer era, the design of mixed-signal blocks becomes more difficult [17]. For instance, ADCs (analog-to-digital converters) designs in nanoscale technologies are challenging due to the reduction of power supply for low-power consumption applications. As a result, TDCs (time-to-digital converters) have been suggested instead of ADCs to improve and maintain the resolution [11]. In theory, a high-resolution TDC outperforms a low-

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resolution TDC for synchronization and measurement applications [2, 16]. A VDL (Vernier Delay Line) TDC increases the converter resolution by minimizing the difference in VDL delays [19]. However, a high-resolution Vernier-bias TDC requires a large area and will be easily affected by PVT (process, voltage, and temperature variations), which degrades the TDC performance. A coarse-fine TDC has been reported, which increases the TDC's fine-time resolution [4]. This type of TA (time amplifier) achieves a fine-time resolution by resampling the amplified residue time [10]. Consequently, this approach improved the TDC's overall accuracy. Aside from VDL and coarse-fine types, the precision of each bit conversion of the TDC can be improved using a time-difference amplifier (TDA) to enlarge the time period to be measured. In addition, a TDA with a steady gain and wide linear input time difference is necessary to increase the TDC's accuracy and resolution.

TDA's concept is to amplify the time difference between two input signals, providing an output signal linearly proportional to the time delay between the inputs. Therefore, the range of the input's time difference, linearity, power consumption, and reliability are KPIs (key performance indicators) to compare the performance of various TDAs. Conventional TDA uses the meta-stability of the SR latch, and its meta-stability recovery time is approximately equal to the input time difference of the TDC [1]. Due to its simplicity, its open-loop gain relies on the transistor transconductance (g_m) and C_{load}, which is easily affected by PVT (process, voltage, temperature) variation. An inverter chain delay in SR latches was reported to improve the resolution of the TDA, which is less affected by PVT variation [9]. However, the metastable region operation of the SR latch limits the predictability and accuracy of the TDC [20]. TDA with gain modulated by a "closed loop" consisting of a delay switch and two chains of delay cells to control the delay of the variable delay cell (VDC) was reported [13]. The gain is controlled using a DLL-like closed-loop control that utilizes VDC, phase-frequency detector (PFD), and charge pump, trying to ensure stability against PVT variation. The process variation, however, results in a mismatch between two chains of the delay cells and two PFD inputs resulting in an inaccurate VDC/delay cell ratio and a distorted gain.

Another prior approach based on a mathematical analysis of the conventional 2 × TA (cascaded time interval amplifier) [5] using a point of calibration was reported, where the compensation scheme is nonlinear in the TDA's gain, resulting in a lower or higher input time difference from the calibrated point [12]. The current subtraction scheme integrated into the conventional 2 × TA in this report improves its dynamic range and power consumption. Nonetheless, The current subtraction approach has a limited gain and input time difference. Another all-digital programmable TDA with a stable, linear, and programmable gain and an improved resolution was demonstrated [20]. The time latch-based TDA uses three dynamic time memory cells (operates in three phases: write, idle, and read) for time amplification selection to achieve low power, being highly digital, and functional at higher frequencies. Though it achieves accurate gains, the open-loop approach of the programmable TDA is easily affected by PVT variations. A feedback TDA (FTDA) uses feedback keepers that increase the time-difference gain [17]. The gain of the FTDA is improved and controlled by converting the time intervals of its two inputs into a voltage difference on a capacitor. However, the feedback gain control TDA has limited variable gain and resolution,

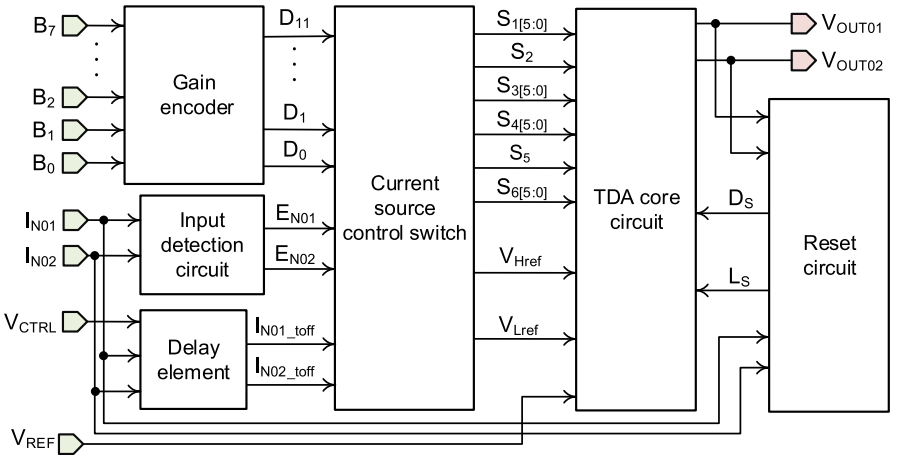

Fig. 1 Proposed adjustable current source-based TDA block diagram

which suffers from excessive PVT variations. Meanwhile, the modified SR latch TDA that provides acceptable linearity properties under PVT variations has a restricted variable input time difference [11].

This research demonstrates a novel TDA with a redesigned current source topology and timing signal control based on the open-loop slew-rate control method [7] and highly linear [3] TDAs. It contains an adjustable current source control for a broader time-difference input range and a reset circuit that discharges the capacitors at the output after the amplification, allowing the TDA to execute the time amplification for another input difference. The proposed TDA is implemented using TSMC 40-nm CMOS technology to demonstrate a wide input time difference, low gain error, and high variable gain.

2 TDA Based on Adjustable Current Source

The proposed TDA architecture based on an adjustable current source is shown in Fig. 1. Input detection circuit determines which input signal, I_{N01} or I_{N02}, is leading. Its output signals, E_{N01} and E_{N02}, will activate the current source control switch based on which is leading between I_{N01} and I_{N02}. The delay element is also coupled to the current source control switch to resolve the leakage current during switch-off intervals of the current sources, generating a constant time delay in various PVT corners. The time gain of the current source control switch is determined by the inputs $B_{[0:7]}$ of the gain encoder. The current source control switch is coupled to the TDA core circuit for time-difference amplification. Finally, the reset circuit avoids capacitors in current sources from charging and discharging simultaneously.

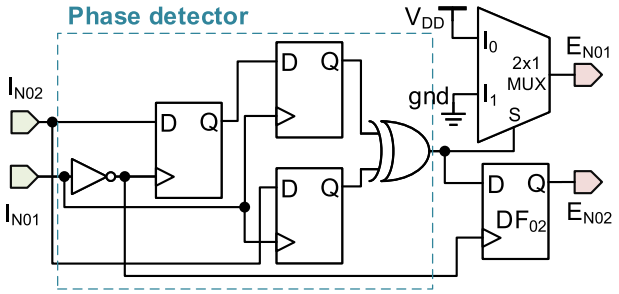

Fig. 2 Input detection circuit schematic diagram

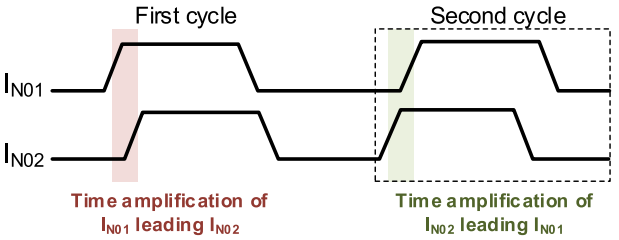

Fig. 3 Input signal detection timing diagram

2.1 Input Detection Circuit

Input detection circuit shown in Fig. 2 will determine which of the inputs, I_{N01} and I_{N02}, is leading. Its outputs, E_{N01} and E_{N02}, enable the current source control switch. The operation of the signal detection timing diagram is illustrated in Fig. 3. During the first cycle, signal I_{N01} is earlier than I_{N02}, resulting in a “high” E_{N01} and "low" E_{N02}. As a result, the time amplification in this cycle is complete. In the second cycle, I_{N02} is earlier than I_{N01}. At this point, E_{N02} is high, and E_{N01} is low; thus, the time amplification in this cycle is completed. The Input detection circuit’s phase detector provides a single-bit signal connected to the MUX’s selection input to output E_{N01}. In generating signal E_{N01}, the inverted I_{N01} and phase detector will be the clock signal and D input of the DF02, respectively.

2.2 Delay Element

Because the proposed TDA employs current sources, it generates a significant leakage current during switch-off intervals. A delay element shown in Fig. 4 is intended to address this leakage current, producing the same t_{off} (time delays) at various corners. This circuit delays I_{N01} and I_{N02} by t_{off} (in the picosecond range), producing $I_{\text{N01\_toff}}$ and $I_{\text{N02\_toff}}$, respectively. The delay time of the input signal can be varied through external V_{CTRL} and the internally generated P_{CTRL}. This delay element employs cascaded current-starving inverters to generate required time delays.

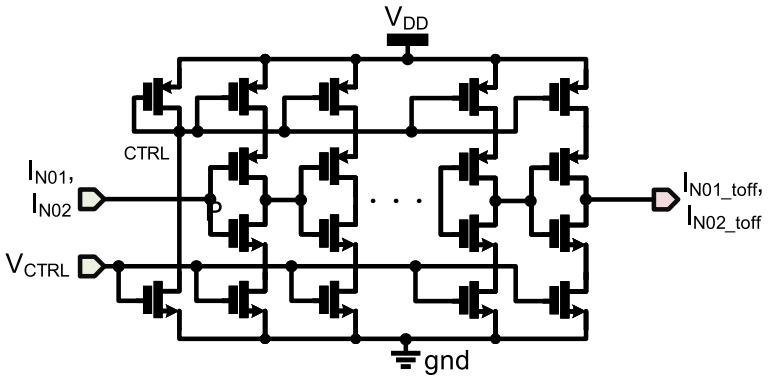

Fig. 4 Delay element circuit [6]

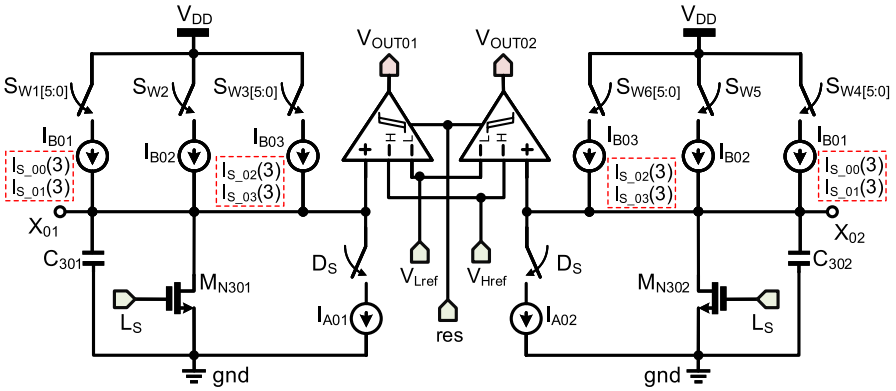

Fig. 5 TDA's core schematic diagram

2.3 TDA Core Circuit

Figure 5 shows the core circuit of the proposed TDA. It is a symmetrical architecture that contains current sources (I_{B01}, I_{B02}, I_{B03}, I_{A01}, and I_{A02}), Schmitt trigger comparator, capacitors (C_{301}, and C_{302}), and NMOS (M_{N301} and M_{N302}). I_{B02} is a single current source, whereas I_{B01} is a combination of current sources I_{S_00} and I_{S_01}, and I_{S_02} and I_{S_03} for I_{B03} for both nodes X_{01} and X_{02}. The switching signals of I_{B01}, I_{B02}, and I_{B03} are $S_{W1[5:0]}$, S_{W2}, and $S_{W3[5:0]}$, respectively, at the side of node X_{01}, while $S_{W4[5:0]}$, S_{W5}, and $S_{W6[5:0]}$ at node X_{02}. Finally, D_S is the signal that controls I_{A01} and I_{A02}, and L_S is the signal that turns on M_{N301} and M_{N302}.

As mentioned, the time amplification of the proposed TDA depends on which inputs I_{N01} and I_{N02} are leading. The two cases are explained as follows:

Case 1: I_{N01} **leads** I_{N02}

Figure 6 shows the timing diagram when I_{N01} leads I_{N02}. At t_0 and t_1, I_{N01} and I_{N02} change from a low potential (gnd) to a high potential (V_{DD}), respectively. The input time difference (Δt_{IN}) is determined from t_0 to t_1. The output time difference

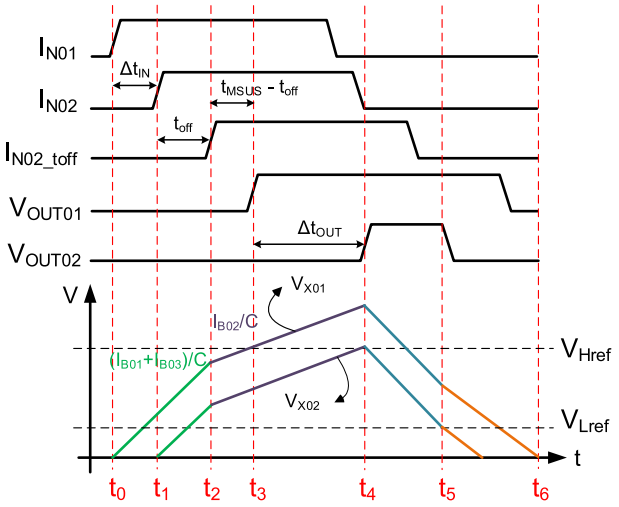

Fig. 6 Timing diagram showing time amplification when I_{N01} leading I_{N02}

(Δt_{OUT}) occurs when both V_{OUT1} (at time point t_3) and V_{OUT2} (at time point t_4) become high potential. When I_{N01} and I_{N02} are initially low (0) and $C_{301} = C_{302} = C$, the charge of the capacitors can be derived through Eqs. (1) and (2) at nodes X_{01} and X_{02}, respectively.

$$V_{Href} \cdot C = (I_{B01} + I_{B03}) \cdot (\Delta t_{IN} + t_{\text{off}}) + I_{B02} \cdot [t_3 - (\Delta t_{IN} + t_{\text{off}})] \quad (1)$$

$$V_{Href} \cdot C = t_{\text{off}} \cdot (I_{B01} + I_{B03}) + I_{B02} \cdot [t_4 - (\Delta t_{IN} + t_{\text{off}})] \quad (2)$$

The gain of the proposed TDA (G_{TDA}) for this state can be derived from Eqs. (1) and (2) by computing t_3 and t_4 as follows:

$$\begin{aligned} t_3 &= \frac{V_{Href} \cdot C - (I_{B01} + I_{B03}) \cdot (\Delta t_{IN} + t_{\text{off}})}{I_{B02}} + (\Delta t_{IN} + t_{\text{off}}) \\ t_4 &= \frac{V_{Href} \cdot C - t_{\text{off}} \cdot (I_{B01} + I_{B03})}{I_{B02}} + (\Delta t_{IN} + t_{\text{off}}) \\ G_{TDA} &= \frac{\Delta t_{OUT}}{\Delta t_{IN}} = \frac{t_4 - t_3}{t_1 - t_0} = \frac{I_{B01} + I_{B03}}{I_{B02}} \end{aligned} \quad (3)$$

1. Timing analysis at node X_{01}: Referring again to Fig. 6, after I_{N01} goes high at t_0, current sources I_{B01} and I_{B03} correspondingly open $S_{W1[5:0]}$ (off) and shorted $S_{W3[5:0]}$ (on) until t_2 with a period of $\Delta t_{IN} + t_{\text{off}}$. At t_2, I_{N02_toff} becomes high potential so that the corresponding switch S_{W2} of the current source I_{B02} is turned on, and V_{X01} reaches V_{Href}. During t_3, node X_{O1} outputs a high-potential time-difference amplified signal through the Schmitt comparator V_{OUT01}.
2. Timing analysis at node X_{02}: In Fig. 6 timing diagram, once the I_{N02} reaches high potential first, current sources I_{B01} and I_{B03} correspond to switches $S_{W4[5:0]}$, and

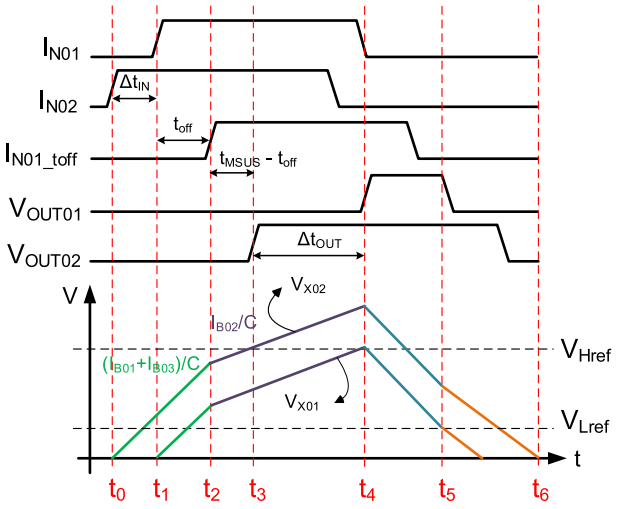

Fig. 7 Timing diagram showing time amplification when I_{N02} leading I_{N01}

$S_{W6[5:0]}$ are turned on until the end of t_2 with a period of t_{off}. At t_2, I_{N02_toff} changes to high potential allowing source I_{B02} corresponding to switch S_{W5} to open. $V_{X_{02}}$ reaches V_{Href} at the same period. During t_4, $V_{X_{02}}$ passes through the Schmitt comparator, producing a high-potential time-difference amplified signal V_{OUT2}.

Case 2: I_{N02} leads I_{N01}

The time amplification timing diagram of the proposed TDA when I_{N02} leads I_{N01} is shown in Fig. 7. I_{N02} changes from low to high potential at t_0. During t_1, I_{N01} becomes high potential, and we can determine the input time difference Δt_{IN} from t_0 to t_1. The output time difference Δt_{OUT} occurs when V_{OUT02} and V_{OUT01} reach high potential at t_3 and t_4, respectively. The charge at nodes X_{01} and X_{02} given $C_{301} = C_{302} = C$, while I_{N01} and I_{N02} are initially low (0), can be derived using Eqs. (4) and (5), respectively:

$$V_{Href} \cdot C = t_{\text{off}} \cdot (I_{B01} + I_{B03}) + I_{B02} \cdot [t_4 - (\Delta t_{IN} + t_{\text{off}})] \tag{4}$$

$$V_{Href} \cdot C = (I_{B01} + I_{B03}) \cdot (\Delta t_{IN} + t_{\text{off}}) + I_{B02} \cdot [t_3 - (\Delta t_{IN} + t_{\text{off}})] \tag{5}$$

G_{TDA} of this state can be determined using Eq. (6) from t_3 and t_4 as follows.

$$\begin{aligned} t_3 &= \frac{V_{Href} \cdot C - (I_{B01} + I_{B03}) \cdot (\Delta t_{IN} + t_{\text{off}})}{I_{B02}} + (\Delta t_{IN} + t_{\text{off}}) \\ t_4 &= \frac{V_{Href} \cdot C - t_{\text{off}} \cdot (I_{B01} + I_{B03})}{I_{B02}} + (\Delta t_{IN} + t_{\text{off}}) \\ G_{TDA} &= \frac{\Delta t_{OUT}}{\Delta t_{IN}} = \frac{t_4 - t_3}{t_1 - t_0} = \frac{I_{B01} + I_{B03}}{I_{B02}} \end{aligned} \tag{6}$$

1. Timing analysis at node X_{01}: In the timing diagram shown in Fig. 7, after I_{N01} becomes high potential at t_1, current sources I_{B01} and I_{B03} correspondingly switch $S_{W4[5:0]}$ and open $S_{W6[5:0]}$ until t_2, with a period of a t_{off}. During t_2, I_{N01_off} changes to high potential letting the current source I_{B02} switch S_{W5} open until $V_{X_{01}}$ reaches V_{Href}. At t_4, $V_{X_{01}}$ passes through the Schmitt comparator, resulting in a high-potential time-difference amplified signal V_{OUT01}.
2. Timing analysis at node X_{02}: Referring again to Fig. 7, after I_{N02} becomes high potential at t_0, current sources I_{B01} and I_{B03} correspondingly turned off $S_{W1[5:0]}$ and turned on $S_{W3[5:0]}$ until t_2 with a period of $\Delta t_{IN} + t_{\text{off}}$. At t_2, I_{N01_toff} becomes high potential allowing S_{W2} of the current source I_{B02} to be turned on until $V_{X_{02}}$ reaches V_{Href}. During t_3, $V_{X_{02}}$ passes through the Schmitt comparator and outputs a high-potential time-difference amplification signal V_{OUT02}.

The time amplification gain for both states is the ratio of the current source (I_{B01} and I_{B03})/I_{B02}. The reset circuit is turned on after t_4.

The node potential $V_{X_{01}}$ or $V_{X_{02}}$ that begins charging first must not be greater than V_{Href} during the period (i.e., $t_{\Delta IN}$ + t_{off}) required to charge the capacitor (C_{301}=C_{302}=C). In addition, the current source I_{B02} is turned on to charge C_{301} and C_{302} to make the nodal voltage reach the trip voltage. When $V_{X_{01}}$ or $V_{X_{02}}$ is higher than V_{Href}, the time amplification gain matches the calculated ratio. In this case, the maximum input time difference is kept at $t_{\Delta INMAX}$, which may be computed using Eqs. (7) and (8) as follows:

$$V_{Href} \geq \frac{(I_{B01} + I_{B03}) \cdot (\Delta t_{INMAX} + t_{\text{off}})}{C} \tag{7}$$

$$\Delta t_{INMAX} \leq \frac{V_{Href} \cdot C}{I_{B01} + I_{B03}} - t_{\text{off}} \tag{8}$$

From the timing diagram in Fig. 6, during time duration t_1 to t_2, both nodes $V_{X_{01}}$ and $V_{X_{02}}$ will be charged to at least [(I_{B01} and I_{B03})·t_{off}]/C. The nodes will be charged further by the current source I_{B02} as it continues charging. In the charging stage of the current source I_{B02}, the input signals I_{N01} and I_{N02} are both at high potential. Equation (9) depicts this case.

$$V_{Href} \cdot C \leq (I_{B01} + I_{B03}) \cdot t_{\text{off}} + (t_{MSUS} - t_{\text{off}}) \cdot I_{B02} \tag{9}$$

The minimum time (t_{MSUS}) necessary for the two input signals to sustain a high potential so that $V_{X_{01}}$ and $V_{X_{02}}$ can reach the high comparison potential V_{Href} of the Schmitt comparator during the charging period of the current source I_{B02}. t_{MSUS} can be determined using Eq. (10) from Eq. (9).

$$t_{MSUS} \geq \frac{V_{Href} \cdot C - (I_{B01} + I_{B03} - I_{B02}) \cdot t_{\text{off}}}{I_{B02}} \tag{10}$$

The shortest period (t_{MIN}) of a square wave input signal (i.e., twice of t_{MSUS}) and the maximum frequency of the input signal (f_{MAX}) can be obtained using Eqs. (11)

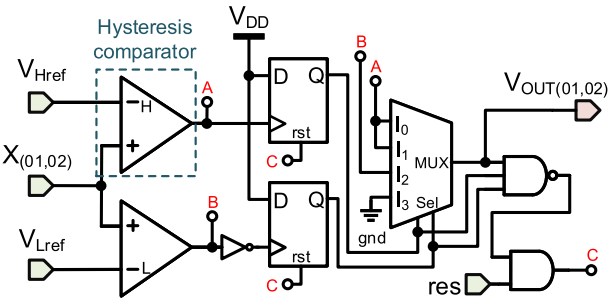

Fig. 8 TDA core circuit Schmitt comparator schematic

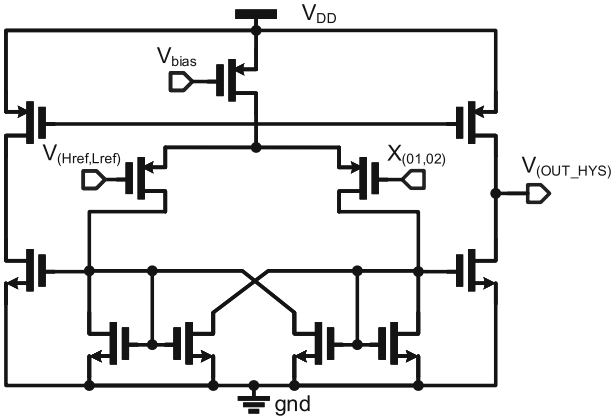

Fig. 9 Hysteresis comparator schematic [8]

and (12), respectively.

$$t_{\mathrm{MIN}} \geq 2 \cdot \left[\frac{V_{\mathrm{Href}} \cdot C - (I_{B01} + I_{B03} - I_{B02}) \cdot t_{\mathrm{off}}}{I_{B02}} \right] \tag{11}$$

$$f_{\mathrm{MAX}} = \frac{1}{t_{\mathrm{MIN}}} \leq \frac{I_{B02}}{2 \cdot [V_{\mathrm{Href}} \cdot C - (I_{B01} + I_{B03} - I_{B02}) \cdot t_{\mathrm{off}}]} \tag{12}$$

Due to the large charge injection created by the conventional Schmitt trigger, the comparator implemented in the core of the proposed TDA has been improved and modified to have an accurate comparison point and output [14]. Shown in Fig. 8 is the schematic of the Schmitt comparator that improves the TDA stability. $\mathrm{X}_{(01,02)}$ is the input of the Schmitt comparator, $\mathrm{V}_{OUT(01,02)}$ is the output signal, the upper and lower comparison references are V_{Href} and V_{Lref}, respectively, and the res input is for reset. The Hysteresis comparator shown in Fig. 9 improves reliability and prevents false switching [8].

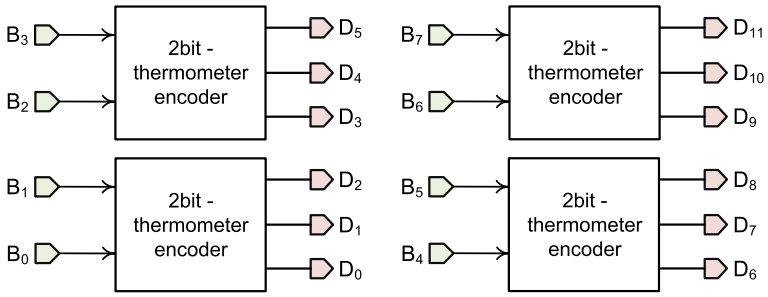

Fig. 10 Gain encoder block diagram

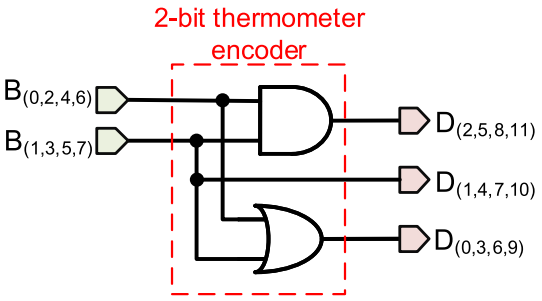

Fig. 11 2-bit thermometer to binary encoder [18]

Table 1 2-bit thermometer to binary encoder conversion table

B_1	B_0	D_2	D_1	D_0
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

2.4 Gain Encoder

As shown in Fig. 10, the gain encoder consists of four groups of 2-bit thermometer encoders, designed to accommodate up to 8 bits and are driven by an external input $B_{[7:0]}$. The 8-bit input is converted to 12-bit code ($D_{[11:0]}$). The 12-bit code, along with I_{N01_toff}, I_{N02_toff}, E_{N01}, and E_{N02}, will be the input to the current source control switch that will determine the value of time gain. The schematic of each 2-bit thermometer code encoder and its corresponding code are shown in Fig. 11 [18] and Table 1, respectively. The output coding signal of this Gain encoder corresponds to four sets of current sources of different sizes. The current sources from large to small are I_{S_03}, I_{S_02}, I_{S_01}, and I_{S_00} are used to form the I_{B03} and I_{B01} current values, as shown in Fig. 5.

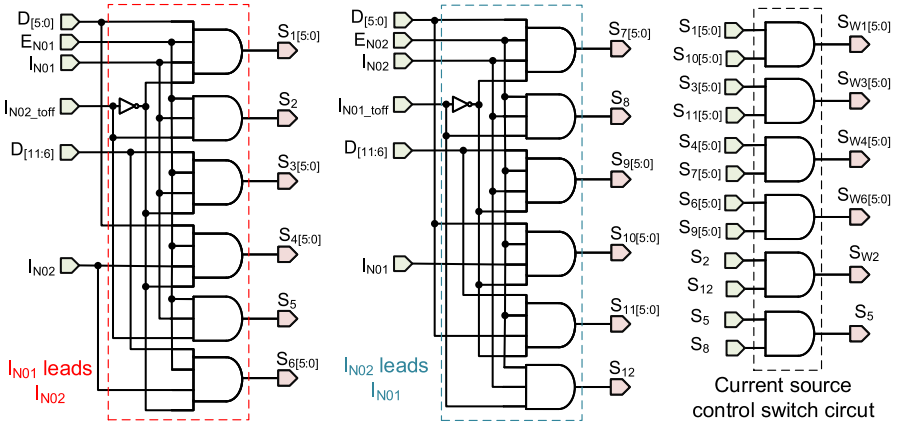

Fig. 12 Current source-controlled switch circuit

Table 2 Functional value of current source control switch circuit

Time interval	$S_{W1[0]}$	$S_{W2[0]}$	$S_{W3[0]}$	$S_{W4[0]}$	S_{W2}	S_{W5}	D_S	L_S
t_0–t_1	1	1	0	0	0	0	0	0
t_1–t_2	1	1	1	1	0	0	0	0
t_2–t_3	0	0	0	0	1	1	0	0
t_3–t_4	0	0	0	0	0	0	1	0
t_4–t_5	0	0	0	0	0	0	0	1

2.5 Current Source Control Switch

Figure 12 shows the current source control switch that generates switching signals required by the TDA core circuit. The signals produced by the input detection circuit (E_{N01} and E_{N02}), delay element (I_{N01_toff} and I_{N02_toff}), and gain encoder ($D_{[11:0]}$) are connected to the input of the control circuit. The current source switching signals of the TDA have different codes for I_{N01} leading and lagging I_{N02}, respectively.

Table 2 illustrates the functional value of the current source control switch circuit when the digital input codes B_0 and B_4 are "1"; while the remaining input codes are "0". This condition will enable one I_{S_00} and one I_{S_02} current source at nodes X_{01} and X_{02}. The table values correspond to the timing diagram in Fig. 6 at each time step when I_{N01} leads I_{N02}.

2.6 Reset Circuit

The reset circuit based on the timing diagram in Figs. 6 and 7 is illustrated in Fig. 13. The reset circuit is turned on after t_4 to perform two-stage discharge as follows:

(1) First-stage discharge

From t_4 to t_5, the output signals V_{OUT01} and V_{OUT02} are connected to the reset circuit's AND gate, creating a D_S signal that goes to current sources I_{A01} and I_{A02}

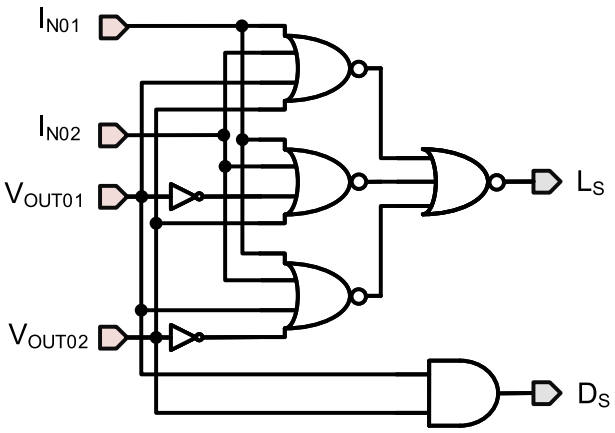

Fig. 13 Reset circuit schematic

(where $I_{A01} = I_{A02}$). Due to the effect of inputs I_{N01} and I_{N02} frequencies, discharging and charging may be performed in parallel until one of $V_{X_{01}}$ or $V_{X_{02}}$ is lower than V_{Lref}. From this point, the current sources I_{A01} and I_{A02} are turned off and will no longer discharge.

(2) Second-stage discharge

This stage occurs when both I_{N01} and I_{N02} are at low potential because $V_{X_{01}}$ and $V_{X_{02}}$ still hold a low residual potential after the first stage of discharge. V_{OUT01} and V_{OUT02} will be divided into the following situations due to the different charging times as follows:

1. Both V_{OUT01} and V_{OUT02} are at low potential.
2. V_{OUT01} is low and V_{OUT02} is still high potential.
3. V_{OUT01} is still at high potential and V_{OUT02} is at low.

3 Simulation and Analysis

The proposed current source-based TDA is implemented using TSMC 40-nm technology. The layout and floorplan of the overall chip are illustrated in Fig. 14. The design has an overall chip size of $964.24 \times 961.81\,\mu m^2$ and a core area of $209.42 \times 84.76\,\mu m^2$.

Figures 15 and 16 show the post-layout simulations when I_{N01} leads I_{N02}. The core circuit's C_{301} and C_{302} have a value of 1 pF, $V_{Href} = 0.7$ V at the operating frequency of 3.3 MHz. In this state, delay t_{off} is 640 ps, while $I_{B01} = 94\ \mu$A, $I_{B02} = 19.6\ \mu$A, and $I_{B03} = 227.3\ \mu$A. Using Eqs. (3) and (8), the theoretical gain of the TDA ($G_{TDA(computed)}$) and linear input maximum range (Δt_{INMAX}) are determined as 16.4 and 1575 ps, respectively.

In Fig. 15, a 130 ps input time difference results in a time amplification of 2.11 ns. The gain of the TDA ($G_{TDA(actual)}$) in this state is 16.23, while gain error (G_{error}) is calculated using Eq. (13), which is equal to 1.036%.

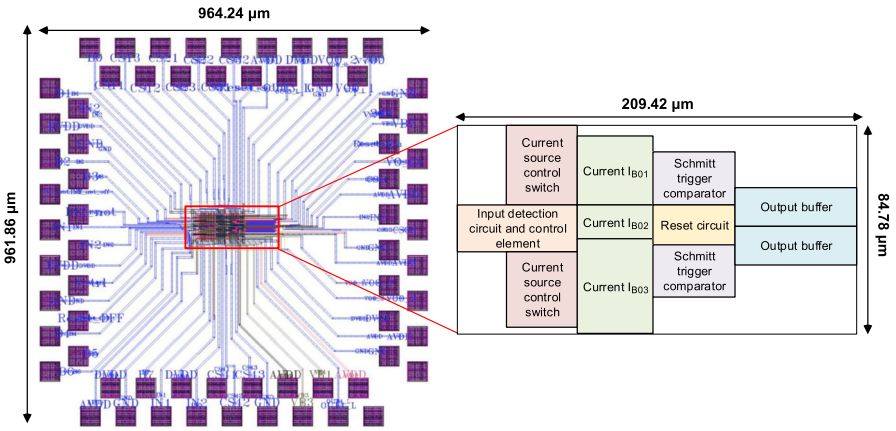

Fig. 14 Current Type TDA layout

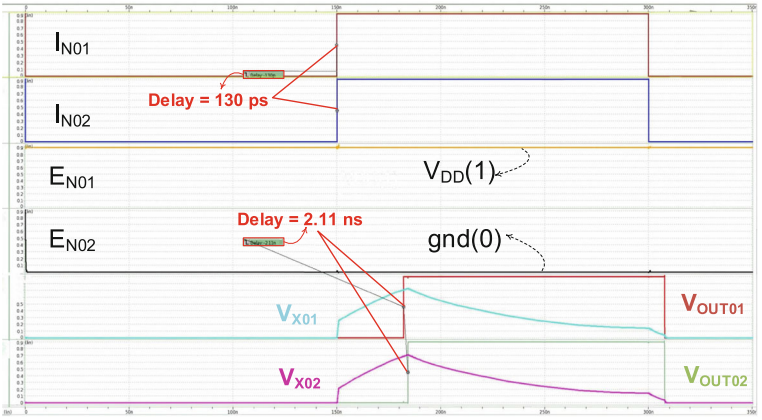

Fig. 15 I_{N01} leads I_{N02} time amplification at Δt_{IN} = 130 ps

$$G_{\text{error}} = \frac{|\, G_{TDA(computed)} - G_{TDA(actual)} \,|}{G_{TDA(computed)}} \times 100\% \tag{13}$$

As illustrated in Fig. 16, an actual time-difference amplification of 25.6 ns is achieved for an input time difference of 1.57 ns. The actual TDA's gain is determined to be 16.3, with a G_{error} of 0.6%.

The post-layout simulations, when I_{N02} leads I_{N01}, are shown in Fig. 17 and 18. It has the same values of C_{301}, C_{302}, V_{Href}, operating frequency, I_{B01}, I_{B02}, I_{B03}, and t_{off} of the previous state. A Δt_{IN} of 30 ps produces an amplified output of 511 ns, as illustrated in Fig. 17. Referring again to Eqs. (3) and (8), the calculated $G_{TDA(actual)}$ is 17 with a G_{error} of 3.65%.

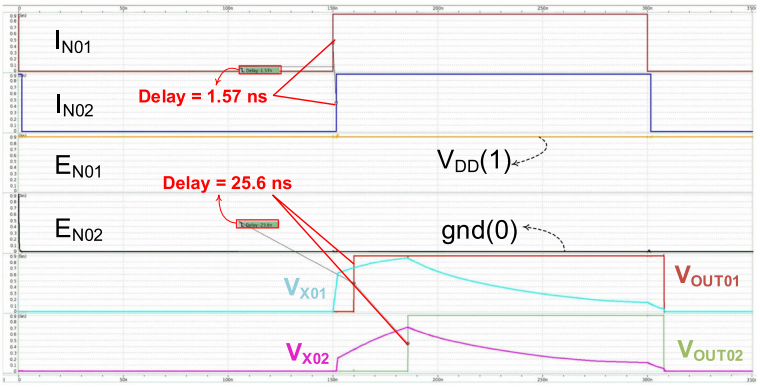

Fig. 16 I_{N01} leads I_{N02} time amplification at Δt_{IN} = 1.57 ns

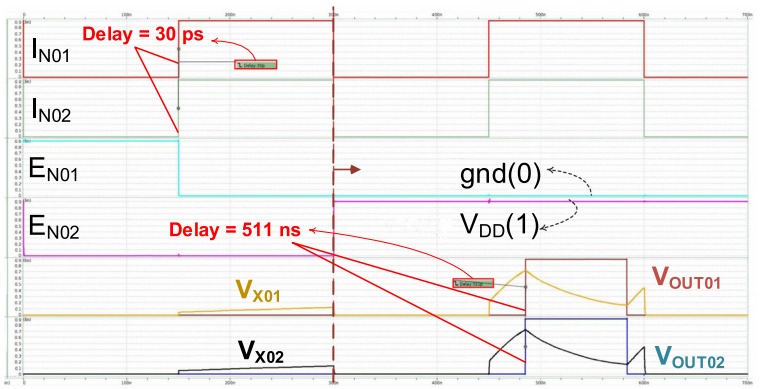

Fig. 17 I_{N02} leads I_{N01} time amplification at Δt_{IN} = 30 ps

In Fig. 18, the input time difference of 300 ps has Δt_{OUT} = 4.81 ns. The actual TDA's gain is calculated to be 16, with a G_{error} of 2.5%.

Figure 19 shows the time input difference and amplified output relationship for different TDA's gain (16.4, 25.3, 41, and 57.8). The linear relationship between Δt_{IN} and Δt_{OUT} in different G_{TDA} demonstrates the TDA's accuracy.

The relationship between Δt_{IN} and gain error is shown in Fig. 20. It has a maximum gain error of approximately 4% at the highest G_{TDA}.

Monte Carlo simulations in terms of TDA gain are run to assess the design's robustness as illustrated in Fig. 21. For 291 samples, the design achieved a minimum and maximum G_{TDA} of 2.1 and 21.52, respectively. It has an average gain (μ) of 13.74 with a deviation (σ) of 3.06, proving the design's robustness.

Table 3 provides a comparison between the designed TDA and prior works. The performance of the TDAs is defined as follows in Eq. (14),

$$\text{FOM} = \log[\text{Input Diff. Range}] \cdot G_{\text{TDA}} \cdot (V_{\text{supply}})^2 \tag{14}$$

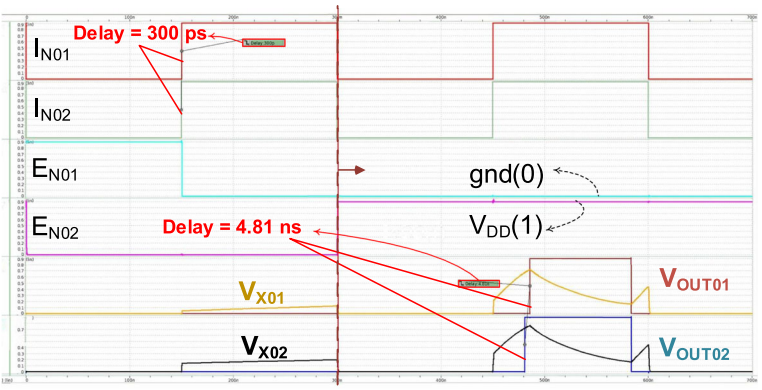

Fig. 18 I_{N02} leads I_{N01} time amplification at Δt_{IN} = 300 ps

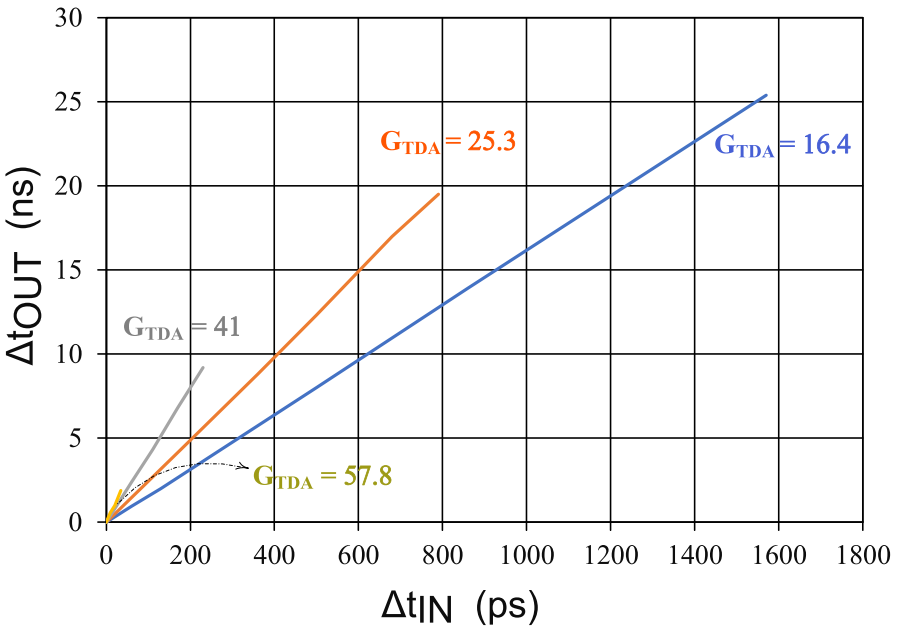

Fig. 19 Proposed TDA Δt_{IN} vs. Δt_{OUT} at different G_{TDA}

where Input Diff. Range is the input time difference range. The proposed TDA has the highest linear input time difference, resulting in a wide range of input that can be amplified. The time amplification gain of the TDA is adjustable, with a relatively wide working range and a low gain error (less than 4%). Notably, the TDA design has the best FOM based on post-layout simulations with a value of 5.8.

Future work includes fabrication and testing of adjustable current source-based TDA on silicon. The measurement setup plan of this TDA is shown in Fig. 22. The Agilent E3631A Power Supply will be used for 8-bit code input $B_{[7:0]}$ and VDD. The Schmitt comparator res signal will be generated by Agilent 33522A Waveform

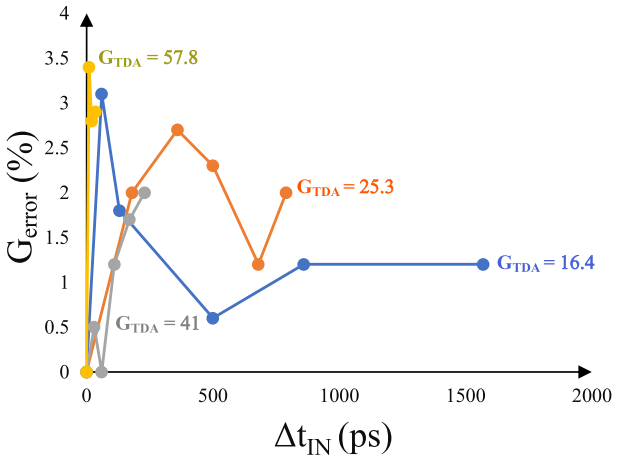

Fig. 20 Proposed TDA G_{error} at different G_{TDA}

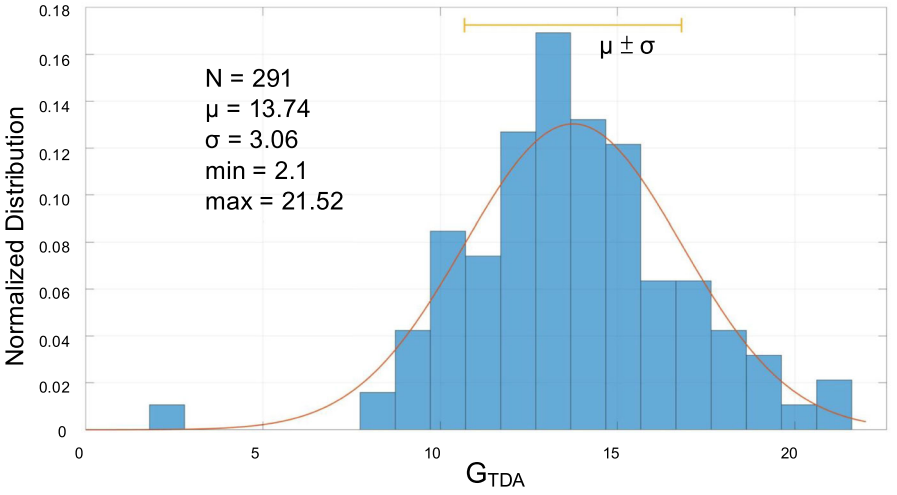

Fig. 21 Monte Carlo simulation for G_{TDA}

Generator. Input signals I_{N01} and I_{N02} will come from the Agilent 81,250 Pattern Generator and be monitored through the Agilent 16962A Logic Analyzer in setting the required frequency and phase difference of the input signals. Finally, the Keysight DSAV134 Oscilloscope will be utilized in observing outputs V_{out01} and V_{out02}.

4 Conclusion

This research demonstrates a time-difference amplifier (TDA) based on an adjustable current source. The proposed TDA has a variable linear input time-difference range, a selectable gain size, and a low gain error. The theoretical derivation of the design has

Table 3 TDA performance comparison

	[12]	[17]	[15]	[20]	[11]	This work
Year	2016	2016	2016	2018	2020	2023
Process (nm)	180	130	130	65	180	40
Verification	Pre-sim	Pre-sim	Pre-sim	Pre-sim	Meas	Post-sim
Supply Voltage (V)	1.2	1.2	1.2	1.0	1.8	0.9
Input Diff. Range (ps)	300	$\pm$ 20	34	200	$\pm$ 130	$\pm$ 13,730
Gain	2	25.06 – 734.9	4	2 – 8	1.54	2.4 – 57.8
Gain Error (%)	N/A	N/A	N/A	< 4	< 6.5	< 4
Clock freq. (MHz)	1000	2	1000	0.45	1000	14
Power disp. (μW)	28	91.54	N/A	518.8	2230	4311
Core area (mm^2)	N/A	N/A	N/A	N/A	0.000182	0.01775
FOM	2.9	4.3	2.3	3.2	2.8	**5.8**

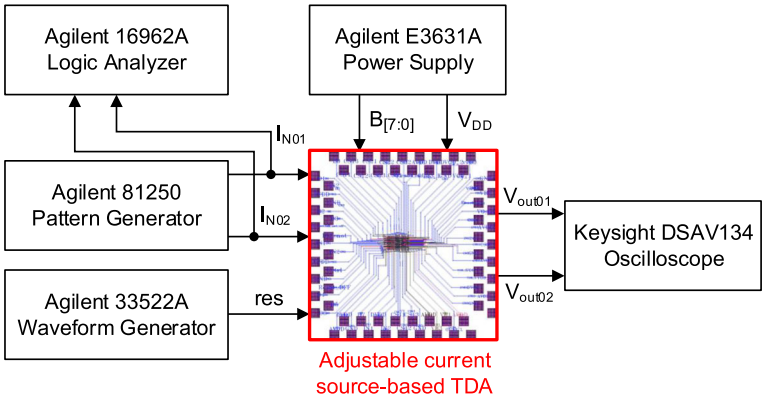

Fig. 22 Proposed measurement setup

been confirmed through post-layout simulation and Monte Carlo analysis. Compared to prior works, the simulation results of our TDA have the best performance in terms of input time-difference range and gain error with the lowest supply voltage.

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