A 210-MHz 4.23 fJ Energy/Bit 1-kb Asymmetrical Schmitt-Trigger-Based SRAM Using 40-nm CMOS Process

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***Abstract*—This study introduces a 1-kb SRAM design that operates at low power utilizing asymmetrical Schmitt-trigger based SRAM cells. By adopting an asymmetrical design, the SRAM cell performance in terms of hold, access, and write capabilities were enhanced. A power reduction and speed compensation circuit is presented in the design. The SRAM is implemented and fabricated on-silicon using a typical 40-nm TSMC CMOS technology. Measurements show that the design can operate up to 210 MHz clock frequency with a 4.23 fJ energy per bit for a supply voltage of 0.8 V. It also has an average delay of 5.659 ns, which is reduced to an average of 1.708 ns when the speed compensation circuit is enabled.**

***Index Terms*—Schmitt trigger, data retention, memory integrity, low power, static noise margin, SRAM cell**

I. Introduction and Overview

SRAM is essential for low power applications because it allows for high-speed data processing and access while using very little power. Internet of Things (IoT), mobile, and wearable devices are examples of low power applications that demand efficient power utilization to optimize battery life and reduce energy consumption. The fast speed and low power consumption of SRAMs make it the perfect memory solution for low power applications [1]. Because of this SRAM feature, the refresh circuitry is not required, which reduces power consumption and simplifies circuit design.

SRAM is intended to be self-sustaining, unlike other forms of memory like dynamic RAM (DRAM), which needs frequent power refresh cycles to keep data state. This makes it perfect for systems like cache memory in microprocessors, graphics processing units (GPUs), and other high-performance systems that need quick access while consuming little power. Overall, SRAM is critical in low power applications due to its capacity to deliver high-speed data access and processing with low power consumption. Battery life optimization, device efficiency improvement, and energy consumption reduction are key factors for contemporary electronic gadgets.

Different techniques have been used to reduce the energy consumption of SRAM designs for the said applications. Examples are single-ended cell configurations [2]–[6], voltage scaling [4]–[6], voltage splitting [7], voltage stacking with array swap [8], and Schmitt-trigger cells [9]–[15]. Single-ended architecture have been proved as an effective way to minimize energy consumption. However, it requires a more complex controller and is somehow more susceptible to noise. Prior Schmitt-trigger SRAM cells proved to have a good noise performance, but it is yet to be tested on silicon [9]–[15].

Contributions of the paper

In this paper, we proposed a 1-kb SRAM with 8T Schmitt-trigger cells that has improved read and write performance having the following attributes: (1) quick access speed, (2) low energy consumption through voltage selection; and (3) high noise immunity. We also presented the implementation and measurement on silicon to support the performance claimed.

This report is sequenced as follows: Section I presents an overview discussion of the study. The architecture, implementation and measurements are presented in Sections II and III, respectively. Finally, a conclusion is given in Section IV.

II. Proposed SRAM Architecture and Cells

A. Proposed Architecture

Fig. 1 shows the top level view of the proposed SRAM consisting of seven (7) main blocks:

- SRAM array (1-kb)
- Power Reduction and Speed Compensation circuit
- Row and Column Decoders
- Control circuit
- Memory Built-In Self-Test (MBIST) Circuit
- Sense Amplifiers
- Output Column Selector

B. Asymmetric Schmitt-trigger based SRAM Cell

Referring to Fig. 2, the proposed cell consists of a traditional inverter, composed of M_{201} and M_{203}, and a Schmitt-trigger (ST) inverter, composed of M_{202}, M_{204}, & M_{205}, acting as the

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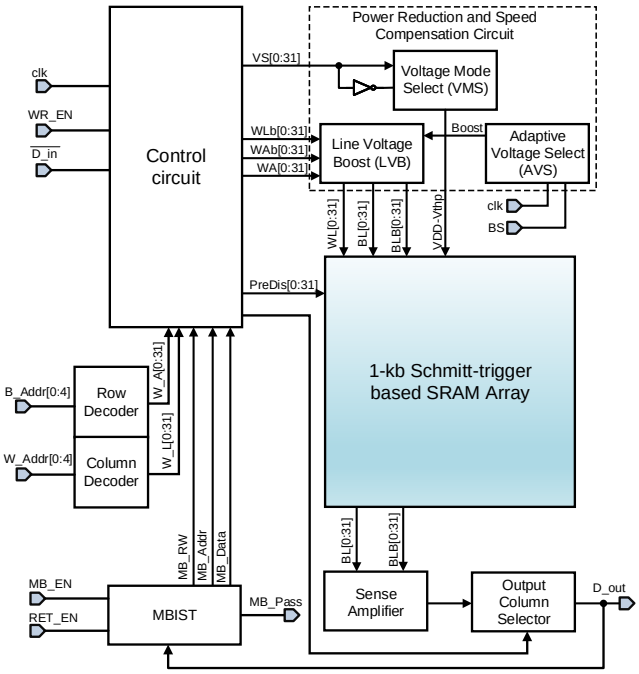

Fig. 1. Block diagram of the proposed 1-kb SRAM

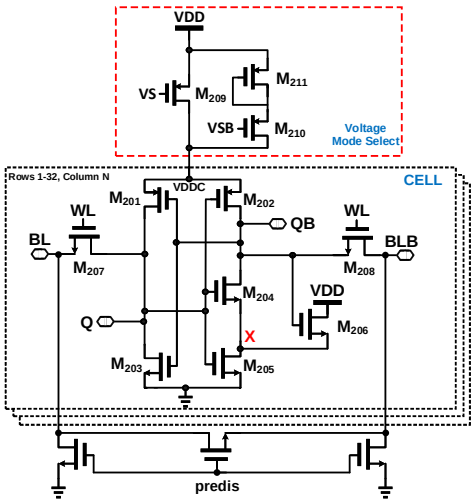

Fig. 2. Asymmetric Schmitt-trigger based SRAM cell with Voltage Mode Select

storage node. M_{207} & M_{208} are the access transistors for the read and write operations. Feedback transistor M_{206} raises the voltage at node 'x' to VDD-Vth when QB is high, requiring a larger voltage at Q to invert QB. Because of this, the noise margin of the SRAM is improved. Fig. 3 shows the voltage transfer curves (VTC) of the ST inverter and the traditional inverter. It shows a steeper curve, due to the positive feedback transistor in the ST inverter, which can improve the noise rejection performance.

Shown in Fig. 4 is the timing waveform of the three operations of the proposed SRAM, namely read, write, and standby operations.

1) Write and Read operations: During the write operation, the bitlines (BL/BLB) are pre-discharged firstly to refresh the

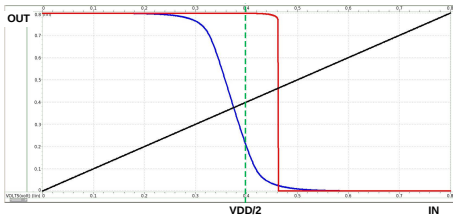

Fig. 3. Schmitt-trigger and traditional inverter voltage transfer curves (VTC)

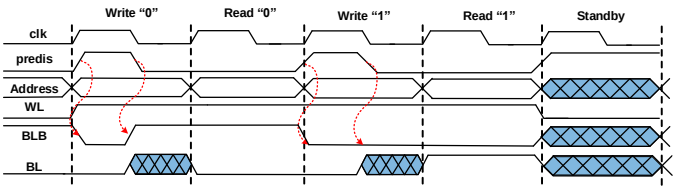

Fig. 4. SRAM operation timing diagram

state of the cell. Discharging the state of the cell also reduces the power consumption. Both access transistors M_{207} or M_{208} are turned on when a corresponding row address is selected. The control circuit then drives BLB to 1 or 0 during "Write 0" or "Write 1", respectively, while BL is released of the control. During a "Write 1" operation, M_{201}, M_{204}, and M_{205} are turned on, driving node Q high and node QB low. While during "Write 0" operation, M_{202} and M_{203} are on, giving nodes Q and QB a low and high value, respectively.

When the read operation is initiated, the control circuit releases control of the bitlines and turns on the sense amplifiers. The corresponding address are selected to access the states of the cells. When Q is high and QB is low, BL will be at a higher potential than BLB. Thus, when it is fed to the sense amplifier, it will generate a high output. The same is true for the inverse operation.

In both operations, VS (in Fig. 2) is set to low to turn on M_{209} to give a higher supply voltage to the cells.

2) Standby operation: Standby operation is entered when the cells are not being accessed. In this operation, VS is turned off and VSB is on thus giving a lower supply, VDD–Vthp, to the cells. By this way, the standby power of the cells are decreased. The access transistors M_{207} & M_{208} are turned off to disconnect the cells from the bitlines, preventing the access to any of the cells. Transistor M_{206} also prevents the cells to be flipped from 1 to 0, when Q drops due to noise or other external disturbance.

3) Cell Sizing: Eqns. (1), (2), and (3) are used to determine the sizes of the transistors in the cells [16]. The cell and pull-up ratios (CR and PR) are assigned a value of 1 to reduce the effects of NBTI (negative-bias temperature instability). The upper trip point (utp) of the ST inverter in Fig. 2 is set to 0.5 V, slightly higher than half of the supply. This is to have a better hold of the high logic value. The storage transistors in the cells are high-Vth devices which reduces the probability of a voltage flip in standby mode. The access transistors are chosen to be low-Vth devices to shorten the access time.

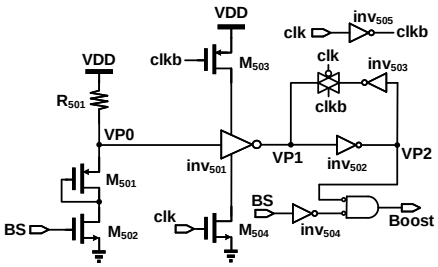

Fig. 5. Adaptive Voltage Select (AVS) circuit

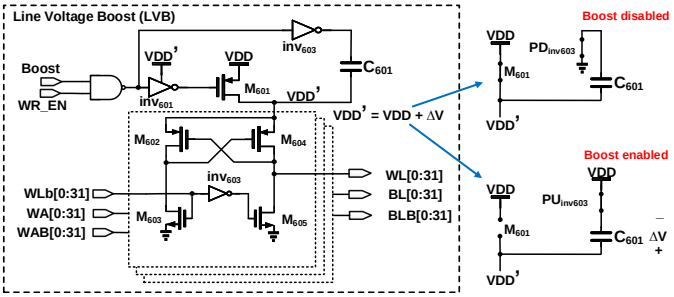

Fig. 6. Line Voltage Boost (LVB) circuit

$$PR = \left(\frac{W}{L}\right)_{M202} \div \left(\frac{W}{L}\right)_{M208} \tag{1}$$

$$CR = \left(\frac{W}{L}\right)_{M203} \div \left(\frac{W}{L}\right)_{M201} \tag{2}$$

$$\frac{\beta_1}{\beta_3} = \left(\frac{W}{L}\right)_{M205} \div \left(\frac{W}{L}\right)_{M206} = \left(\frac{V_{DD} - V_{utp}}{V_{utp} - V_{thn}}\right)^2 \tag{3}$$

C. Power Reduction and Speed Compensation Circuit

Power Reduction and Speed Compensation circuit is composed of three components as shown in Fig. 1, (1) Voltage Mode Select (VMS), (2) Adaptive Voltage Select (AVS), and Line Voltage Boost (LVB). This is meant to decrease the energy consumption of the SRAM as well as compensate for the speed drop when needed.

1) Voltage Mode Select (VMS): The VMS circuit is designed to give the cell a lower supply voltage during standby operation and a normal voltage during read or write operations. Referring to Fig. 2, the proposed SRAM cell is powered through the VMS circuit. The VMS selects the supply voltage being used in the column of the SRAM.

2) Adaptive Voltage Select (AVS): The adaptive voltage select (AVS) circuit is illustrated in Fig. 5. The AVS circuit is triggered when boost select (BS) is enabled driving node VP0 to ground through M_{501} and M_{502}. This will then drive node VP1 high and node VP2 low. The latch composed of inv_{502}, inv_{503}, and the transmission gate ensures that VP2 is low even when BS is not enabled. This then gives out the boost signal to the Line Voltage Boost (LVB) circuit.

3) Line Voltage Boost (LVB) Circuit: The Line Voltage Boost (LVB) circuit is shown in Fig. 6. When LVB is activated, the capacitor C_{601} is charge to a higher voltage equivalent to the voltage (ΔV) from the pull-up circuit of inv_{603}. When the boost circuit is disabled, M_{601} is turned on and the pull-down network (PD_{inv603}) of inv_{603} activates and charges up capacitor C_{601}. Upon enabling the boost circuit, M_{601} is then turned off and activating the pull-up network (PU_{inv603}) of inv_{603} providing a bitline and wordline voltages of VDD' = VDD + ΔV providing the speed boost to the circuit.

D. Memory Built-in Self-test (MBIST)

In order to ensure the SRAM reliability, a memory built-in self-test circuit is included in the design. Fig. 7(a) shows the block diagram of the MBIST circuit. It consists of a controller, pattern generator (PG), and an output response analyzer (ORA). The test patterns are generated by an LFSR circuit (linear feedback shift register), as shown in Fig. 7(b) and the corresponding polynomial is described in Eqn. (4). A simplified timing diagram of the MBIST is shown in Fig. 4. March C– algorithm is used since it performs better than other March algorithm, requiring 10 access per SRAM bits and detects more faults. The algorithm can detect transition faults (TF), stuck-at faults (SAF), neighborhood pattern sensitive faults (NPSF), coupling faults (CF), bridging faults (BF), and address decoder faults (ADF). The March C– algorithm is described using the notations in Eqn. (5) and Table I.

TABLE I
MARCH C– ALGORITHM NOTATIONS

Description	Notation
March element. Contains the operation needed.	( )
Write pattern 0 to SRAM	W0
Read SRAM, check if equal to pattern 0	R0
Write pattern 1	W1
Read SRAM, check if equal to pattern 1	R1
Increment address after operation	$\Uparrow$
Decrement address after operation	$\Downarrow$

*Pattern 0 and 1 are generated by the LFSR, they are inverse of each other

$$f(x) = 1 + x + x^3 + x^4 + x^5 \tag{4}$$

$$\begin{aligned}\{&\Uparrow (W0); \Uparrow (R0, W1); \Uparrow (R1, W0);\\ &\Downarrow (R0, W1); \Downarrow (R0, W1); \Downarrow (R0)\}\end{aligned} \tag{5}$$

III. SIMULATION AND MEASUREMENT ON SILICON

The proposed SRAM prototype is fabricated on silicon using TSMC 40-nm CMOS technology and packaged in a 32-pin dual-inline package (DIP) chip. Referring to Fig. 9, it shows the die photograph of the proposed 1-kb SRAM. The die is 595×595 μm^2 and the core is 249×212 μm^2. An all-PVT-corner post-layout simulation is performed for the design. Fig. 10(a) shows the worst corner Static Noise Margin (SNM) simulation at VDD = 0.8 V. The worst-case SNM is 608.11 mV. Fig. 10(b) shows the Dynamic Noise Margin (DNM) of the proposed cell showing that the cells could still operate even when a 0.3 V noise enters the wordline ensuring that the cells would not be easily flipped during hold operation. SNM for the supply variations from 0.3 V to 0.8 V is shown in Fig. 11 and is compared to recent proposed Schmitt-trigger

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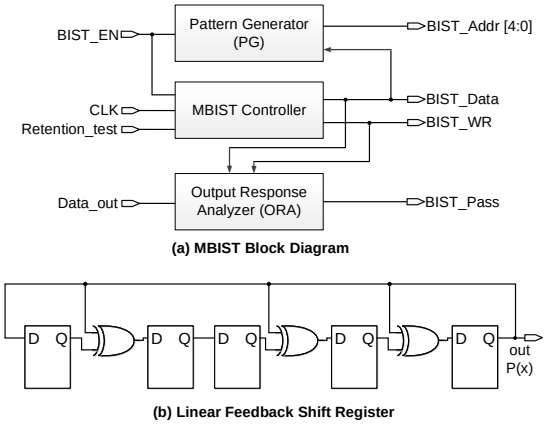

Fig. 7. Memory Built-in Self-test (MBIST)

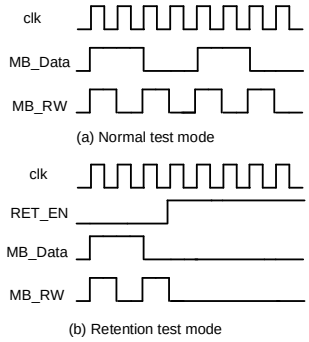

Fig. 8. MBIST Timing diagram

based SRAM cells. This shows that the cells can still operate at a VDD of 0.3 V. Ref. [10] has managed to have their cells work at 0.2 V supply, this could be because they are using an advanced 7-nm FinFET process.

Referring to Fig. 12, the measurement setup for the prototype chip is presented. Agilent E3631A is the power supply used. The input signals are generated using the Agilent 81250 function generator, and the outputs are measured using Keysight DSAV134A. The measurements are done for 6 chips measured 100 times each (at a clock rate of 100 MHz to 300 MHz at an increment of 10 MHz). Fig. 13 shows examples of the measurement result during normal operation and when the boost signal is enabled. It shows that when boost is enabled,

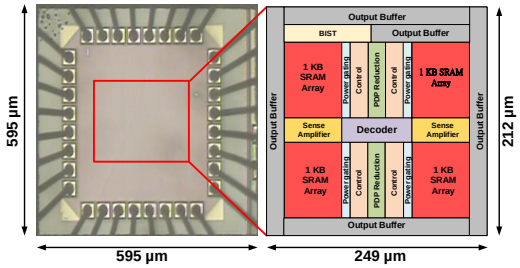

Fig. 9. Die photograph of the fabricated SRAM

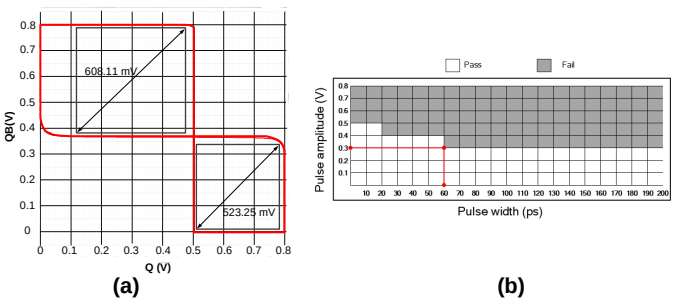

Fig. 10. Noise performance of the proposed SRAM cell, (a) Static Noise Margin (SNM); (b) Dynamic Noise Margin (DNM)

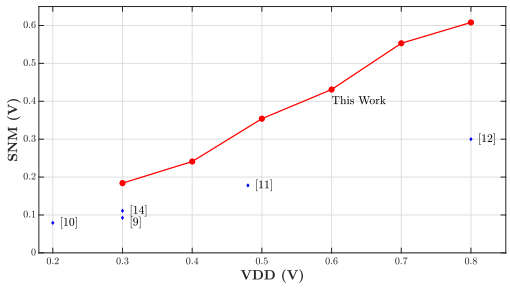

Fig. 11. SNM comparison with previous Schmitt-trigger SRAM cells

there is a significant improvement of the output delay, i.e., from 2.5 ns to 1.8 ns. It can also be observed that the output glitch during write-0 operation in Fig. 13(a) is removed when boost is enabled. Repeatability test, as shown in Fig. 14, presents the delay measurements during normal mode and when boost is enabled. The average delay during normal mode is 5.659 ns and 1.708 when the boost is enabled. This shows the reliability of the proposed design.

Table II presents a performance comparison with several prior SRAM designs that were implemented on silicon. The proposed SRAM achieved the best SNM when referred to the supply voltage due to the use of Schmitt-trigger cells. The proposed design has the best read PDP (power delay product) and energy per bit with values of 1.758 and 4.23 fJ, respectively at the cost of a slightly larger area.

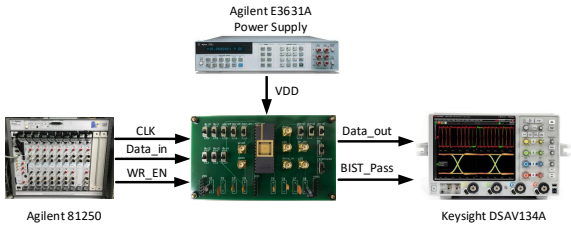

Fig. 12. Measurement setup for the prototype chip

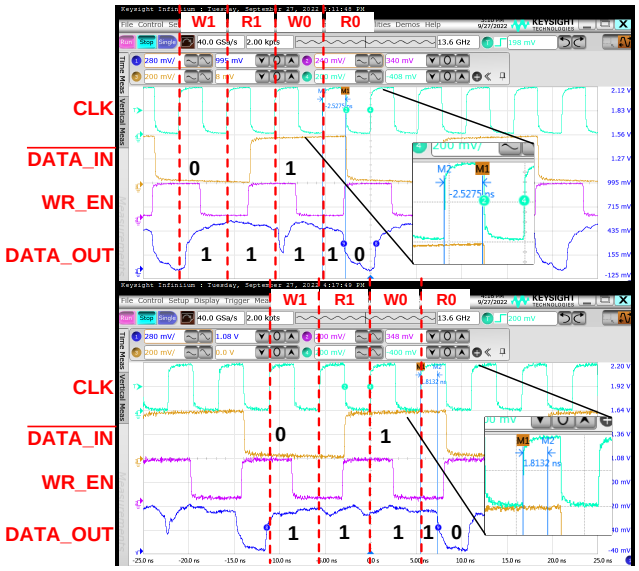

Fig. 13. Measurement results with (a) Boost disabled, and (b) Boost enabled

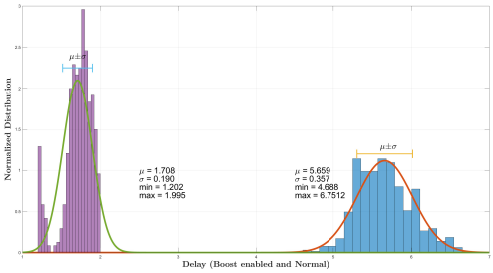

Fig. 14. Delay histogram (600 measurements)

IV. Conclusion

A very low power 1-kb SRAM is realized on silicon using asymmetrical cells. A combination of traditional and Schmitt-trigger inverters is used to improve the noise rejection capability of the SRAM. A power reduction circuit is used to improve energy consumption during standby operation through a voltage mode select circuit and a line voltage boost is added to improve the read and write delays. The proposed SRAM offered the lowest energy consumption operating at more than 100 MHz up to date.

TABLE II
Performance Comparison with Previous SRAM

	[17]	[18]	[5]	[4]	[6]	Ours
Year	2020	2021	2021	2021	2023	2023
Process (nm)	65	55	40	16	40	40
V_{DD}	0.36	1.2	0.9	0.8	0.8	0.8
Cell	8T	6T	6T	6T	6T	8T
Capacity (kb)	32	4	1	1	1	1
Word Size	128	32	32	32	32	32
Freq. (MHz)	0.25	935	200	500	10/2	210
SNM (mV)	0.19	N/A	0.38	0.5	0.41	**0.61**
Read PDP (pJ)	4454.4	233.4	47.4	2.7	2.1	**1.758**
En./access (pJ)	0.3	1.04	0.23	0.22	0.032	**0.163**
En./bit (fJ)	2.34	32.5	7.23	6.8	1.0/4.3	**4.23**

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