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A 2xVDD digital output buffer with gate driving stability and non-overlapping signaling control for slew-rate auto-adjustment using 16-nm FinFET CMOS process

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ABSTRACT

This paper presents a 2 × VDD mixed-voltage digital output buffer where its slew rate (SR) is automatically adjusted based on PVT (process, voltage, and temperature) detection. The developed buffer is the first to be fabricated using TSMC 16-nm CMOS Logic FinFET Compact (Shrink) LL ELK Cu 1P13 M process. Since slew rate is one of the major required parameters in many interfacing protocols, it is really hard to meet if the mixed-voltage output buffer is needed in FinFET processes. The major reason is the low VDD in these advanced processes. However, our buffer's SR is improved by implementing low threshold voltage (V_{th}) type of device for always-on driving transistors in the Output Stage, thereby increasing the output current. Moreover, since FinFET devices were used in the buffer, the stability of the gate drives of the said driving transistors must be ensured so that noise interference will be avoided. Lastly, the buffer's Timing Shifters used non-overlapping signaling control directly implemented at the transistor level to eliminate the errors caused by delay variations. Based on silicon measurement results, at a load capacitance of 20 pF, the said circuit can be operated at a maximum data rate of 250 MHz for both supply voltages of 0.8 and 1.6 V (namely external VDD or VDDIO), respectively. When the SR auto-adjustment is activated, the SR improvement is at least 49.2% and 37.5% for 0.8 and 1.6 V, respectively.

1. Introduction

FinFET, fabricated in 20-nm silicon on insulator (SOI) technology, was first reported in 1999 [1] as a three-dimensional, non-planar, self-aligned, and double-gate MOSFET. It challenges prior planar technologies as the transistor gate length is scaling down below 20 nm. Unlike in traditional planar CMOS where leakage degradation is an issue, it has a suppressed sub-threshold leakage current in its gate, since its gate capacitance is near the channel even though it has a lower channel impurity concentration. Due to its self-alignment, its parasitic resistance & capacitance and the length of its channel is reduced. This gives the FinFET many advantages such as operating in higher frequency and consuming lower power.

Several electronic systems used older CMOS processes, e.g., 180 nm [2–4], to operate at different higher power supplies such as 3.3 V or 1.8 V [2,3], 2 × VDD [5], and 2.5 V or 1.2 V. Since new nanoscale-based chips and systems are operating at lower supplies such as 1.5 V and 0.9 V, the interfacing communication between chips fabricated in legacy processes and chips fabricated in nano-CMOS processes is a serious issue. Though this issue can be resolved through the insertion of voltage level converters or translators, these extra devices consume larger area and higher power. With this, mixed-voltage I/O buffers fabricated in FinFET CMOS process is more preferred to implement communication between these two different processes [6–8].

In the design of mixed-voltage I/O buffers, one factor to be considered is slew rate (SR) besides the voltage level compatibility. The SR variation is a concern during the interfacing and communication between systems implemented in legacy processes and systems realized

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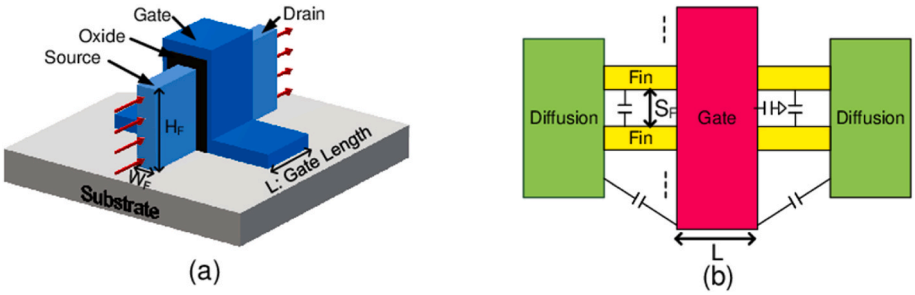

Fig. 1. FinFET structure: (a) 3D view, (b) top view.

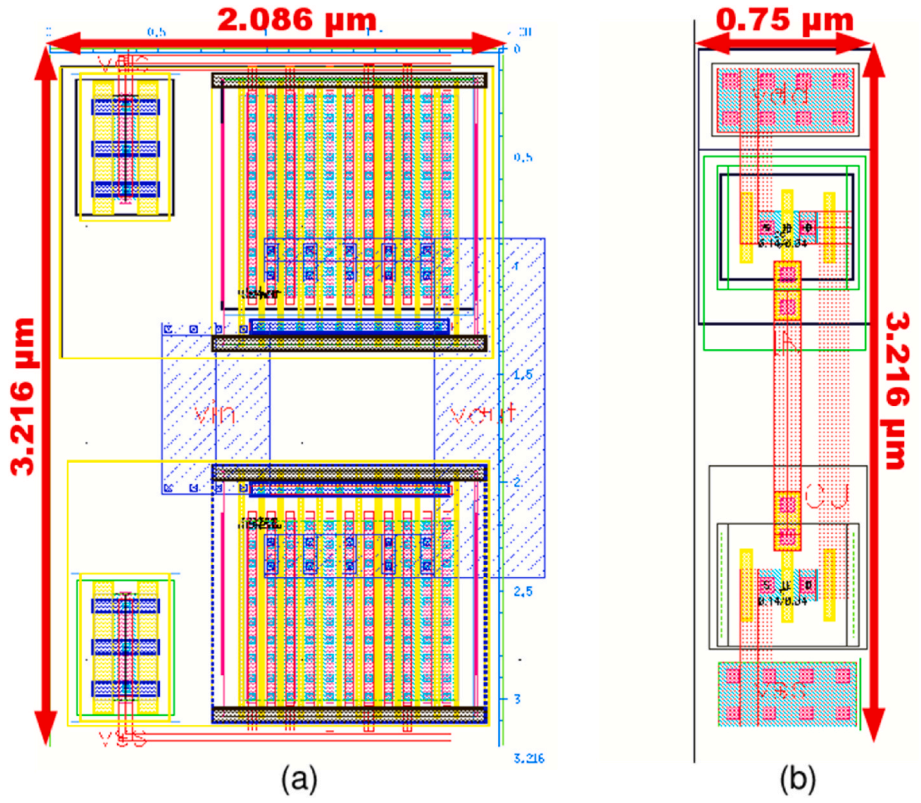

Fig. 2. Layout of the inverter implemented in (a) 16-nm FinFET process, (b) 40-nm planar CMOS process.

using advanced technologies such as FinFETs. The process, voltage, and temperature (PVT) variations affect the said SR stability. There have been attempts made to detect these PVT scenarios present in these I/O buffers for the correction and adjustment of SR [9,10], but they only managed to detect 3 corners (FF, SS, and TT). Moreover, their techniques make the settling time longer and the SR worse due to the missing corners. Also, for the current PVT scenario to be detected, multiple clock cycles are required by the said methods [9]. Another process detector [11] implemented digitally achieved a better detection and faster data rate with the trade-off of larger area and higher power consumption.

Based on prior reports and the above-mentioned problems stated, none of these have focused on the design and development of mixed-voltage output buffers which are implemented using FinFET process. In this paper, a 2 × VDD digital output buffer which operates at two voltage modes of 0.8 V and 1.6 V was realized and fabricated using TSMC 16-nm CMOS Logic FinFET Compact (Shrink) LL ELK Cu 1P13 M process. 0.8 V is the nominal power supply voltage or internal VDD (VDD or VDD_{int}), while 1.6 V is the I/O voltage or external VDD (VDD_{ext} or VDDIO). On-silicon measurement results justify the feasibility and the performance.

2. FinFET design basics

Fig. 1 (a) and (b) show the 3D and top views of FinFET, respectively. During saturation, the drain current (ID) equation was can be stated as [12,13].

$$I_D = \frac{W_{eff}}{L} \cdot \mu_s \cdot C_{ox} \cdot \left[\left(V_{gs} - V_{th} \right)^2 - 8 r V_{kT}^2 e^{\frac{V_{gs} - V_0 - V_{ds}}{V_{kT}}} \right] \tag{1}$$

$$W_{eff} = M \cdot N_F \cdot (2H_F + W_F) \tag{2}$$

$$r = \frac{\varepsilon_{Si} \cdot T_{ox}}{\varepsilon_{ox} \cdot W_F} \tag{3}$$

$$V_0 = V_{fb} + 2 v_{kT} \ln \left(\frac{2}{W_F} \sqrt{\frac{2 \varepsilon_{Si} \cdot v_{kT}}{q \cdot n_i}} \right) \tag{4}$$

where W_{eff} is the effective or total FinFET width, L is the FinFET gate length, μ_s is the FinFET's surface mobility of inversion carriers, C_{ox} is oxide capacitance, V_{gs} is the gate-source voltage, V_{th} is the threshold voltage, v_{kT} is the thermal voltage, V_{ds} is the drain-source voltage, M is

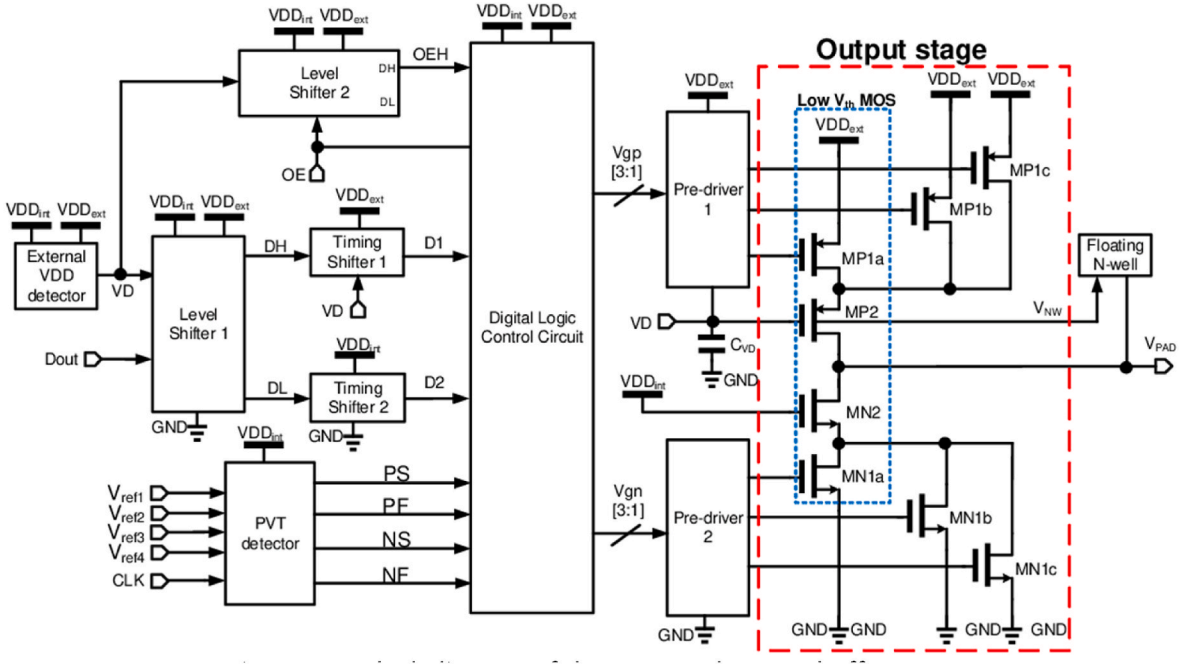

Fig. 3. Block diagram of the proposed output buffer.

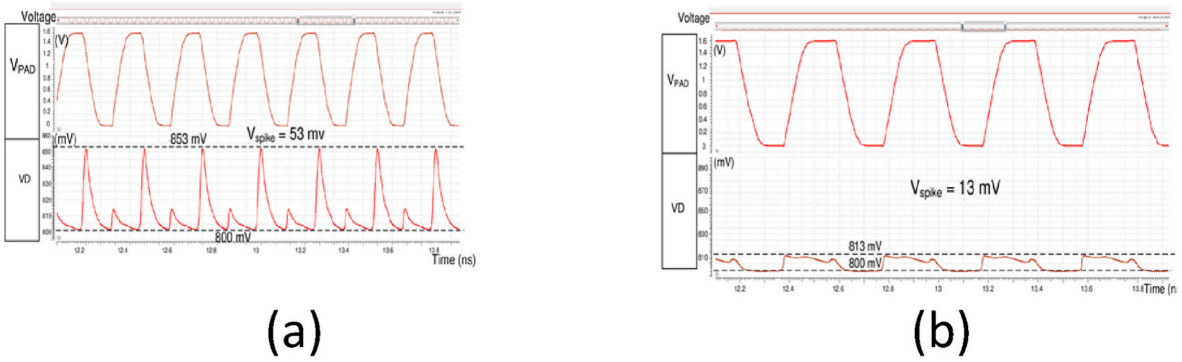

Fig. 4. Spikes in VD at MP2's gate (a) no CVD; (b) with CVD.

the number of gate multipliers or fingers, N_F is the number of fins, H_F is the fin height, W_F is the fin width or fin thickness, ε_{Si} is the permittivity of silicon, T_{ox} is gate oxide thickness, ε_{ox} is the oxide permittivity, V_{fb} is the flatband voltage of the silicon body, q is the electron charge, and n_i is the intrinsic carrier concentration.

Assuming $8rV_{kT}{}^2 e^{\frac{V_{gs}-V_0-V_{ds}}{v_{kT}}}$ is small, Eqn. (1) turns into Eqn. (5):

$$I_D = \frac{W_{eff}}{L} \cdot \mu_s \cdot C_{ox} \cdot \left(V_{gs} - V_{th}\right)^2 \tag{5}$$

By Eqn. (5), it is possible to derive an approximation of the FinFET's equivalent switching resistance for digital circuit implementation by getting the reciprocal slope of the line in the I–V curve that goes from Vds = VDD to Vds = 0 as shown in Eqn. (6).

$$R_n = \frac{VDD}{\mu_s \cdot C_{ox} \cdot \frac{W_{eff}}{L} \cdot (VDD - V_{th})^2} \tag{6}$$

The limit for the N_F to be adjusted in FinFET design is quite small. Usually, when N_F is exceeded, the M can be increased instead until the maximum effective width depending on the FinFET process used is reached. This is seen from the comparison of the inverter layouts implemented in 16-nm FinFET and 40-nm planar CMOS processes as shown in Fig. 2 (a) and (b), respectively. If the FinFET inverter is implemented with the maximum number of fins, the inverter's cell height becomes fixed. In turn, to increase the effective width, the fingers shall be increased.

3. System architecture of the 2xVDD digital output buffer using FinFET CMOS

Fig. 3 shows the block diagram of the proposed mixed-voltage output buffer consisting of Output stage, Floating N-well, External VDD detector, two Level Shifters, two Timing Shifters, two Pre-driver circuits, PVT detector, and Digital Logic Control Circuit (see Fig. 4).

3.1. Output stage

Fig. 3 shows the Output Stage where stacked transistors MP1a, MN1a, MP2, and MN2 are implemented for transistors' over-voltage prevention at a condition where VDDext is higher than VDD_{int}. To prevent fluctuations of the output current, the said stacked transistors should always be turned on. Notably, FinFET devices are different from planar devices such that the current is directly related to the numbers of

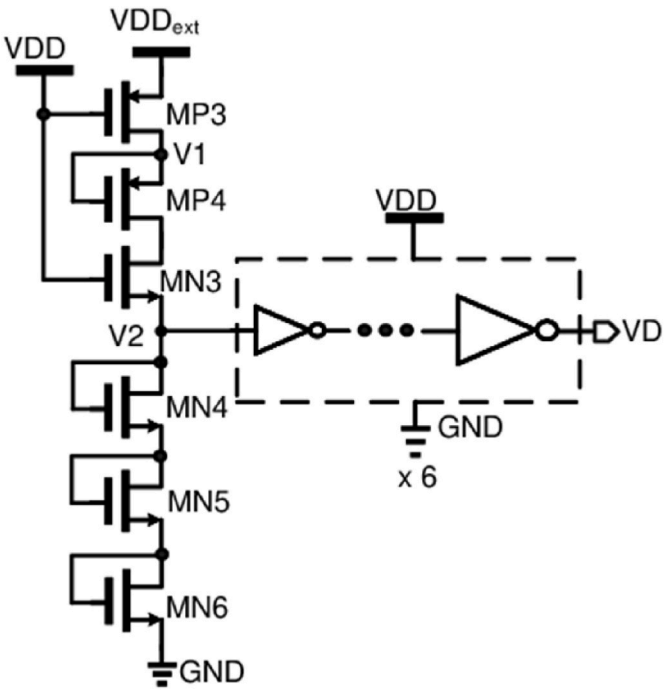

Fig. 5. VDDext detector circuit.

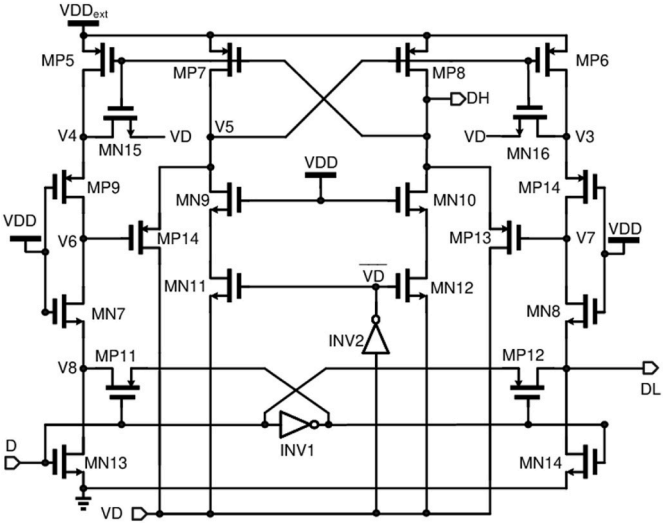

Fig. 6. Level Shifter circuit.

Table 1
Level Shifters' truth table.

VDD_{ext} (V)	VD (V)	D (V)	DH (V)	DL (V)
1.6	0.8	0/0.8	0.8/1.6	0/0.8
0.8	0	0/0.8	0/0.8	0/0.8

fins rather than the usual random channel width in planar transistors. Since the stacked transistors are always on, low-threshold voltage (V_{th}) FinFET devices were used to reduce the turn-on resistance. Lastly, the Output Stage transistors are sized and optimized for the load capacitance of 20 pF to conform with the outcome provided by real measurements [14].

In addition, the gate drives' stability of the always-on transistors is a serious concern. High stability of transistor MN2 is ensured since the

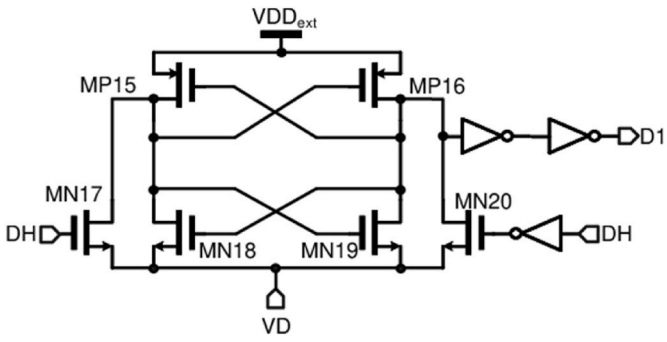

Fig. 7. Timing Shifter circuit for VDDext.

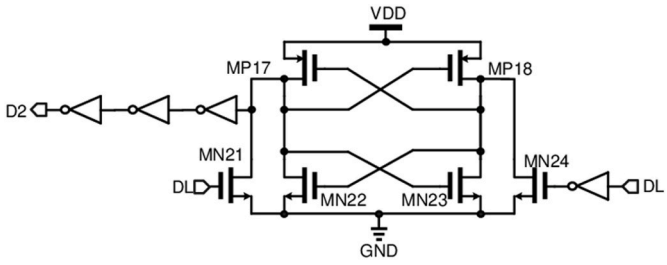

Fig. 8. Timing Shifter circuit for (VDDint).

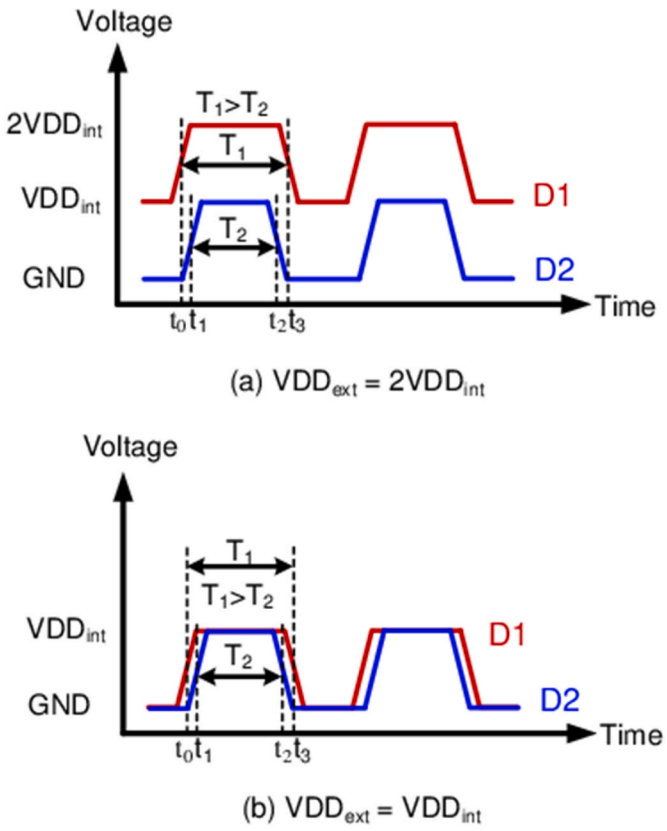

Fig. 9. The gate control timing diagram of Output Stage transistor, MP1a, MN1A. (a) VDDext = 2 · VDDint; (b) VDDext = VDDint.

device is turned on by VDDint. Pre-drivers 1 and 2 are designed for high stability to further drive MP1a and MN1a, respectively, based on the result of the PVT detection made by the PVT detector. Lastly, to further improve the stability of the gate drive of MP2, a capacitor CVD is added

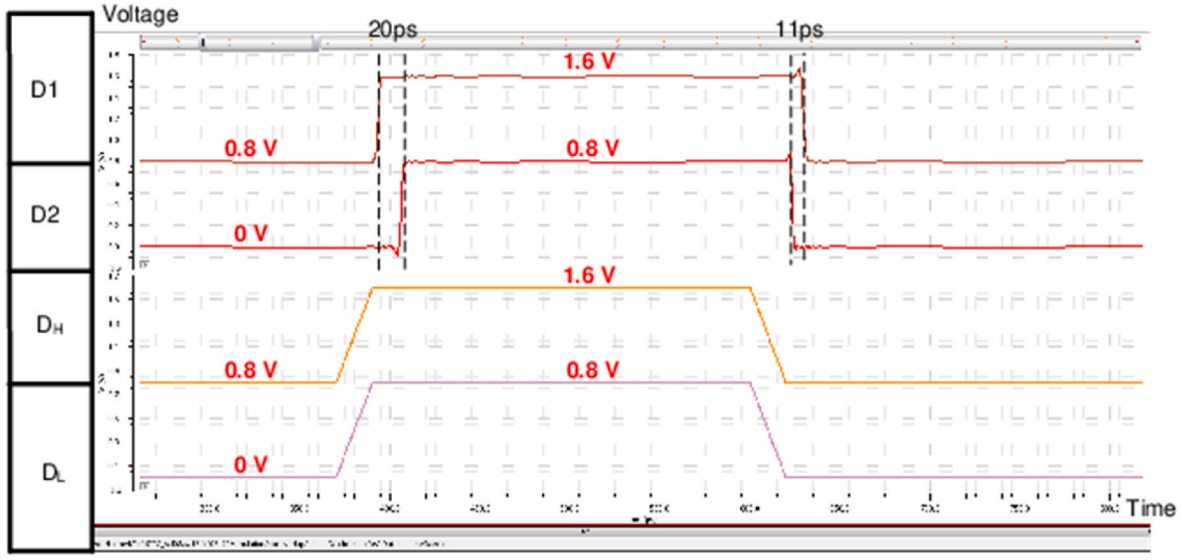

Fig. 10. Timing Shifter's non-overlapping of timing signals.

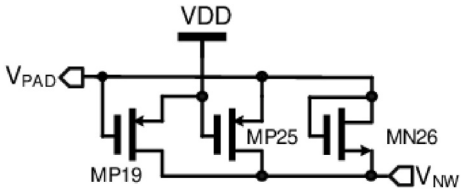

Fig. 11. Floating N-Well circuit.

for the rejection of the coupled noise (as shown in Fig. 3) at VD which might be generated by the External VDD Detector. The capacitor is sized to a minimum value such that the spikes shown in Fig. 3 are suppressed.

On the other hand, transistors MP1b and MP1c will be based on the corresponding PVT Detector's detected corner value. The PVT Detector detects these corners to determine if driving current and the rising edge's SR are needed to be increased. Similarly, to increase the falling edge's SR, transistors MN1b and MN1c are driven to sink more current. Finally, high-threshold voltage (Vth) FinFET devices were used for the said 4 transistors to prevent the leakage current which will be present once these devices are switched off.

Referring to Fig. 3, when Dout is low to high, MN1a, MN1b, MN1c, and MN2 are all turned off, and then MP1a, MP1b, MP1c, MP2 are turned on to charge VPAD to 2 × VDD. On the contrary, when Dout is high to low, MP1a, MP1b, MP1c, MP2 are turned off while MN1a, MN1b, MN1c, and MN2 are turned on to discharge VPAD to 0 V.

3.2. External VDD detector

As shown in Fig. 5, the External VDD (VDD_{ext}) detector in Fig. 3 uses a single-string, diode-connected structure and driving buffers to reduce the area unlike in the similar Vg2 generator reported in Ref. [15]. Since $VDD_{ext} = 2 \times VDD$, to avoid over-voltage of the transistor, an appropriate bias voltage VD must be provided. In addition, since the VD needs to be provided to Output Stage, Level Shifters 1 and 2, Timing Shifters 1 and 2, and Pre-driver 1, it is necessary to add an additional buffer to make the VD reach the full swing and increase the driving current.

Referring again to Fig. 5, when $VDD_{ext} = 2 \times VDD$, MP3 will be turned on, MP4 will lower the voltage of V1 so that the lower transistors will not reach over-voltage. MN4, MN5, MN6 will be turned on so that V2 is higher than the transition point of the following buffer, and a stable output VD is obtained (0.8 V). When $VDD_{ext} = VDD$, MP3 will be cut-off,

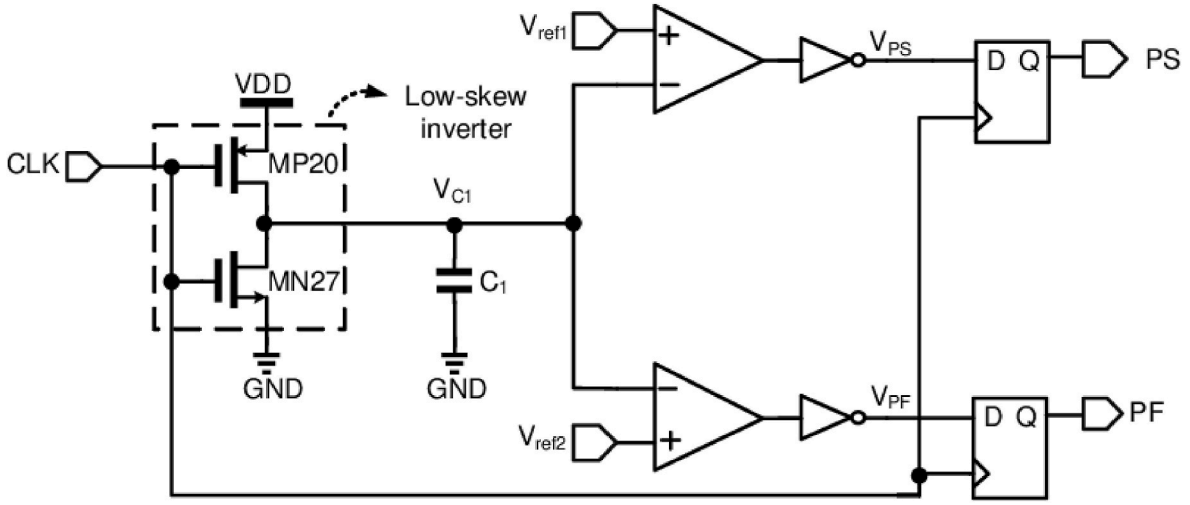

Fig. 12. P-type PVT detector.

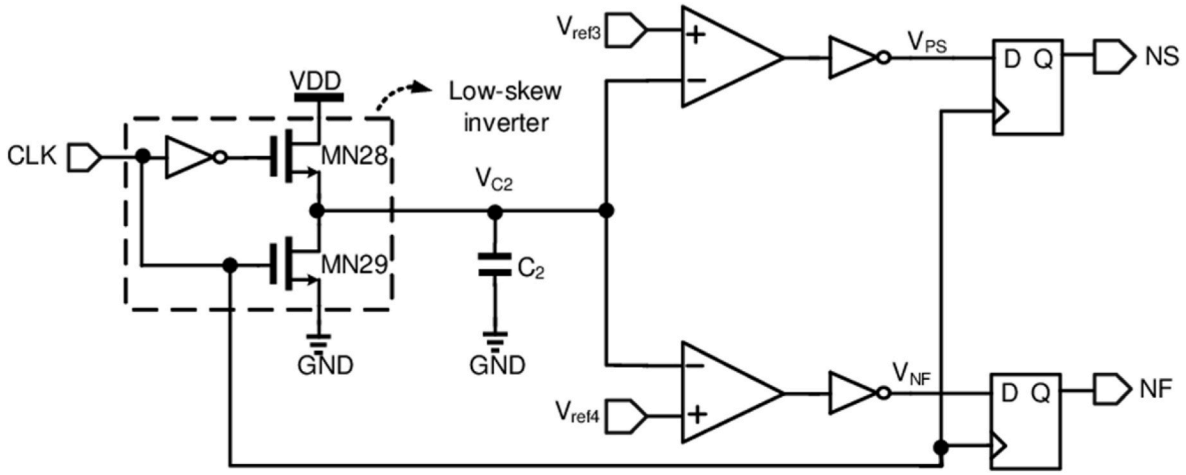

Fig. 13. N-type PVT detector.

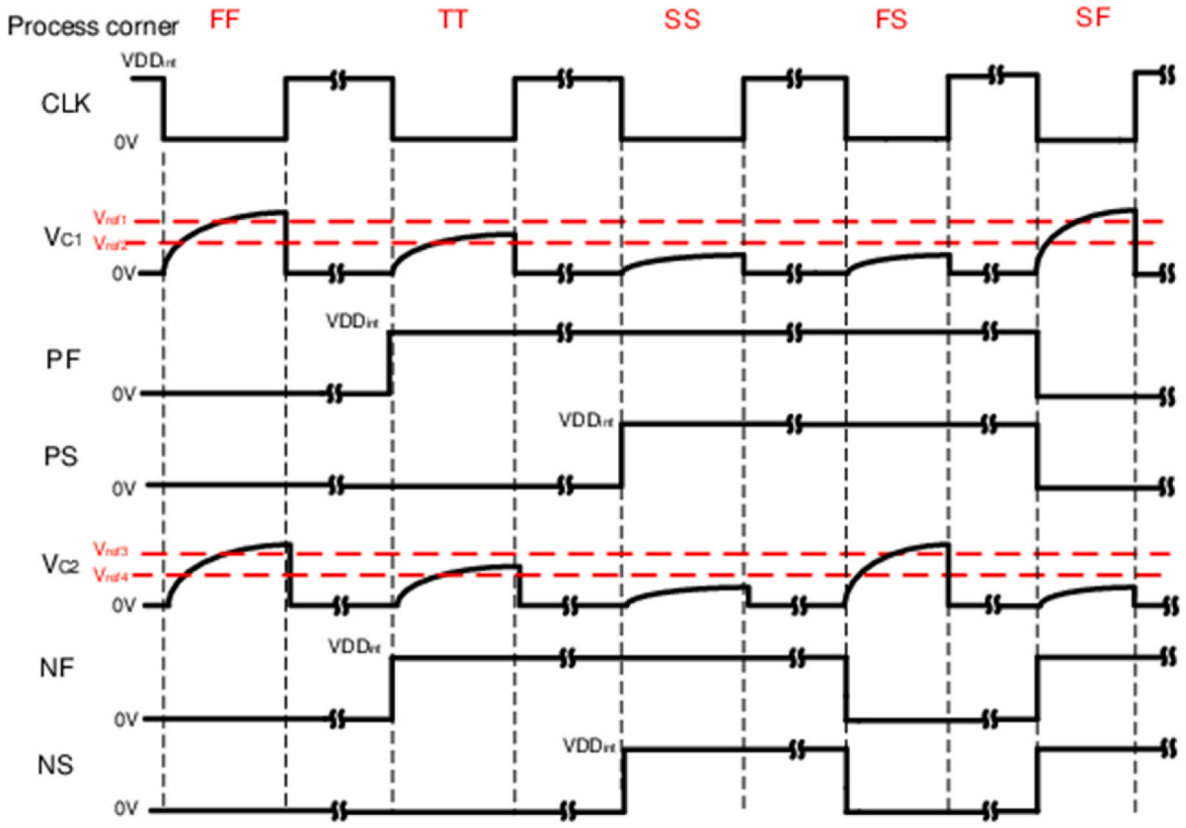

Fig. 14. Timing diagram of the PVT Detector.

causing the following circuits to be cut-off, making V2 approximately equal to 0 V, and through the buffer, a generating stable output VD = 0 V.

3.3. Level Shifters (LS)

Fig. 6 shows the Level Shifters (Level Shifters 1 and 2) in Fig. 3, which use a symmetrical type. Since VDD_{ext} can be 2 × VDD or VDD, an LS is needed to provide proper bias to MP1a, MP1b, and MP1c of the Output Stage. When VDDIO = 2 × VDD and VD = VDD, D controls MN13-14 and MP11-12, and cross-coupling transistors MP7-8 output the signal DH from voltage level VDD to 2 × VDD. When VDD_{ext} = VDD and VD = 0 V, VD through the inverter controls MN11-12, and cross-coupling transistors MP7-8 generated the signal DH from the output voltage level 0 V to VDD. Table 1 shows the Level Shifters' truth table. Like the Output Stage, MN15-16 and MP11-12 are auxiliary transistors, which assist V3–V8 and DL to charge and discharge to appropriate potentials during the transition period of the transistor to avoid overvoltage in the transistor. Therefore, the LS can output high and low level signals (DH and DL) at the same time.

Notably, this circuit is modified from the voltage level converter reported by Ref. [16], which has the advantage of avoiding a sudden overstress issue. However, the difference is their auxiliary transistors, $M_{p18\text{-}21}$, are removed in our new Level Shifter circuit. Instead of using

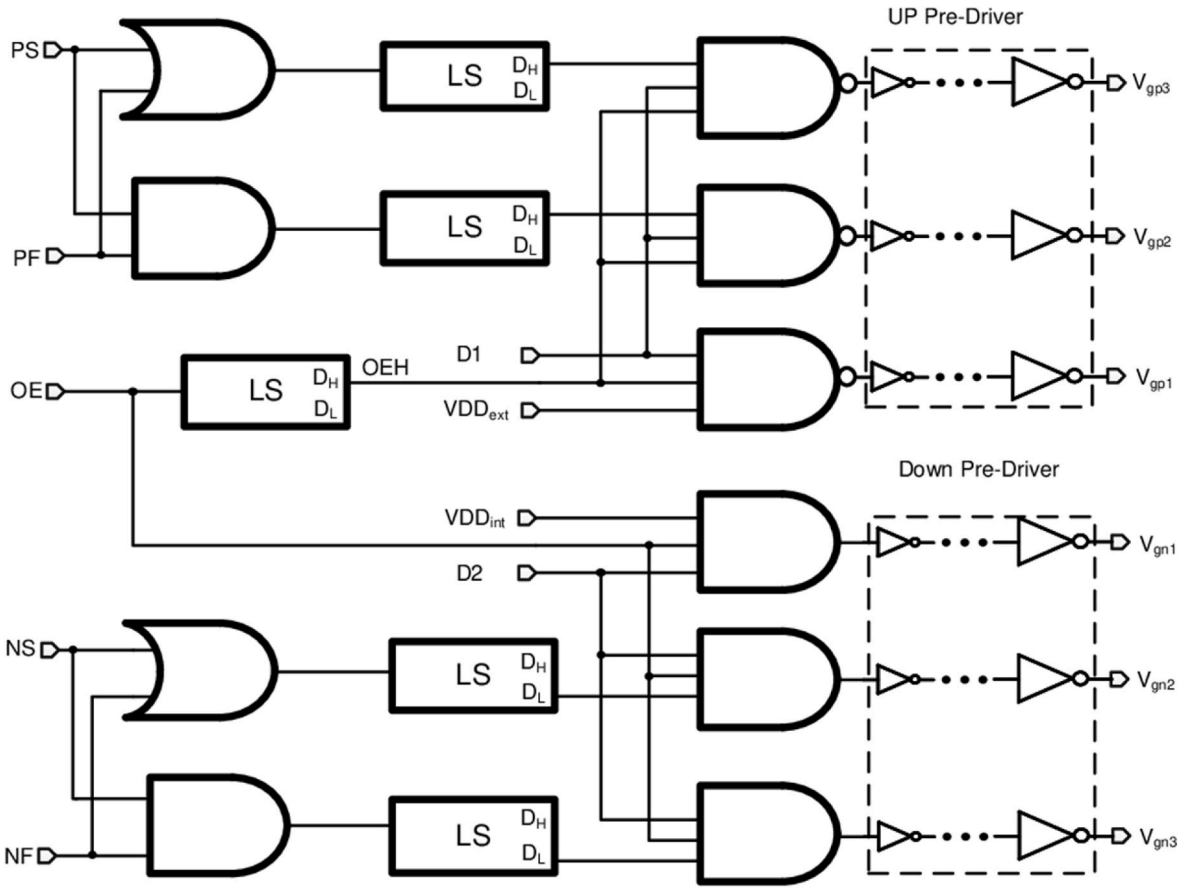

Fig. 15. Digital Logic Control circuit.

Table 2
Digital Logic Control circuit's truth table for P-type Output Stage.

OEH	PS	PF	D1	V_{gp1}	V_{gp2}	V_{gp3}
0	x	x	x	1	1	1
1	0	0	1/0	1/0	1	1
1	0	1	1/0	1/0	1/0	1
1	1	1	1/0	1/0	1/0	1/0

Table 3
Digital Logic Control circuit's truth table for N-type Output Stage.

OEH	PS	PF	D1	V_{gp1}	V_{gp2}	V_{gp3}
0	x	x	x	0	0	0
1	0	0	1/0	1/0	0	0
1	0	1	1/0	1/0	1/0	0
1	1	1	1/0	1/0	1/0	1/0

the said auxiliary transistors to successfully drive voltages V3, V4, and V8 in Fig. 6, MN15 and MN16's sources (M_{n7} and M_{n8} in Ref. [16], respectively) are now directly connected to VD, thus decreasing the transistor count.

3.4. Timing Shifter circuit

To prevent over-voltage during the transition of the transistor, Timing Shifter circuits as shown in Figs. 7 and 8 are used to make transistors MP1a, MP1b, MP1c and MN1a, MN1b, and MN1c of the Output Stage not turn on at the same time during the transition. The architecture used is composed of transistors instead of traditional logic gates, which can increase the transmission speed. Since VDD_{ext} can be equal to 2 × VDD or VDD, two different Timing Shifter circuits are required for VDD_{ext} and VDD_{int} as shown in Figs. 7 and 8. The highest and lowest potentials of Timing Shifter's outputs, D1 and D2, are the voltage levels of inputs, DH and DL, respectively.

Referring to Fig. 3, D1 and D2 will send a signal to the Output Stage transistors, MP1A and MN1A, through the Digital Logic Control circuit. As shown in the Timing Shifter's timing diagram in Fig. 9, when the signal is rising, D1 will boost the voltage to VDDint and double VDD_{int} first. Then, the Output Stage P-type transistor (MP1A) is turned off. Afterwards, D2 rises to VDD_{int} such that the Output Stage N-type transistor (MN1A) is turned on. On the other hand, D2 will drop to low first, and then MN1A transistor is turned off. D2 will drop to VDD_{int}, and MP1A transistor is turned on. By controlling the clock duty cycle, the short-circuit current issue can be reduced. Fig. 10 shows the magnitudes and the non-overlapping feature of timing signals of the Timing Shifter circuits. Time Shifters adjust the duty cycle of D1 and D2. The rising edge of D1 turns 20 ps earlier than that of D2, and the falling edge of D1 turns 11 ps later than that of D2.

3.5. Floating N-well

In either transmission or reception mode, V_{PAD} may have two voltages, VDD or 2 × VDD. Hence, a Floating N-well circuit [16], which utilized only 3 devices unlike prior floating n-well circuits [17,18], is needed as shown in Fig. 11. When VPAD receives 2 × VDD, it is necessary to prevent the P+/N-well parasitic diode of MP2 from causing leakage current paths due to the device's drain-bulk voltage (V_{db}) which is greater than its V_{th}. Therefore, the bulk of MP2 must not be connected to the source. Instead, it needs to be connected to a specific potential, V_{NW}.

Regardless of the transmission or reception mode, when V_{PAD} is 0 V,

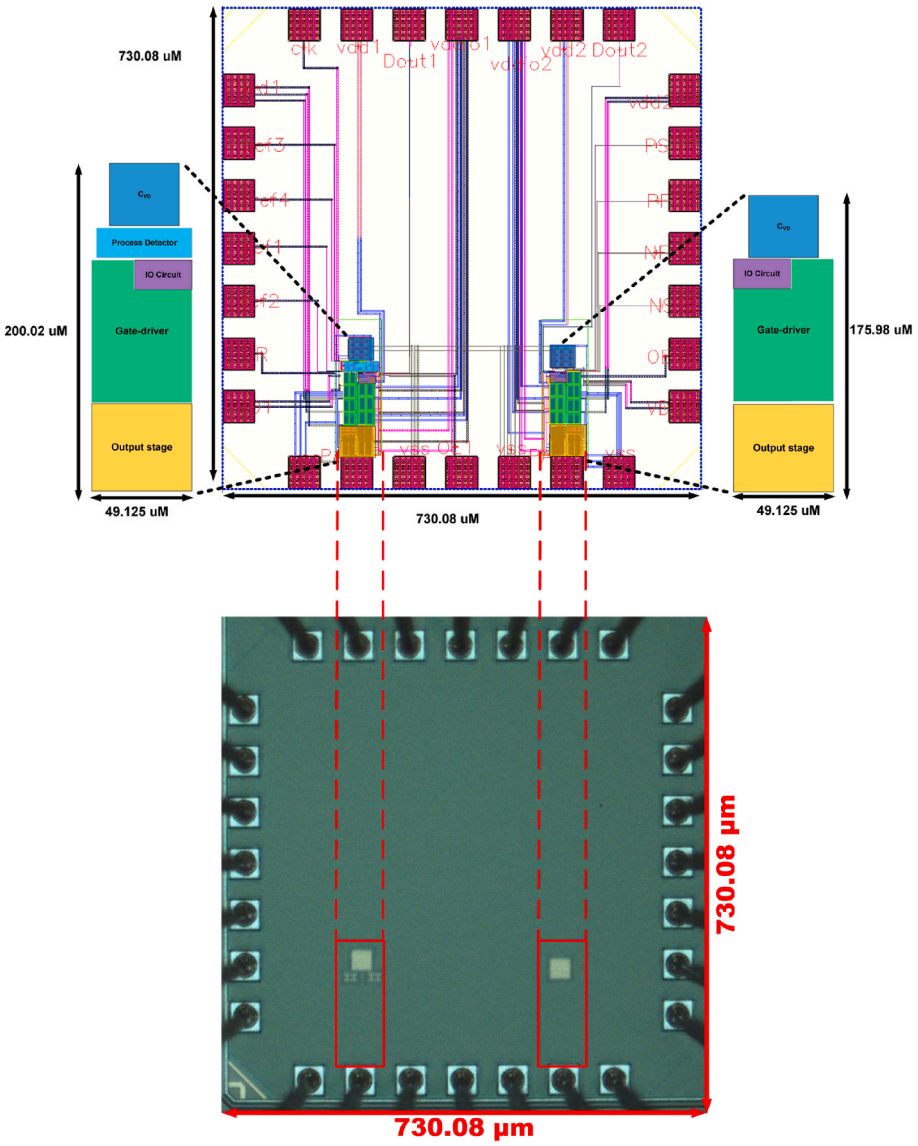

Fig. 16. The proposed output buffer's layout and die micrograph.

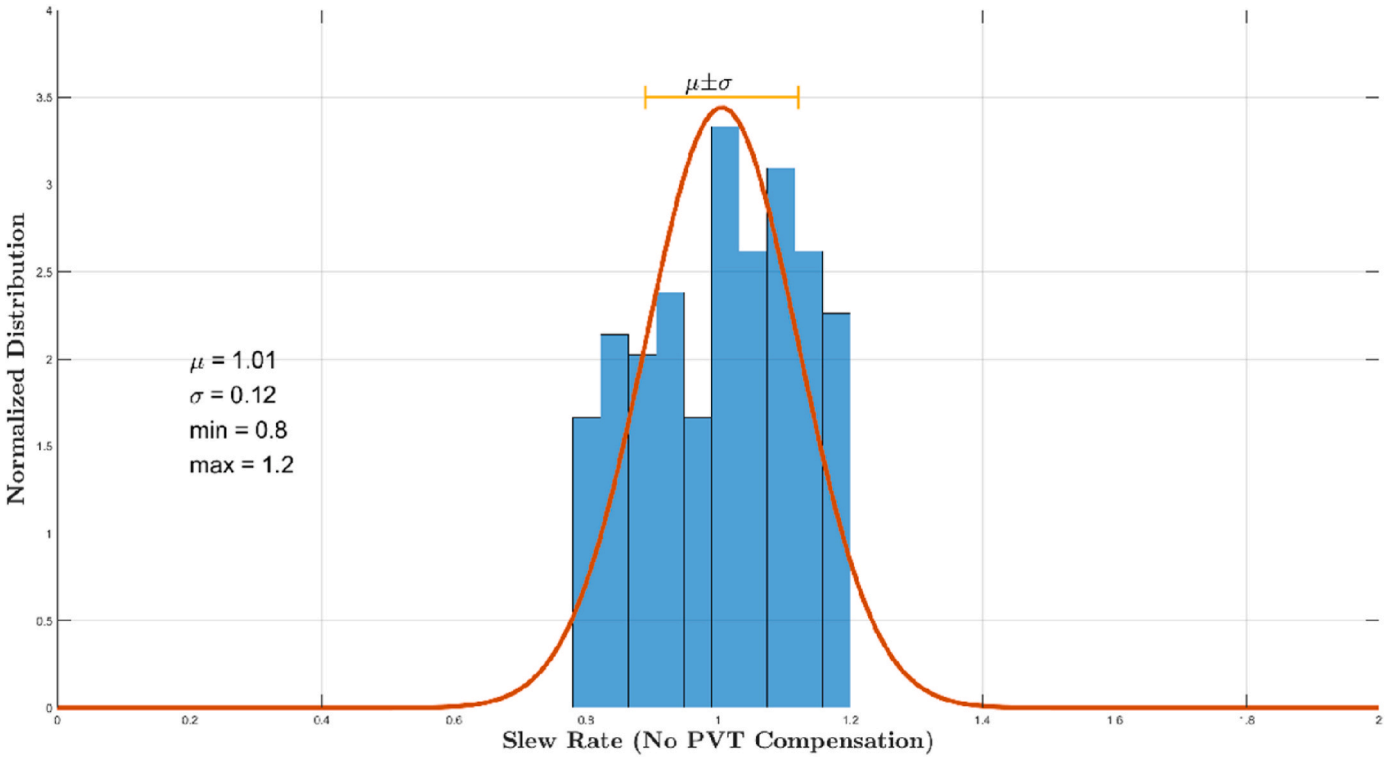

Fig. 17. Monte Carlo simulations of the output buffer's slew rate without PVT detection.

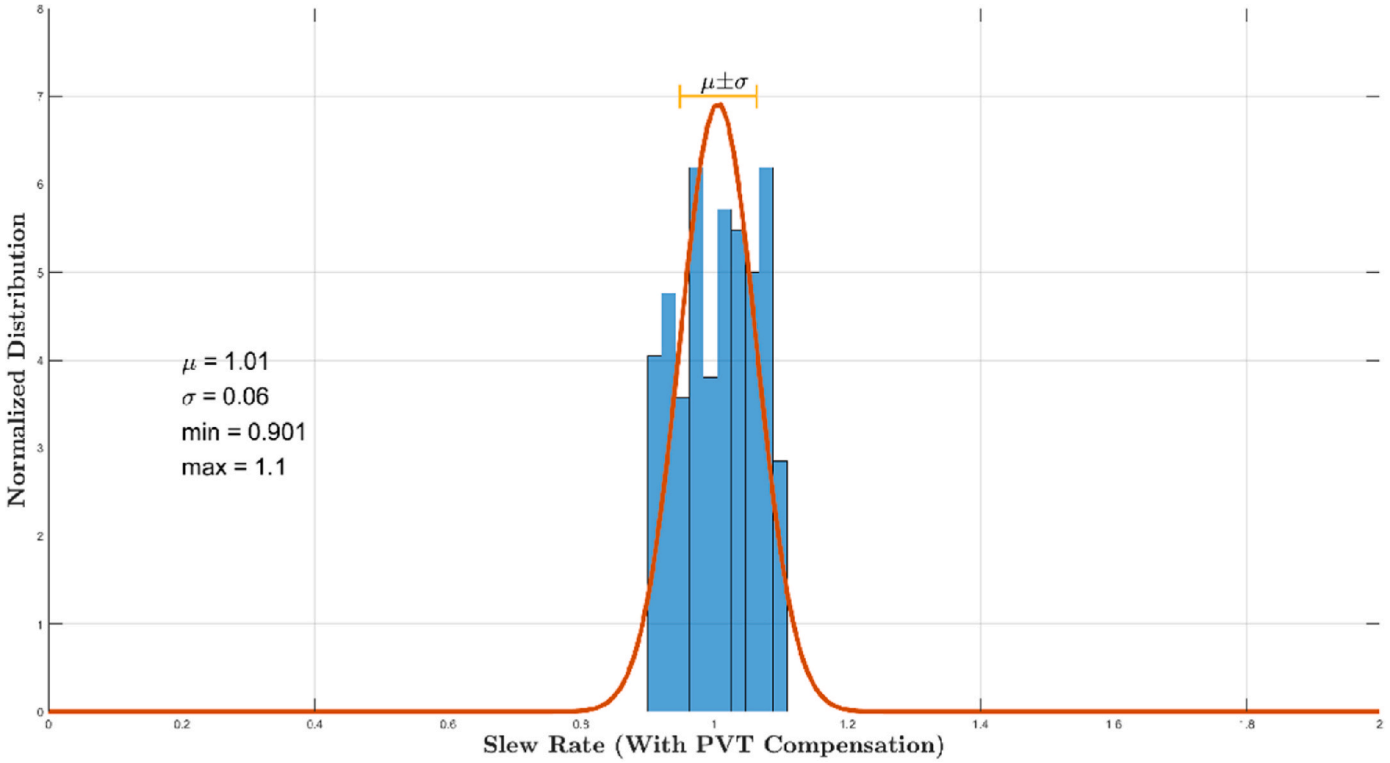

Fig. 18. Monte Carlo simulations of the output buffer's slew rate with PVT detection.

there will be no leakage current path at this time. When V_{PAD} is VDD, because MN17 has a voltage drop so that V_{NW} = VDD - V_{th}, the Vdb of MP2 is less than the Vth of MP2. The V_{th} of the diode closes the leakage current path of MP2. Meanwhile, when V_{PAD} is 2 × VDD, MP18 is turned on so that V_{NW} = 2 × VDD. At this time, the parasitic diode of MP2 is off, so there will be no leakage current path.

3.6. PVT detector

Since the process drift has five corners: TT, FF, SS, FS, and SF, PVT

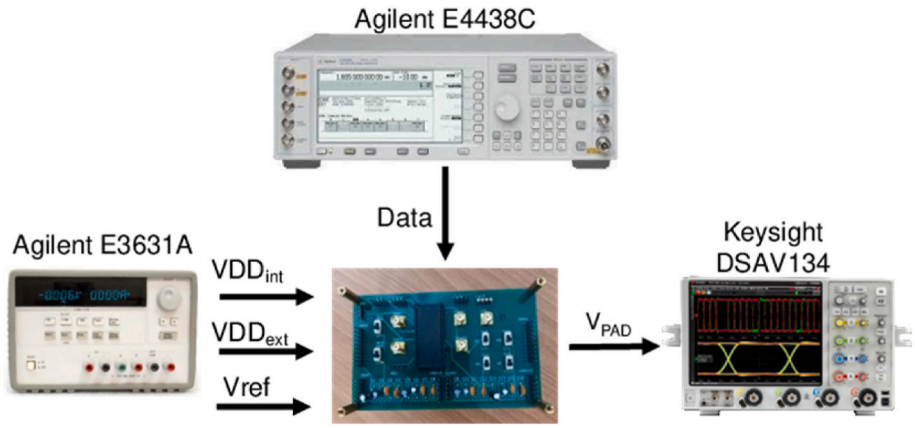

Fig. 19. Measurement setup for the proposed output buffer.

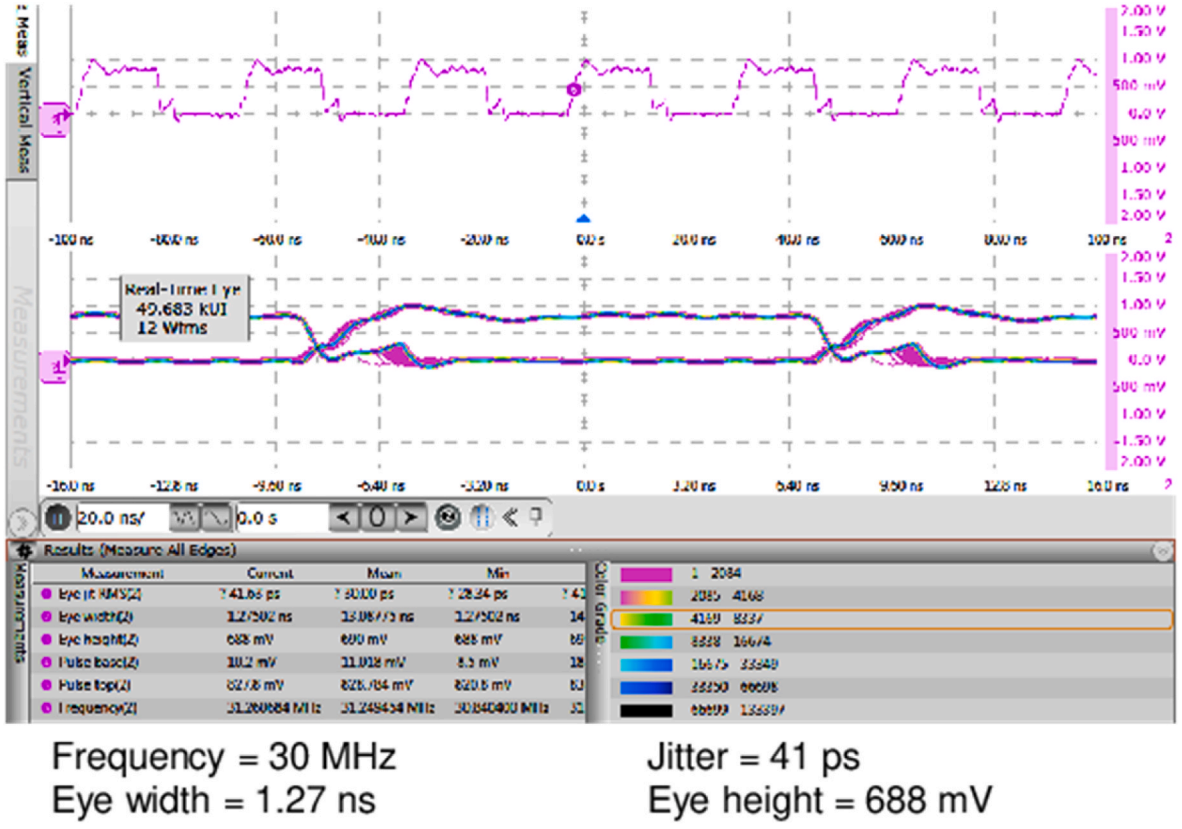

Fig. 20. Output waveform at VDD_{ext} = 0.8 V without PVT detection.

detectors are classified into two types: P-type PVT detector (Fig. 12) and N-type PVT detector (Fig. 13) detecting PMOS and NMOS corners, respectively. The topology of these PVT detectors was referred to Ref. [15], since this topology can detect the process variations easily through the charging of capacitors C_1 and C_2. In the said topology, fast and slow corners can be easily detected if the capacitors are charged faster and slower, respectively. One prior work implemented logic gate strings of delay units consisting of 2 cascaded inverters [19]. This method can hardly detect process variations, if the delay is the only factor to be considered. Both are composed of a set of low-distortion inverters with a MOS capacitor, and two sets of voltage comparators, inverters and flip-flops. The low-distortion inverters are composed of an inverter of minimum width. A PMOS with a lower aspect ratio and an NMOS with a higher aspect ratio are designed so that the charging speed is lower than the discharging speed.

The detection principle is to input a clock with a duty cycle of 50%. Referring to Figs. 12 and 13, when the clock is triggered by a negative edge, transistors MP20 and MN28 are turned on so that a current slowly charges the capacitor. When the temperature is changed, the MOS capacitor value will change. When the voltage corner changes, the charging current will also change. At this time, V_{c1} and V_{c2} will be sent to the comparator to compare with V_{ref1}, V_{ref2}, V_{ref3}, and V_{ref4}. Finally, the flip-flop captures the output of the comparator when the positive edge of the clock is triggered, and discharges V_{c1} and V_{c2} to 0 V through MN27 and MN29, so that the corners of the overall circuit can be periodically detected.

When the corner is located in a faster process or at a low temperature, the equivalent capacitance values of MN27 and MN29 will

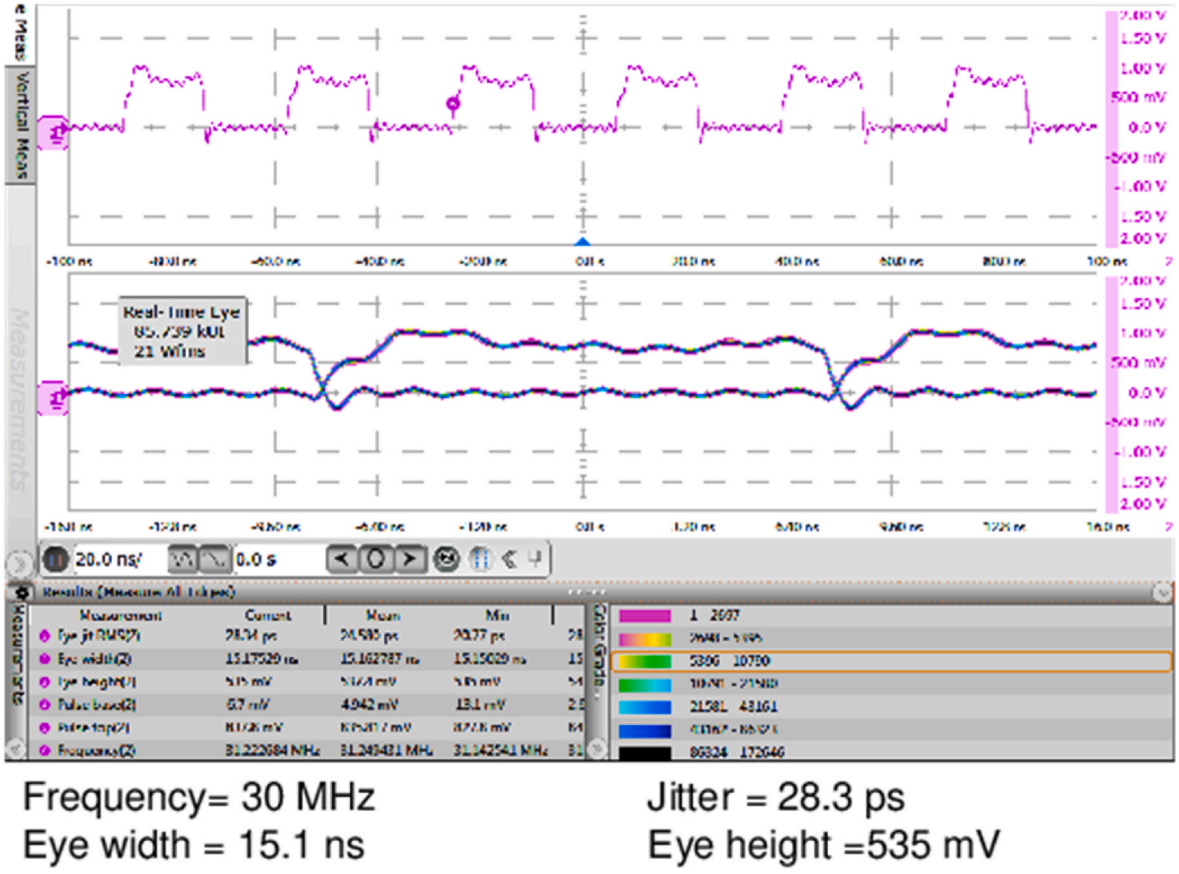

Fig. 21. Output waveform at VDD_{ext} = 0.8 V with PVT detection.

decrease, which will cause the charging voltage value of V_{c1} and V_{c2} to rise when the clock is triggered. On the contrary, when the corner is equivalent to a slower manufacturing process or corners of higher temperature, the equivalent capacitance values of MN27 and MN29 will increase, causing V_{c1} and V_{c2} to decrease. When the corner of the power supply voltage is at VDD+10%, the charging current of MN27 and MN29 will increase, so V_{c1} and V_{c2} will also increase. Conversely, when the corner of the power supply voltage is at VDD-10%, V_{c1} and V_{c2} will decrease.

When outputs PS and PF are high, it means that the V_{c1} is greater than the reference voltage when the positive edge is triggered, i.e., the corner is located in the fast process, VDD+10%, and low temperature (referred to as "Fast"). At this time, the charging current of the Output Stage should be lowered. For the charging current, the compensation transistors MP1b and MP1c are turned off based on the corner of the overall circuit. On the contrary, when the outputs PS and PF are low, it means that V_{c1} is less than the reference voltage, i.e., the corner is in the slow process, VDD-10%, and high temperature (referred to as "Slow"). At this time, the charging current of the Output Stage should be increased, and the compensation transistors MP1b and MP1c should be turned on based on the corner of the overall circuit.

When outputs NS and NF are high, it means that V_{c2} is greater than the reference voltage, i.e., the corner is at "Fast". At this time, the discharge current of the Output Stage should be lowered, and the compensation transistors MN1b and MN1c should be turned off based on the corner of the overall circuit. Conversely, when the outputs NS and NF are low, it means that the V_{c2} when the positive edge is triggered is less than the reference voltage, i.e., the corner is at "Slow". At this time, the discharge current of the Output Stage should be increased, and compensation transistors, MN1b and MN1c should be turned on based on the corner of the overall circuit. The timing diagram of the PVT Detector circuit is shown in Fig. 14.

3.7. Digital Logic Control circuit

The Digital Logic Control circuit as shown in Fig. 15 serves as the digital coder for the driving of the transistors in the Output Stage. In addition, the output PS, PF, NS, and NF from the PVT detectors are encoded by this circuit, and the control signals $V_{gp[2:3]}$ and $V_{gn[2:3]}$ are generated to select which compensation transistors MP1b, MP1c, or MN1b, MN1c, respectively, will be turned on.

Signals OE and OEH are the operation modes of the control circuit. The Digital Logic Control circuit's truth tables for P-type and N-type Output Stage are shown in Tables 2 and 3, respectively. When OE and OEH are 0, the Digital Logic Control circuit will generate logic 1 for V_{gp1}, V_{gp2}, V_{gp3} and logic 0 for V_{gn1}, V_{gn2}, V_{gn3}, turning off the entire Output Stage. When OE and OEH are 1, the transistors controlled by V_{gp1} and V_{gn1} will always be turned on. D1 and D2 are outputs of the Level Shifter (LS), and PS, PF, NS, NF codes are outputs corresponding to each process corner.

When the process corner is FF, logic 0 is generated at outputs, PS, PF, NS, and NF. The Digital Logic Control circuit will output logic 1 at V_{gp2} and V_{gp3}. It will generate logic 0 for V_{gn2} and V_{gn3}, and the four auxiliary transistors of the Output Stage are turned off to reduce the voltage slew rate. When the process corner is TT, PS and NS will be low, while NF and PF will be high. V_{gp3} is high, and V_{gn3} is low; corresponding Output Stage transistor is off. The second auxiliary transistor in the stage maintains the voltage slew rate. When the PVT Detector circuit detects the SS corner, PS, NS, NF, and PF logic are high; thus V_{gp3} and V_{gp2} are low, and V_{gn2} and V_{gn3} are high, turning on the four auxiliary transistors of the Output Stage and increasing the slew rate.

3.8. Pre-driver

Two pre-driver circuits shown in Fig. 3 are added between the Digital

Fig. 22. Output waveform at VDD_{ext} = 1.6 V without PVT detection.

Logic Control circuit and the Output Stage to drive the very large-width transistors in the Output Stage. Each pre-driver circuit consists of 6 inverter stages in series where the aspect ratio of every stage is triple that of the aspect ratio of the previous stage.

4. Measurement results

The proposed output buffer is fabricated using TSMC 16-nm FinFET process. Its layout and die micrograph is shown in Fig. 16. Referring to the layout, the left side is the circuit with PVT detection, and the right side is the circuit without PVT compensation. These circuits were developed and compared to each other to evaluate their slew rate performance in the presence or absence of PVT detection and compensation. Notably, the die micrograph in Fig. 16 can not be seen with all the details because the foundry demands the minimum metal density such that the whole die is covered with metals. To avoid the loading effect of the pulled-out pins, buffers are added to increase the drive current. The chip uses the SB28 package and its area is 730.08 × 730.08 μ m^2. The left side's core area is 200.02 × 49.125 μ m^2 while for the right side is 175.98 × 49.125 μ m^2.

Monte Carlo analysis was performed no less than 200 times to determine the mean and standard deviation at each corner. This is done so that the performance of the PVT detection and SR auto-adjustment may be further justified. When the PVT detection is turned on, there is a discernible reduction in the amount of SR fluctuation as shown in Figs. 17 and 18. The PVT auto-adjustment approach has been shown to be successful as a result of this fact.

The measurement setup is shown in Fig. 19. A signal generator (Agilent E4438C) provides the input signals. A power supply (PRT3230) supplies VDD_{int}, VDD_{ext}, and Vref. Lastly, an oscilloscope (Keysight DSAV134) observes the V_{PAD}'s output waveform.

Figs. 20 and 21 shows the output PAD voltages (V_{PAD}) at VDDext = 0.8 V without and with PVT compensation, respectively, while Figs. 22 and 23 shows the output PAD voltages (V_{PAD}) at VDD_{ext} = 1.6 V without and with PVT compensation, respectively. When VDD_{ext} = 0.8/1.6 V, the SR in V/ns is 0.67/0.8 without compensation and 1.0/1.0 with compensation, respectively. This corresponds to an SR improvement of 49.2% and 37.5% for 0.8 and 1.6 V, respectively. Notably, the jitter in both VDD_{ext} = 0.8/1.6 V decreased by 30.97%/100%, respectively, after compensation. Better and lower jitters, 270.4 ps and 45 ps, were recorded for VDD_{ext} = 0.8/1.6 V, respectively, as shown in Figs. 24 and 25. Lastly, highest data rate was achieved at 250 MHz as presented in Figs. 26 and 27 for VDD_{ext} = 0.8/1.6 V, respectively.

The proposed buffer has a low SR compared to the others, though having lower SR has an advantage of the capability of the buffer to be utilized in applications such as USB 2.0 (SR = 1.0–1.2 V/ns) and DDR3 (SR = 0.4–2 V/ns). Its performance is compared with the recent DDR3 buffers between 2017 and 2022 as shown in Table 4. Though the slew rate adjustment of Ref. [3] (50%) and Ref. [20] (62.6%/75.8%) are better than ours (49.2%/37.5%) at same data rate (250 MHz) and the normalized power of Refs. [2,21] outperform our work, our buffer can function at a maximum load capacitance of 20 pF. Moreover, the prior buffer which was also realized and measured in silicon [20] did not contribute to a jitter reduction (320 ps; −116.2%) compared to ours. Apparently, it performs at a higher data rate than that of Ref. [4] (200 MHz). Meanwhile, Table 5 shows the performance comparison of our buffer to other state-of-the-art high frequency buffers. Most of these buffers outperform our buffer in terms of high slew rate, but only Refs. [19,22] are comparable to the proposed buffer, since they can be applied in DDR3 applications. However, they did not report any jitter reduction.

Fig. 23. Output waveform at VDD_{ext} = 1.6 V with PVT detection.

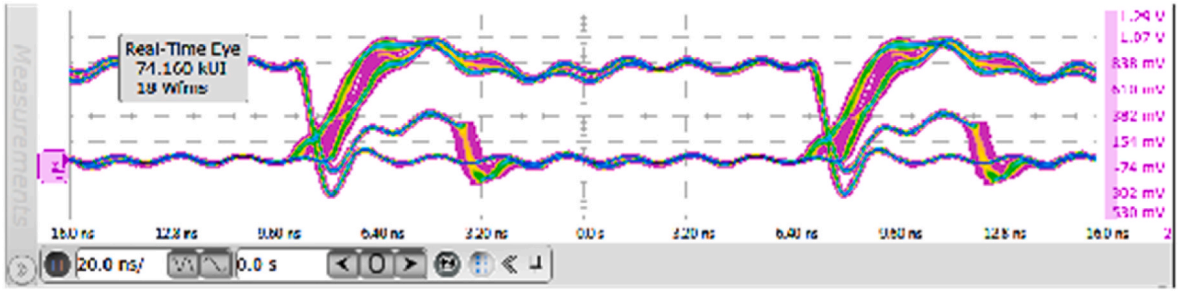

Fig. 24. Jitter eye diagram for VDD_{ext} = 0.8 V.

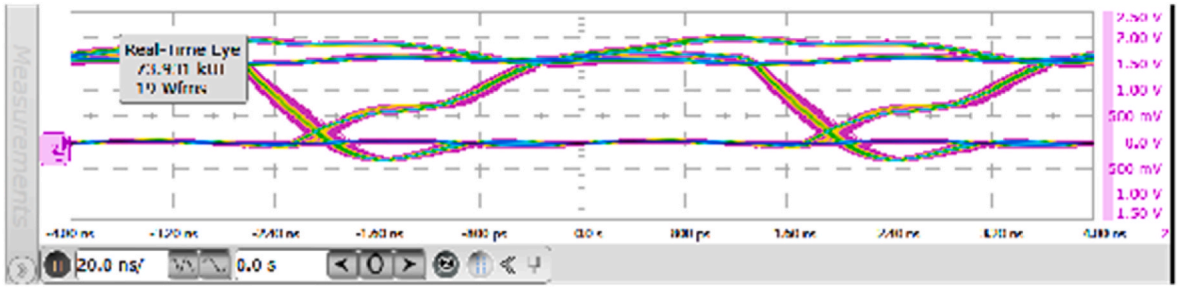

Fig. 25. Jitter eye diagram for VDD_{ext} = 1.6 V.

5. Conclusion

This paper proposes an output buffer, which is the first to be implemented and fabricated in a 16-nm FinFET CMOS process. The speed can be as high as 250 MHz, but it also makes the transistor more sensitive and is susceptible to the influence of process corners on the voltage slew rate of the output buffer. As a solution, an improvement mechanism by implementing gate driving stability and non-overlapping

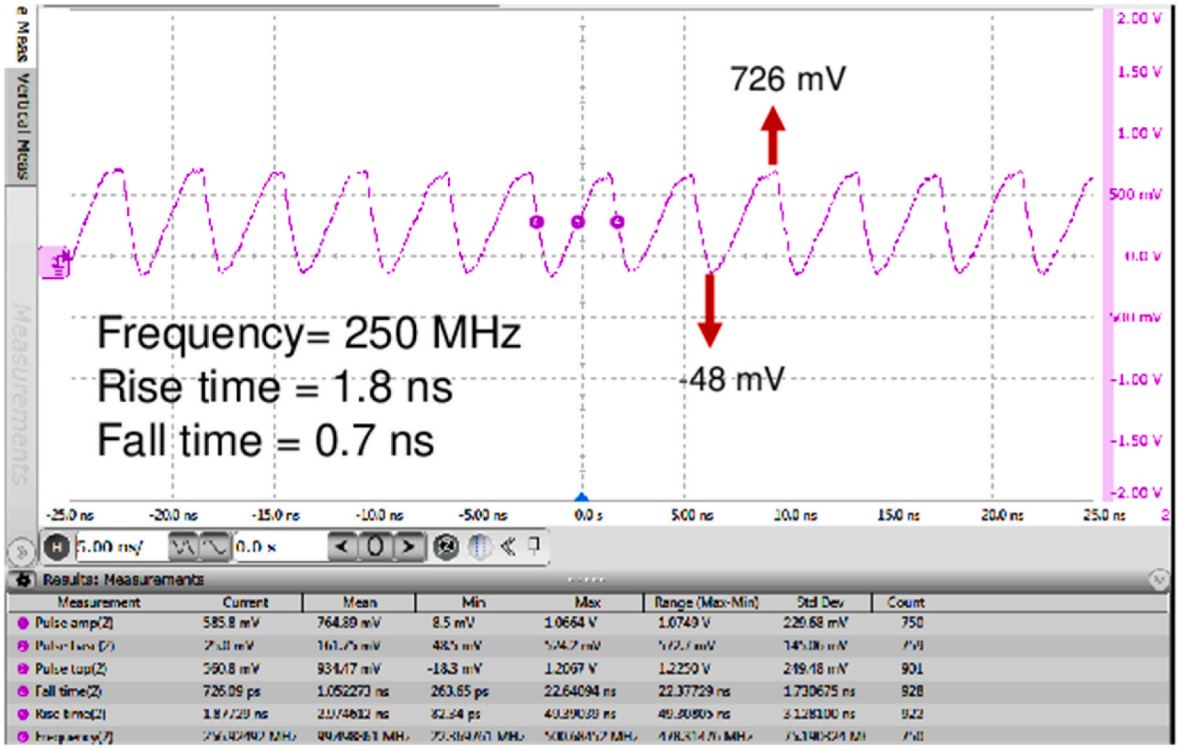

Fig. 26. Output waveform for the highest data rate at VDD_{ext} = 0.8 V.

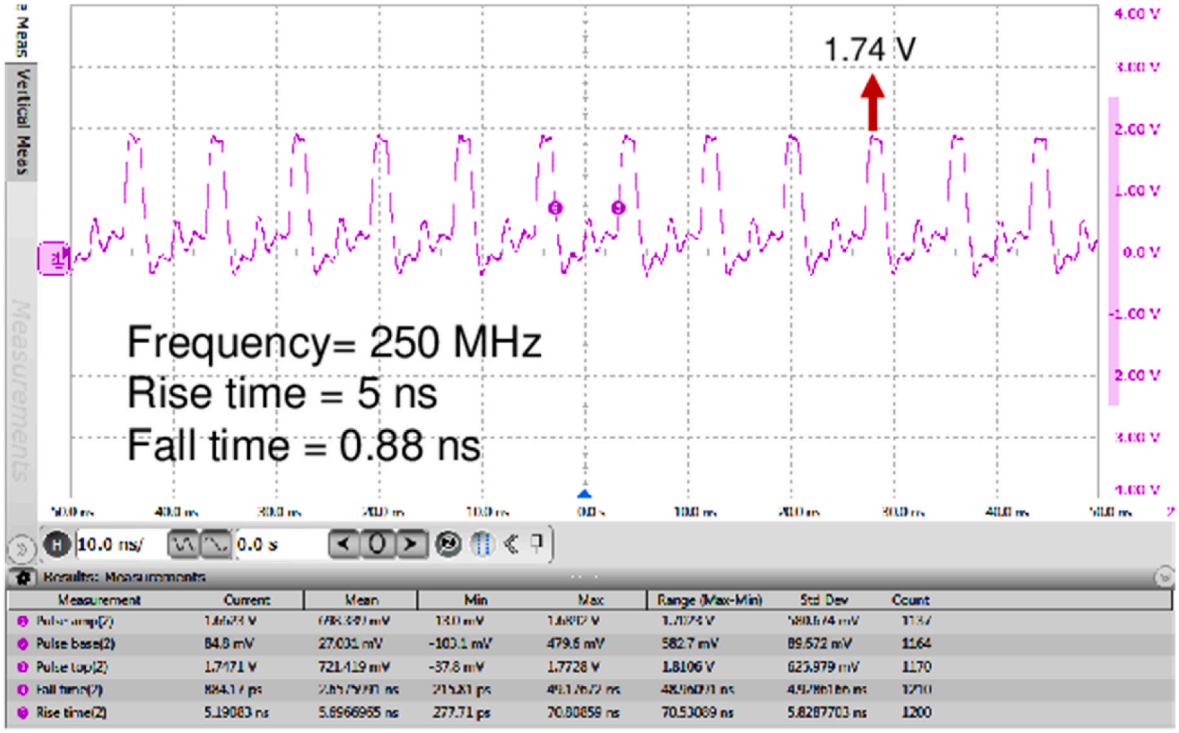

Fig. 27. Output waveform for the highest data rate at VDD_{ext} = 1.6 V.

signaling control is proposed. Moreover, by implementing the PVT compensation, slew rate is increased by 49.2% and 37.5% for 0.8 and 1.6 V, respectively, and the jitters for both voltages are decreased. Our work exhibited a jitter reduction rate of 30.97% and 100% for VDD_{ext} = 0.8/1.6 V.

Author statement

Chua-Chin Wang: Conceptualization, Methodology, **Lean Karlo S. Tolentino**: Data curation, Writing- Original draft preparation. **Shao-Wei Lu**: Circuit Simulation and Layout **Oliver Lexter July A. Jose**: Software coding. **Ralph Gerard B. Sangalang**: Software Validation.

Table 4
Comparison of performance with prior low frequency buffers.

	RACS	MWSCAS	ASICON	ISCAS	ICAECC	IET-CDS	Ours
	[2]	[3]	[4]	[23]	[21]	[20]	
Year	2017	2018	2019	2021	2022	2022	2022
Process (nm)	180	180	180	65	22	180	16
Verification	Simul.	Simul.	Simul.	Simul.	Simul.	Meas.	Meas.
VDD_{int} (V)	1.8	1.8	1.05–3.7	1.8	1.8	1.8	0.8
Tx voltage (V)	3.3/1.8	N/A	1.05–3.7	1.8/2.5/3.3	3.3/0.8–1.8	1.8	1.6/0.8
Data rate (MHz)	100	250	200	200	50	250	250
Slew rate (V/ns)	N/A	0.75–1.41	N/A	N/A	N/A	0.714–0.816	**1.0–1.1**
Nor. Power (mW/MHz)	1.04×10^{-3}	N/A	N/A	0.1195–0.149	0.058	0.221	0.112
Slew rate adjustment (%)	N/A	50	N/A	N/A	N/A	62.6/75.8	49.2/37.5
Jitter reduction (%)	N/A	N/A	N/A	N/A	N/A	−116.2	**30.97/100**
Load (pF)	10	5	100	N/A	5	5	20

Table 5
Comparison of performance with other prior buffers.

	ISCAS	ESSCIRC	TCAS-I	TCAS-II	ICDV	APCCAS	TCAS-II	Ours
	[22]	[24]	[25]	[19]	[26]	[27]	[16]	
Year	2013	2013	2013	2017	2017	2018	2019	2022
Process (nm)	40	28	90	40	28	40	40	16
Verification	Meas.	Meas.	Meas.	Meas.	Meas.	Simul.	Meas.	Meas.
VDD_{int} (V)	0.9	1.8	1.2	0.9	1.05	0.9	0.9	0.8
Tx voltage (V)	1.8	3.3	2.5	1.8	1.8	1.8	1.8	1.6/0.8
Data rate (MHz)	460	200	125	250	2000	1600	500	250
Slew rate (V/ns)	0.53	N/A	2.2–3.4	0.92–1.54	N/A	6.91–7.85	2.81	1.0–1.1
Nor. Power (mW/MHz)	N/A	0.45×10^{-3}	N/A	0.108	N/A	0.067	N/A	0.112
Slew rate adjustment (%)	8/6	N/A	40.5	67.4	36/39	37	46.5	**49.2/37.5**
Jitter reduction (%)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	**30.97/100**
Load (pF)	N/A	N/A	15	N/A	N/A	20	N/A	**20**

Tzung-Je Lee: Writing- Reviewing and Editing. **Pang-Yen Lou**: PCB Design and Measurement. **Wei-Chih Chang**: Technical Consulting.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper

Data availability

Data will be made available on request.

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