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A 16-nm FinFET 28.8-mW 800-MHz 8-Bit All-N-Transistor Logic Carry Look-Ahead Adder

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Abstract
Low-power and high-speed calculation is very important nowadays for energy-efficient demand of electronic devices. With the usage of ANT (All-N-transistor) logic, the speed constraint caused by PMOS transistors can be overcome through an auxiliary current path across NMOS transistors. This study presents a 800-MHz 28.8-mW 8-bit carry look-ahead adder (CLA) using ANT logic implemented on chip. FinFET technology is utilized to improve carrier mobility and increase device speed. R-C parasitic capacitance in FinFET devices is considered in the analysis of the delay time for the 8-bit CLA to improve PDP (power-delay product). The proposed design is implemented in 16-nm FinFET process with core area of $206.403 \times 152.506\ \mu m^2$. It has the lowest normalized PDP at 60 pF load by far.

Keywords FinFET technology · High-speed · Low-power · PDP · CLA · Dual Path

1 Introduction

In a growing number of portable devices, high-speed and low-power components are critical for energy-efficient demand [25]. As VLSI is concerned, CMOS process is widely used due to its temperature-stability response and anti-noise stability over other technologies such as emitter-coupled logic (ECL) and transistor-transistor logic (TTL) [20]. CMOS technology has also conventionally been preferred because of its low static current characteristics that results in low power consumption [3, 7, 21, 27].

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Even with many advantages, certain technologies have been reported for the speed disadvantage of CMOS. Carbon nanotube field-effect transistor (CN-FET) [35] and fin field-effect transistor (FinFET) [1, 26, 28] have recently emerged as viable options for high-speed application because of better carrier mobility and smaller area. CN-FET performs better than CMOS because of its low capacitance C_{gg} and the C_{gg} to I_{on} ratio. However, its incompatibility to the established industry-standard CMOS technology and large I_{off} are not preferred for low-power applications. Another technology to enhance the CMOS technology is double-gate FinFET [28]. A 1-bit full adder using 10 transistors implemented in this FinFET technology was proved to enhance the performance. The double gate technique reduces the leakage current, and the operating power resulting in the decrease of process variation impact. However, the cost is high and the yield is low. Spintronic devices have promising complementary properties such as near-zero static power consumption and are easy to be integrated with CMOS processes. Nevertheless, spin-CMOS-based approximation full adders have very low accuracy [16].

Other techniques widely used to reduce power dissipation are pass-transistor logic [27] and XNOR/XOR logic [3, 7, 21]. Nevertheless, the operation speed suffers due to the increase of the equivalent resistance formed by the series transistors thereof. The 6 hybrid full adders reported by Naseri *et. al.* were implemented using full-swing XOR/XNOR gates which have the characteristics of equal input capacitances, no NOT gates on the critical path, and small output capacitances resulting in higher speed and lower power [21]. They all utilized 2-1-MUX which exploited transmission gates without short-circuit and static power dissipation. However, since some inputs are driven through the diffusions, they will have difficulty in driving the said inputs when the load capacitance is large. Moreover, they are noise prone as well. Akhter *et. al.* proposed a full adder using a new topology for dynamic logic-based [2]. This new topology employs XNOR and XOR logic gates in the implementation of the full adder circuit, which improves the power dissipation and speed over XNOR/XOR logic alone.

The traditional Domino logic can be used also in logic operation in full adder design, but it is only limited to non-inverting operations [6]. Thus, the limitation of the non-inverting operation logic can be resolved by complementary all-N-transistor (CANT) which can realize both inverting and non-inverting logic operation [15]. However, due to the current path across the slow PMOS devices, the operating speed of CANT would be limited. The all-N-logic (ANL) topology is also a good solution because of its assistant driving current path that provides an increase of operation speed through NMOS transistors [13]. Even so, ANL circuit speed varies inversely proportional to the number of series transistors in the pull-down block.

To address all of the issues raised, the proposed 8-bit All-N-transistor logic CLA (carry look-ahead adder) reduced the power consumption and enhanced the operation speed, which is justified by the prototype fabricated by 16-nm FinFET process.

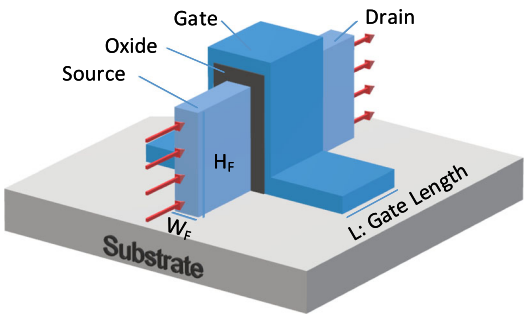


Fig. 1 FinFET perspective view [23]

2 FinFET Design Methodology

In order to enhance the operation frequency of the adder, FinFET technology is used in this research. Referring to [12], there are lots of accurate principles that scientists and engineers can use to evaluate FinFET design trade-offs. Electrical and physical properties of FinFET are associated to Berkeley Short-channel IGFET Model—Common Multi-Gate (BSIM-CMG) SPICE parameters such as GEOMOD and NFIN. Figure 1 shows the rectangular geometry of the FinFET [23]. The drain current in saturation region can be expressed as Eq. (1) [11, 12].

$$I_d = W_{\text{eff}} \cdot \mu_0 \cdot \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} \left(\frac{2kT}{2} \right)^2 \left(\frac{q_{\text{is}} - q_{\text{id}}}{L} + \frac{1}{2} \cdot \frac{q_{\text{is}}^2 - q_{\text{id}}^2}{L - \Delta L} \right) \tag{1}$$

where q_{is} and q_{id} are the normalized inversion sheet-charge densities calculated at the source and drain, respectively, ΔL is the gap between L and the channel pinchoff with effective width (W_{eff}) or the wire's circumference is as follows.

$$W_{\text{eff}} = N_F \cdot (2 \cdot H_F + W_F) \tag{2}$$

where N_F represents the number of fins, while H_F and W_F is the height and thickness of a fin, respectively.

Figure 2a, b is top view and side view, respectively, for the derivation of parasitic capacitances. The fringe C_{fr} and overlap C_{ov} capacitors affect the device characterization in short channel devices, including the gate-to-drain (C_{gd}) and gate-to-source (C_{gs}) parasitic capacitance [17].

Referring to Fig. 3, the parasitic capacitor can be characterized by five different parasitic capacitors. Therefore, the equation for (C_{gd}) as a function of N_F, C_{fr}, and C_{ov} is defined in Eq. (3),

$$C_{\text{gd}} = N_F \cdot (C'_{\text{gd,ov}} + C'_{\text{gd,fr}}) \tag{3}$$

where $C'_{\text{gd,fr}}$ and $C'_{\text{gd,ov}}$ represent the combined fringe and overlap capacitances, respectively.

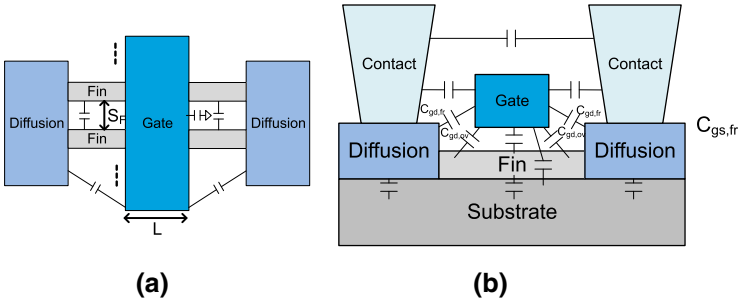


Fig. 2 FinFET **a** top view, and **b** cross-sectional view

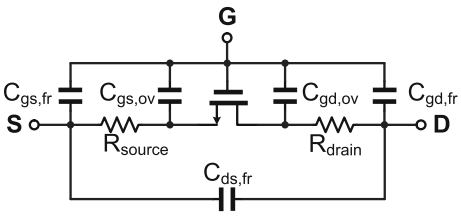


Fig. 3 R-C equivalent circuit of FinFET

A large parasitic resistance is formed by the drain and source terminals on both ends of the narrow fins [12]. In digital applications, the equivalent switching resistance R_n can be approximated to the reciprocal slope of the line starting $V_{\text{ds}} = V_{\text{DD}}$ up to $V_{\text{ds}} = 0$ in the current–voltage (I–V) curve [6]. The equation is characterized by Eq. (4).

$$R_n = \frac{V_{\text{DD}}}{W_{\text{eff}} \cdot \mu_0 \cdot \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} \left(\frac{2kT}{2}\right)^2 \left(\frac{q_{\text{is}} - q_{\text{id}}}{L} + \frac{1}{2} \cdot \frac{q_{\text{is}}^2 - q_{\text{id}}^2}{L - \Delta L}\right)} \tag{4}$$

or

$$R_n' = \frac{L}{W_{\text{eff}}} \tag{5}$$

where R_n' is the effective resistance.

Figure 4a, b shows the setup to determine the I_{d} dc characteristic curve for FinFET and cell layout, respectively, where nFin is the number fin equal to 20 with l = 60 nm. M_N has cell size of 0.625 µm × 1.114 µm with standard threshold voltage (V_{th}) equal to 375 mV, $V_{\text{ds(sat)}}$ = 198.7 mV, I_{d} = 864 mA, and I_g = 5.9 pA given that V_{gs} and V_{ds} are 774.7 mV and 749.4 mV, respectively. Figure 5a, b illustrates the I_d characteristic curve of the FinFET in relation to V_{ds} and V_{gs}. I_d has a value of 651 µA when V_{ds} is 200 mV.

Tabulated in Table 1 are the device specifications of standard V_{th} NMOS and V_{th} PMOS in a 16-nm FinFET CMOS process. These include the V_{th}, $V_{\text{DS(sat)}}$, and area of the transistors for the number of fins, fingers, and total width equal to 1, 1, and 10 nm, respectively.

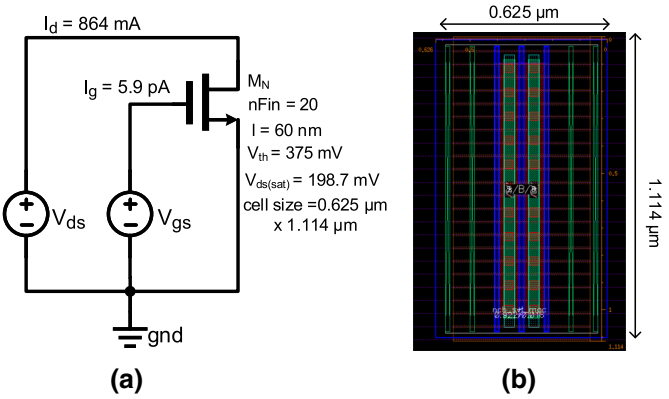


Fig. 4 FinFET **a** setup for I_d dc characteristic curve and **b** cell layout at nFin = 20 and l = 60 nm

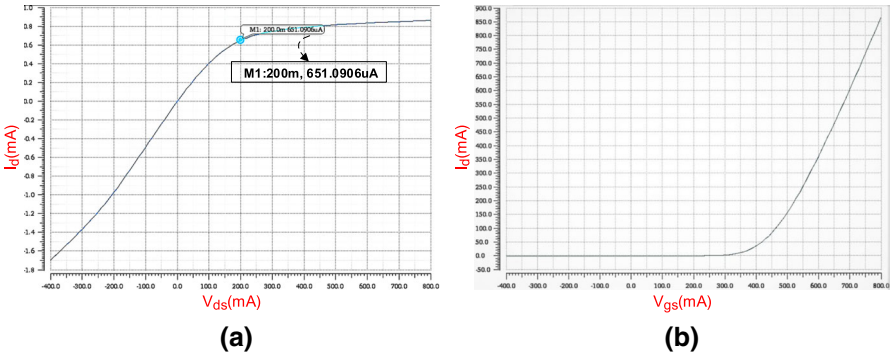


Fig. 5 FinFET I_d characteristic curve vs **a** $V_{\rm ds}$ and **b** V_{gs}

Table 1 Device specifications of transistors in a 16-nm FinFET CMOS process

	Standard $V_{\rm th}$ NMOS	Standard $V_{\rm th}$ PMOS
Length (nm)	16	16
$V_{\rm th}$ (V)	0.4101	−0.4083
$V_{\rm DS(sat)}$	0.2240	0.2783
Number of fins	1	1
Number of fingers	1	1
Total Width (nm)	10	10
Area (nm^2)	0.49 × 0.626	0.49 × 0.626

3 CLA Realized by All-N-transistor logic

Figure 6 shows the proposed 8-bit CLA adder block diagram. $A_0 \sim A_7$ and $B_0 \sim B_7$ are inputs of the adder. Two sets of true single-phase clock DFFs (TSPC-DFF) are used as the input registers. The outputs of TSPC-DFFs are coupled to 8-bit generate

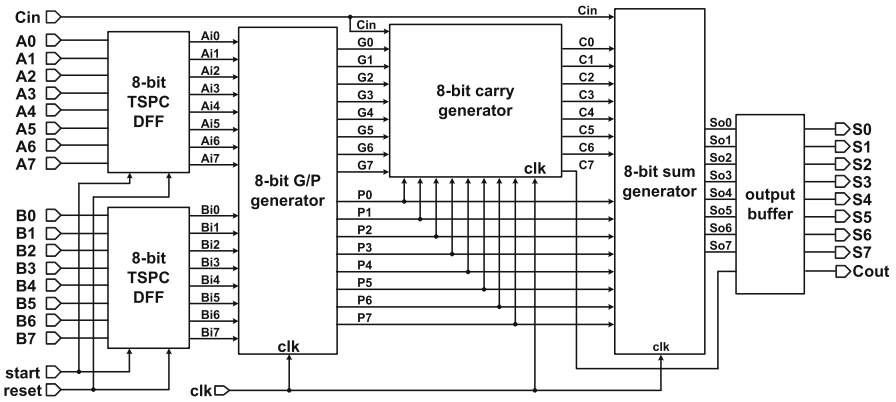


Fig. 6 Proposed 8-bit CLA block diagram

and propagate generator (8-bit G/P generator) synchronized by the system clock, clk. The simplified equations for P_i (propagate) and G_i (generate) are, $i = 0 \sim 7$, shown in Eqs. (6) and (7), respectively [36].

$$P_i = A_i \oplus B_i \tag{6}$$

and

$$G_i = A_i \cdot B_i \tag{7}$$

S_i (sum) and C_i(carry) are then functions of G_i and P_i as given in Eqs. (8) and (9), respectively [36].

$$S_i = C_{i-1} \oplus P_i \tag{8}$$

and

$$C_i = G_i + G_{i-1}P_i + G_{i-2}P_{i-1}P_i + \cdots + C_{in}P_0 + \cdots + P_{i-1}P_i \tag{9}$$

Apparently, the critical path is the generation of C_i, $i = 0 \sim 7$. The generated C_{i-1} and P_i are the input of the 8-bit sum generator. Finally, the C_{out} is computed through S_i and C_7. The final stage of the adder is output buffers to drive external loads, including pads and bondwires.

3.1 All-N-transistor (ANT) logic generic cell

The ANT logic is used to meet the low power-delay product (PDP) criterion. Figure 7a shows the schematic diagram of a generic ANT logic cell. When the clock (clk) signal in the ANT is 0, the circuit will go to the pre-charge phase, switching transistor P2 to OFF state and charging V_A to V_{dd}. Also, this phase turns OFF transistors N1 and N4.

Given the effects of the zero logic at the clk, the output of the ANT is the same as the previous state.

Changing the clk signal to 1, the ANT cell will go to the evaluation mode. In this mode, the output is based on the state inside the N-block. Thus, the operation can be expressed as Eq. (10).

$$Y = \overline{f(X_1, X_2, ..., X_n)} \tag{10}$$

where X_i, $i = 1, \cdots, n$, denotes the logic inputs. The ANT logic operates in one of four distinct cases during the evaluate phase in Fig. 7b, depending on the previous state of the logic output $V_{y,\text{pre}}$ and the logic operation of the N-block. The 4 different cases are discussed as follows:

Case 1: The ANT logic works in this case given $V_{Y,\text{pre}}$ the same as V_{dd} and the N-block is ON. The weak operation in transistor N3 and the discharge of V_A from V_{dd} to $V_{\text{dd}} - \mid V_{\text{thp}} \mid$ are caused by the voltage transition V_B to 0 V when clk changes to 1. Initially, V_C is clamped to zero potential, also through the pre-charge state while the output V_Y is pulled a bit lower by transistor N4.

The N-block together with the loop generated by P3 and N3 was immediately pulled down V_A, when V_A is less than $V_{\text{dd}} - \mid V_{\text{thp}} \mid$. The voltage at the output node is drawn back by transistors P2 and N4. Hence, the delay in case 1 can be expressed from the time V_Y changes from V_{dd} to V_{thp} by Eq. (11) and then Eq. (12).

$$\tau_{11} = k_1 \cdot R'_{n4} \cdot \frac{L}{W_{\text{eff}}} \cdot C_A \tag{11}$$

$$\tau_{11} = k_2 \cdot (R'_{p2} \parallel (R'_{n4} + R'_{p3})) \cdot \frac{L}{W_{\text{eff}}} \cdot C_Y \tag{12}$$

where the value of $k_1 = \frac{|V_{\text{thp}}|}{V_{\text{dd}}}$ and $k_2 = \frac{V_{\text{dd}} - |V_{\text{thp}}|}{V_{\text{dd}}}$, or ratio of the duration for the two-step operation. While C_Y and C_A are the parasitic capacitances at node A and Y, respectively.

When the clk signal is 0, P1 is ON, voltage at V_A is high, and P2 and N4 are short circuit that will give an output same as the previous state.

Case 2: Referring to Fig. 7, case 2 occurs when $V_{Y,\text{pre}}$ =0, and the N-block is ON. In the first step of this case, N-block discharges voltage V_A from V_{dd} to $V_{\text{dd}} - \mid V_{\text{thp}} \mid$. Once the voltage at node A drops below $V_{\text{dd}} - \mid V_{\text{thp}} \mid$, it is pulled down to the gnd quickly through the loop formed by transistors P3 and N3, and the N-block. Thus, since V_A drops below $V_{\text{dd}} - \mid V_{\text{thp}} \mid$, the output voltage across V_Y is then charged to V_{dd} through transistors P2 and N4. The first step delay, in this case, can be derived by the given equation for τ_{21}.

$$\tau_{21} = k_1 \cdot R'_{\text{N-block}} \cdot \frac{L}{W_{\text{eff}}} \cdot C_A \tag{13}$$

For the second step, the delay is the same as case 1, namely, $\tau_{22} = \tau_{12}$

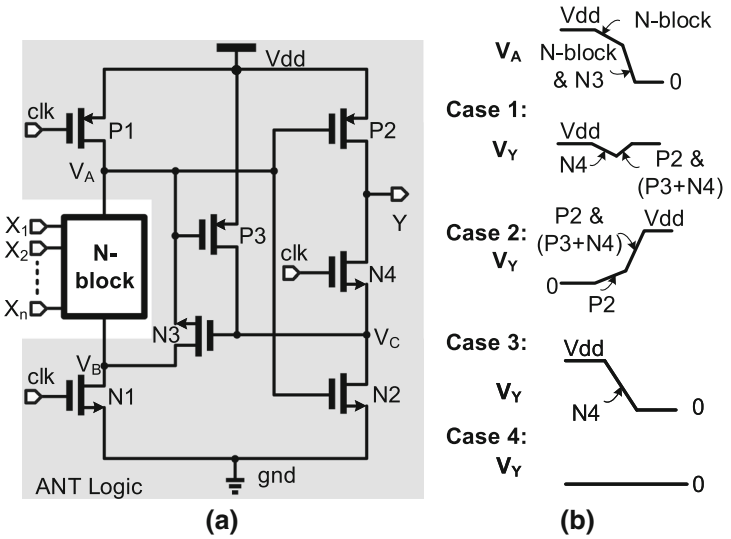


Fig. 7 ANT logic **a** schematic diagram and **b** illustrated waveforms

Table 2 ANT logic summary of operation

Case	$V_{Y,\text{pre}}$	N-block	V_Y
1	V_{dd}	ON	V_{dd}
2	0	ON	0 to V_{dd}
3	V_{dd}	OFF	V_{dd} to 0
4	0	OFF	0

Case 3: When the value of $V_{Y,\text{pre}} = V_{\text{dd}}$ and N-block is off, V_y will be discharged from V_{dd} to 0 through transistor N4 due to the initial condition of V_c which is equal to 0. In this case, the delay can be found as Eq. (14).

$$\tau_3 = (R'_{N4}) \cdot \frac{L}{W_{\text{eff}}} \cdot C_Y. \tag{14}$$

If the input clk signal is 1, N-block is turned on, and $V_{\text{dd}} - V_A > \mid V_{\text{thp}} \mid$, P3 will also go into ON-state through N3. V_A discharges faster and N-block will be charged to V_{dd}. The high potential output will pass to P2 and N4.

Case 4: When clk input is set to 1, N-block logic is not conducting, and voltage $V_Y = 0$, the output will be maintained at logic 0. This is because node A discharges through the short circuit consisting of transistors N3 and N4. If the previous state is high, node A will start to discharge the output through transistors N2 and N4. There is no transition in this case.

In short, the summary of the above 4 cases is tabulated in Table 2.

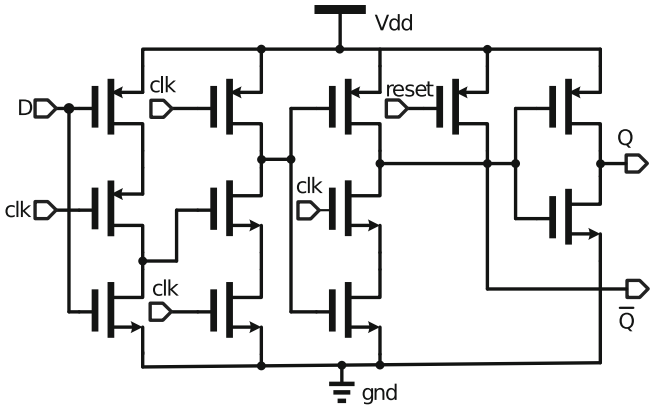


Fig. 8 1-bit TSPC DFF schematic [4]

3.2 True Single Phase Clock (TSPC) DFF

To ensure the synchronization of input signals, TSCP-DFF circuit is used as the input block of the CLA. A single bit of TSCP-DFF is shown in Fig. 8. When reset = 1 and clk = 1, the output Q is equal to whatever the value of the input D is. Changing the clk input to 0, Q will retain the previous state of D. Once the reset is set to zero, the output Q will always be zero, regardless of the values of clk and D. All conditions of the single-bit TSCP-DFF are applicable to 2 sets of 8-bit TSCP-DFFs that are used as input registers of the adder circuit. The advantage of this architecture is it is adaptive to high-frequency clock signals for high-speed computation.

3.3 G/P Generator

Figure 9 shows a 1-bit G/P generator consisting of AND and XOR based on ANT logic [36]. Notably, in the AND block, MN_{215} and MN_{216} are connected in series and driven by the input A_i and B_i, respectively. In the XOR block, as series transistors MN_{221} and MN_{222} are connected in parallel to another series pair composed of MN_{223} and MN_{224}. It is also driven by input A_i and B_i to perform an XOR logic operation. Figure 10 shows an 8-bit G/P block diagram based on single-bit G/P generators.

Referring to Fig. 7a again, P1 is sized with a large width to accommodate high current such that when clk is low, P2's gate will be pulled to high making it operates at cutoff (P2 is sized the same as P1 for symmetry). Since P2 is at cutoff, N4 is also at cutoff where output Y's condition is the same as the prior state.

Meanwhile, when clk is high, P1 is it cutoff while N1 and N3 are on. P3 is on, since its gate and node V_A are grounded. N-device transistor N3, and footer transistor N1 are sized based on inverter switching point or threshold with reference to P1. Since drain current for FinFET can be approximately modeled using nth power law [9] as shown in Eq. (15),

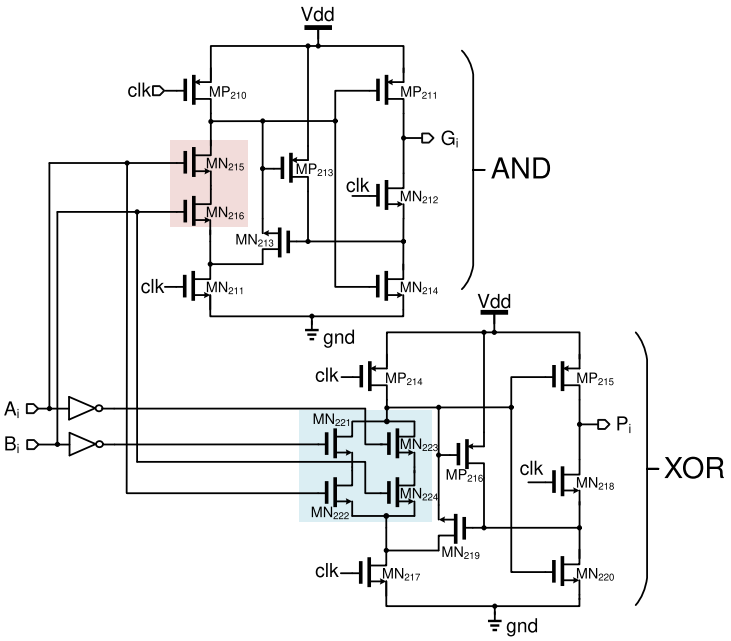


Fig. 9 1-bit generation and propagation (G/P) circuit

$$I_D = \frac{W}{L} \cdot \beta \cdot (V_G - V_{\text{th}})^n;\ V_{\text{DS}} >= V_{\text{Dsat}} = k(V_{\text{GS}} - V_{\text{th}})^m \tag{15}$$

and the current for NMOS and PMOS for the inverter is given in Eq. (16).

$$I_{\text{D(NMOS)}} = I_{\text{D(PMOS)}} \tag{16}$$

Substituting Eq. (15) in (16), where V_{GS} of NMOS is equal to the switching point voltage V_{SP}, and V_{GS} of PMOS is equal to $V_{\text{dd}} - V_{\text{SP}}$, the following equation is derived.

$$\left(\frac{W}{L}\right)_N \cdot (\beta_N) \cdot (V_{\text{SP}} - V_{\text{thn}})^n = \left(\frac{W}{L}\right)_P \cdot (\beta_P) \cdot (V_{\text{dd}} - V_{\text{SP}} - V_{\text{thp}})^n$$

$$V_{\text{SP}} = \frac{\sqrt[n]{\frac{\left(\frac{W}{L}\right)_N \cdot (\beta_N)}{\left(\frac{W}{L}\right)_P \cdot (\beta_P)}} \cdot V_{\text{thn}} + (V_{\text{dd}} - V_{\text{thp}})}{\sqrt[n]{1 + \frac{\left(\frac{W}{L}\right)_N \cdot (\beta_N)}{\left(\frac{W}{L}\right)_P \cdot (\beta_P)}}} \tag{17}$$

Moreover, since P1 is off when clk is high and node V_A is grounded, P2 and N4 are on while N2 is off. The sizing of P2 and P3 is treated as sizing for an inverter using again Eq. (17). N4 and P3 are sized such the switching point voltage equals to half of V_{dd}. The overall transistor aspects are tabulated in Table 3.

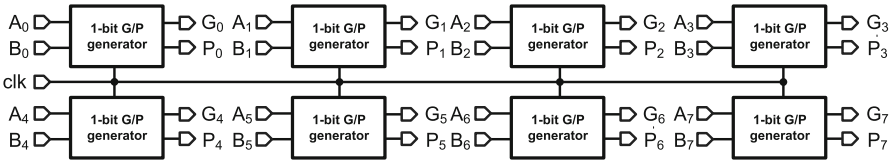


Fig. 10 8-bit generation and propagation (G/P) circuit

Table 3 AND/XOR ANT logic block sizing

AND/XOR transistor	W/L ratio
MN_{211}/ MN_{217}	25
MN_{214}/ MN_{220}	50/3
MN_{213}/ MN_{219}	5
MN_{212}/ MN_{220}	50/3
MP_{210}/ MP_{214}	100/3
MP_{211}/ MP_{215}	100/3
MP_{213}/ MP_{216}	10
$MN_{215} = MN_{216}$/ $MN_{221} = MN_{222} = MN_{223} = MN_{224}$	25/2

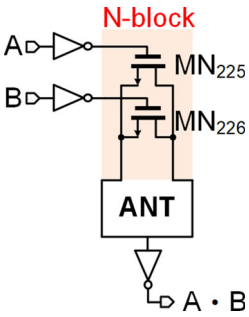


Fig. 11 ANT-based AND equivalent circuit (by De Morgan's law)

3.4 Carry Generation

In generating carries $C_0 \sim C_7$ to be needed by the adder, Eq. (9) is generalized for each carry as shown in Eq. (18).

$$\begin{aligned} C_0 &= G_0 + C_{in} P_0 \\ C_1 &= G_1 + G_0 P_1 + C_{in} P_0 P_1 \\ C_2 &= G_2 + G_1 P_2 + G_0 P_1 P_2 + C_{in} P_0 P_1 P_2 \\ &\vdots \\ C_7 &= G_7 + G_6 P7 + G_5 P_6 P_7 + \cdots + C_{in} P_0 P_1 P_2 P_3 P_4 P_5 P_6 P_7 \end{aligned} \tag{18}$$

Therefore, there is a need to use an AND gate with multiple inputs. A multiple series input AND logic is replaced with a multiple parallel connected NMOS devices

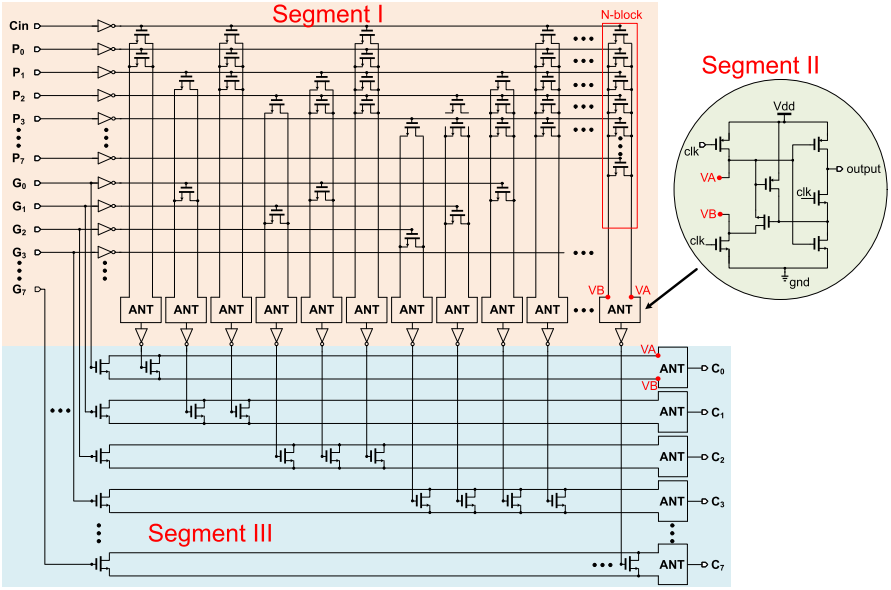
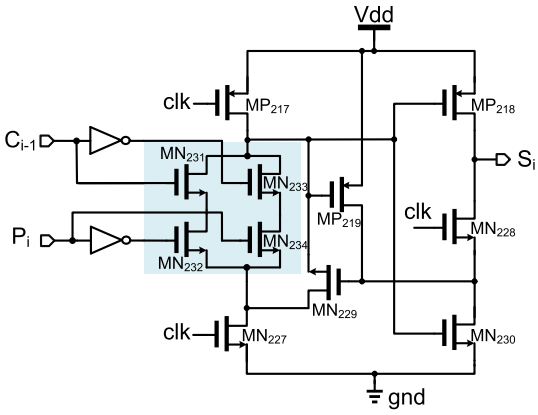


Fig. 12 8-bit carry generation circuit

Fig. 13 1-bit sum generator



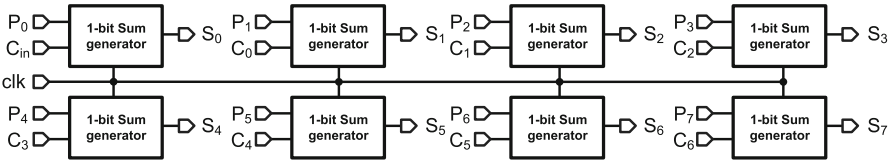


Fig. 14 8-bit sum generator

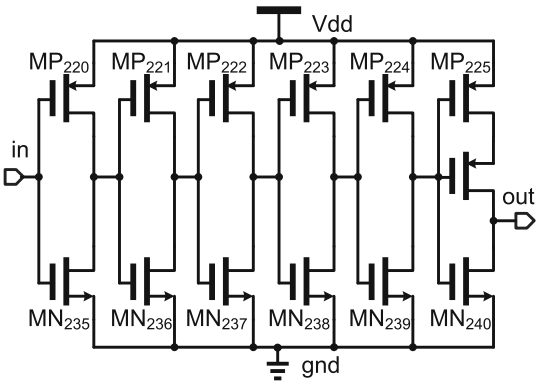


Fig. 15 Output buffer schematic

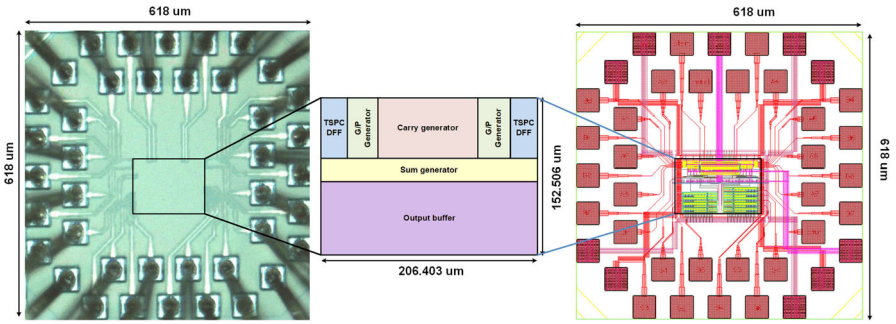


Fig. 16 16-nm CMOS FinFET ANT CLA layout and die photo

by De Morgan's law. Referring to Fig. 11, the inverted input, A and B, is sent to OR gate and the output of the OR gate must be inverted again. An example is shown in Eq. (19).

$$A \cdot B = \overline{\overline{A} + \overline{B}} \tag{19}$$

Figure 12 shows the overall 8-bit carry generation circuit which consists of 3 segments. They are detailed as follows:

Segment I: All AND logic cells presented in Eq. (18) are grouped together in this segment. The gates are designed using De Morgan's law as shown in the top part of Fig. 12.

Segment II: This segment shows the ANT logic cells which use the N-blocks from Segments I as shown in the middle part of Fig. 12.

Segment III: This shows the OR gates which are grouped derived from Eq. (18). Referring to Eq. (18), each carry can be derived depending on its significant bit and can be obtained as a function of C_{in}, G_i, and P_i, $i = 0 \sim 7$. The summation of terms from the equation can be realized using multiple-input ANT-based OR gate.

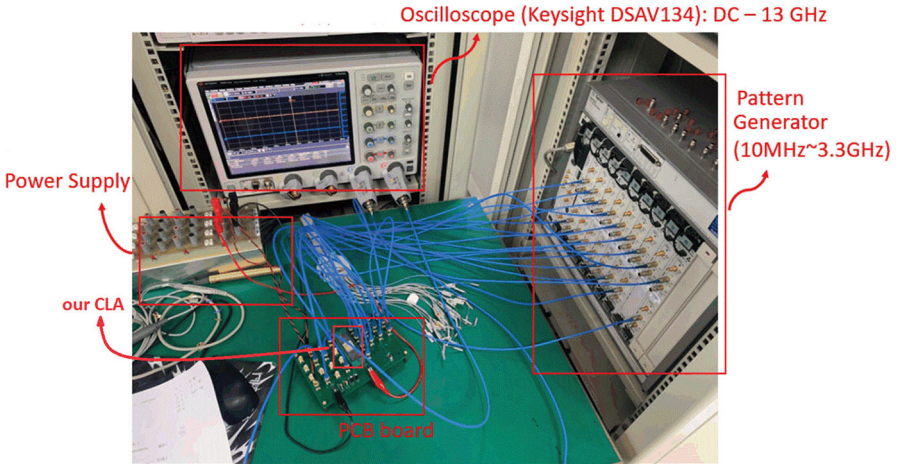


Fig. 17 Measurement setup

3.5 Sum Generator

The 1-bit sum generator circuit can be realized using XOR logic based on Eq. (8). Referring to Fig. 13, MN_{231} and MN_{232} are connected in series, which are parallel to MN_{233} and MN_{234}. Each S_i is then attained by the XOR ANT logic driven by C_{i-1} and P_i. Finally, the block diagram for an 8-bit sum generator based on single bit sum generators is shown in Fig. 14.

3.6 Output Buffer

The output buffer of the CLA consists of 6 stages of tappered inverters shown in Fig. 15. Each stage size is three times more than that of the preceding stage. A PMOS stacked to the last inverter giving a cascode connection. According to TSMC 16-nm FinFET process specifications, if the drain and source terminals of the PMOS are connected to the output PAD pin at the same time, it is recommended to use cascode connection. The additional PMOS also avoids the problem of latch up hazard at the output pad.

4 Implementation and Measurement

Illustrated in Fig. 16, the die photo and layout of the chip implemented using TSMC 16-nm CMOS LOGIC FinFET Compact (Shrink) LL ELK Cu 1P13M 0.8/1.8V process layout are demonstrated. The chip used 40-SB packaging with chip area (overall area) of $618 \times 618 \mu m^2$ and $206.403 \times 152.506\,\mu m^2$ core area. The size ratio and location of each sub-circuit is also shown in the figure as well.

For on-silicon measurement, PCB SMA connections are used for both input and output signals, including a dip switch for reset. The power supply Agilent N6761A

Table 4 Input pattern and expected output of Test 1 (Figs. 18, 19)

Input			Output	
$A_7 - A_0$	$B_7 - B_0$	C_{in}	$S_7 - S_0$	C_{out}
0001 0001	0100 0000	0	0101 0001	0
0001 0010	0100 0000	0	0101 0010	0
0001 0100	0100 0000	0	0101 0100	0
0001 1000	0100 0000	0	0101 1000	0
0000 0000	0100 0000	0	0110 0000	0
0011 0000	0100 0000	0	0111 0000	0
0101 0000	0100 0000	0	1001 0000	0
1001 0000	0100 0000	0	1101 0000	0

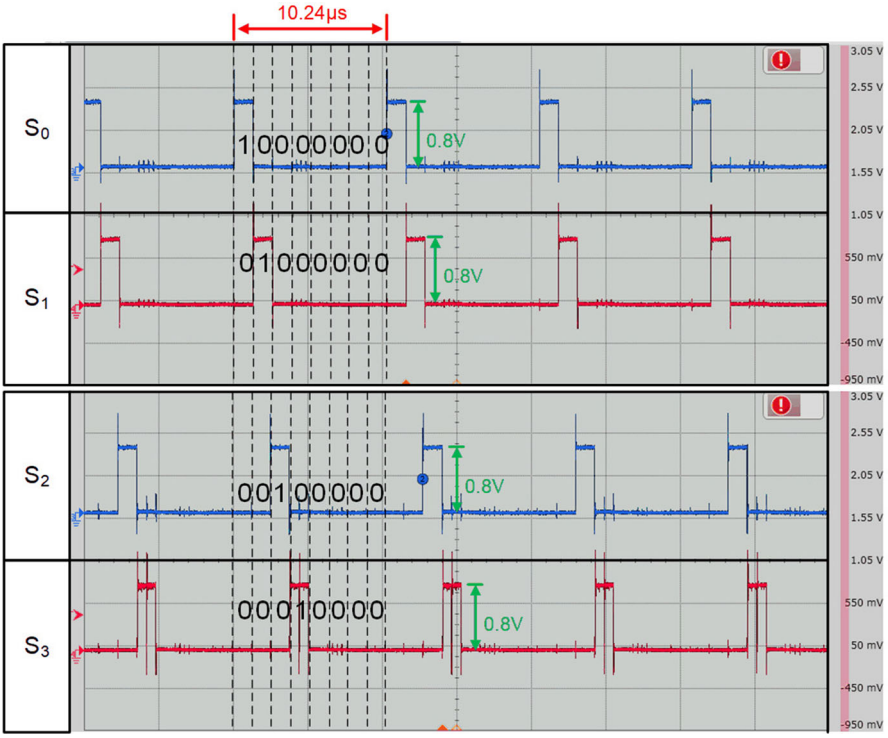


Fig. 18 S0 ∼ S3 at operating frequency of 800 MHz (Test 1)

provides 0.8 V power, and the data generator produced A0 ∼ A7, B0 ∼ B7, and clock input of the CLA adder. The output waveform is observed through Keysight DSAV134 high-frequency oscilloscope. The complete measurement setup for this investigation is shown in Fig. 17.

Table 4 shows the input pattern and expected output for the CLA adder at clk = 800 MHz. Figure 18 and 19 shows the actual results of the input pattern (Test 1). Another round of measurement is given in Table 5. The corresponding measurement

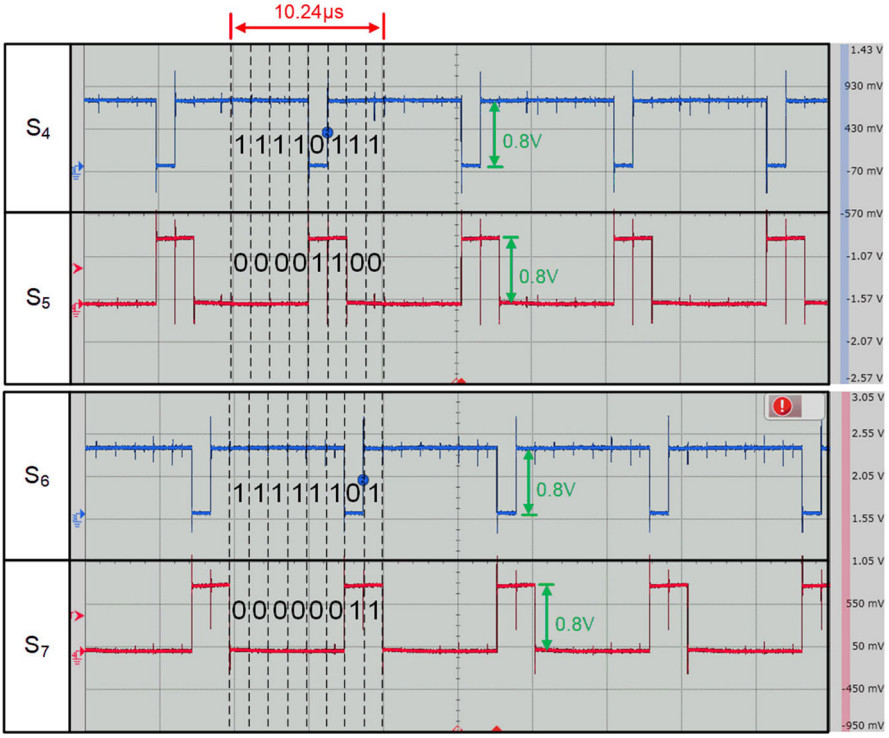


Fig. 19 S4 ∼ S7 at operating frequency of 800 MHz (Test 1)

Table 5 Input pattern and expected output of Test 2 (Figs. 20, 21)

Input			Output	
$A_7 - A_0$	$B_7 - B_0$	C_{in}	$S_7 - S_0$	C_{out}
0001 0000	0100 0001	0	0101 0001	0
0001 0000	0100 0010	0	0101 0010	0
0001 0000	0100 0100	0	0101 0100	0
0001 0000	0100 0000	0	0101 0000	0
0001 0000	0101 0000	0	0110 0000	0
0001 0000	0110 0000	0	0111 0000	0
0001 0000	0100 0000	0	0101 0000	0
0001 0000	1100 0000	0	1101 0000	0

waveforms are given in Figs. 20 and 21 (Test 2). Both measurement results prove the functionality and performance of the proposed ANT-based CLA.

Referring to Fig. 22, this work shows second lowest PDP per bit while most of the previous works are clustered to ten times higher. Notably, the lowest PDP in [18] was only by simulations, not measurements. Recent researches in CLA adder are compared shown in Table 6. Our CLA is the only work that was fabricated and tested on-silicon. We also used the highest value of load capacitance equal to 60 pF. It has the maximum

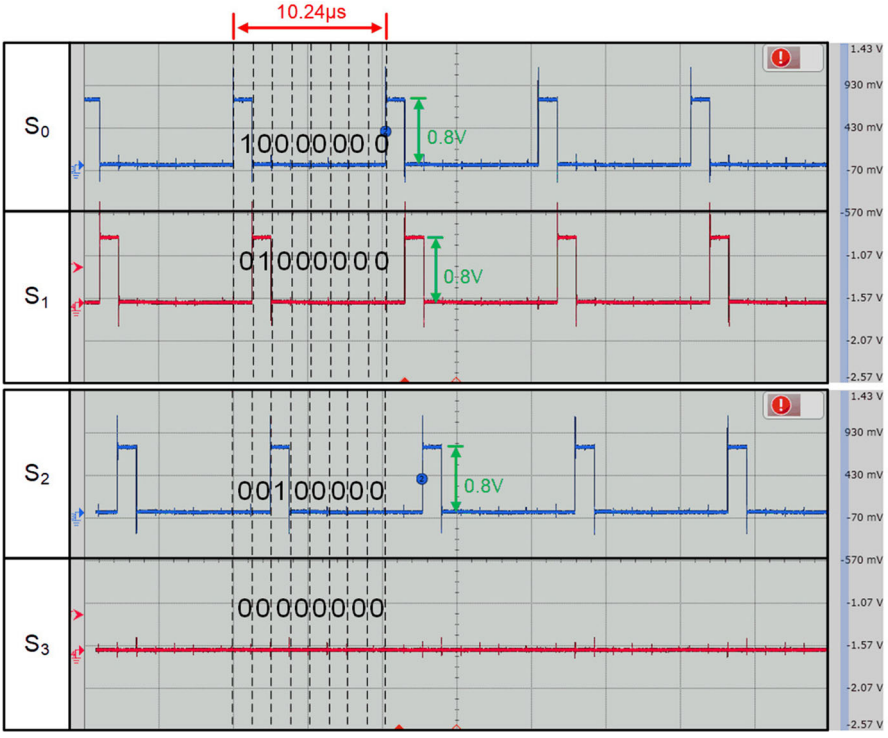


Fig. 20 S0 ~ S3 at operating frequency of 800 MHz (Test 2)

operating clock frequency of 800 MHz. This work also has the lowest simulation value of normalized power-delay product (PDP), which means it dissipates less energy per switching event compared with all prior works.

5 Conclusion

This research study is focused on 800-MHz 8-bit CLA using ANT logic implemented in 16-nm FinFET process with a 60 pF output load. The parasitic RC is derived using FinFET geometry. The low power-delay product (PDP) criterion is met using ANT logic. It is the only CLA design physically fabricated and tested with the highest value of load capacitance. This work has the highest energy efficiency thanks to its lowest amount of energy consumed per switching event compared to the other studies. Future work may propose the use of ANT logic in the BF16 floating adder. Since BF16 floating adder computation accuracy consumes a lot of power, the integration of this research to the adder will benefit the computation process due to its lowest value of norm. PDP.

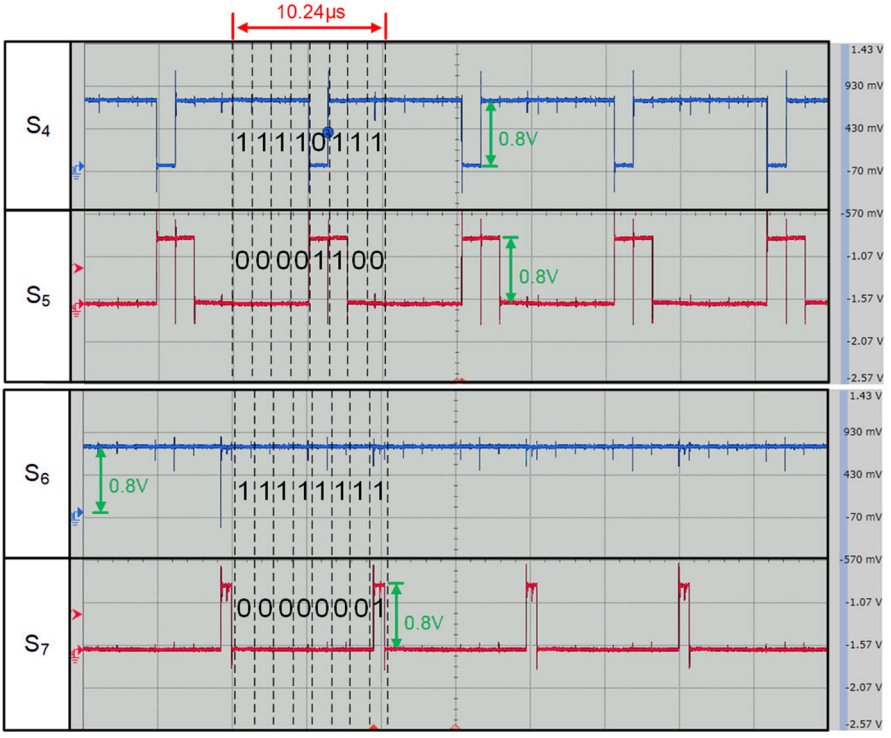


Fig. 21 S4 ∼ S7 at operating frequency of 800 MHz (Test 2)

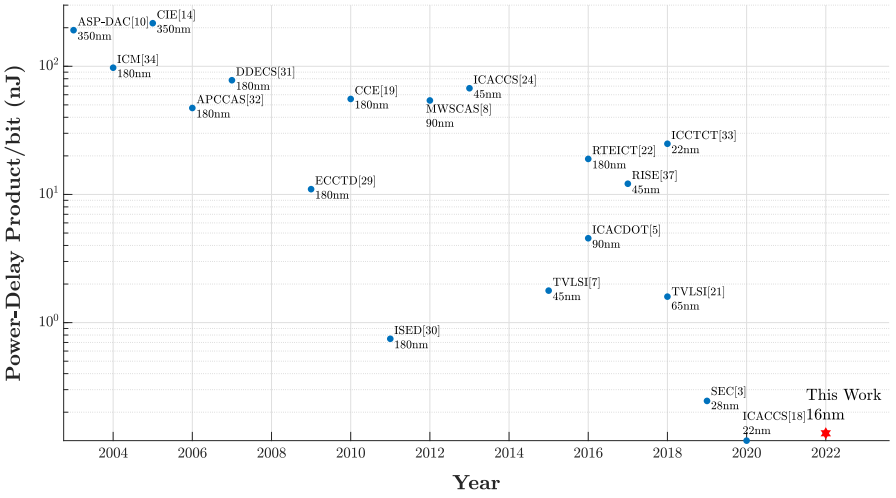


Fig. 22 Technology Roadmap of CLA designs in the past 2 decades

Table 6 Adder performance comparison

	[10]	[34]	[14]	[32]	[31]	[29]	[19]	[30]	[8]	[24]
Year	2003	2004	2005	2006	2007	2009	2010	2011	2012	2013
Publication	ASP-DAC	ICM	CIE	APCCAS	DDECS	EECTD	CCE	ISED	MWSCAS	ICACCS
Verification	Simul	Simul	Simul	Simul	Simul	Simul	Simul	Simul	Simul	Simul
V_{dd} (V)	3.3	1.8	3.3	3.3	3.3	1.8	1.8	1.8	1	0.9
Length (bits)	1	1	1	1	1	1	1	1	4	4
Max. Freq. (GHz)	0.001	0.5	0.125	0.2	0.8	0.1	0.2	1	2	0.333
Delay (ns)	0.12	2.332	0.9	1.4	0.26	0.14	0.238	0.02	0.246	2.164
Power Cons. (nW)	1.174	6.77	3280	3.68	65.2	0.002545	0.01514	0.012123	0.044	0.00084
Load Capacitance (pF)	0.01	0.01	0.1	0.01	0.01	0.01	0.01	0.01	0.01	0.01
Core area (mm^2)	N/A	N/A	N/A	N/A	NA	N/A	N/A	N/A	N/A	N/A
Norm. power [a] (mW)	15.94	0.418	24.096	0.338	2.994	0.785	0.785	0.374	2.2	0.311
Norm. PDP (nJ)	191.29	97.455	216.86	47.271	77.833	10.997	55.607	0.748	54.12	67.392

	[7]	[22]	[5]	[37]	[33]	[21]	[3]	[18]	[35]	This work
Year	2015	2016	2016	2017	2018	2018	2019	2020	2021	2022
Publication	TVLSI	RTEICT	ICACDOT	RISE	ICCTCT	TVLSI	SEC	ICACCS	TN	
Verification S	Simul	Simul	Simul	Simul	Simul	Simul	Simul	Simul	Simul	**Meas.**
V_{dd} (V)	1.2	1	1	1.2	1.2	1.2	0.9	0.8	1	0.8
Length (bits)	1	8	1	1	1	1	8	1	1	8
Max. Freq. (GHz)	0.1	0.5	1	0.5	1	1	0.5	1	0.1	0.8
Delay (ns)	0.0913	0.08	1.138	0.215	0.219	0.0518	0.001117	0.007	0.027	8.79
Power Cons. (nW)	1176.6×10^{6}	11835×10^{6}	46.25×10^{6}	4.06×10^{3}	0.01635	4.44×10^{3}	8865×10^{6}	0.0011	0.0024	28.8
Load Capacitance (pF)	0.0205	0.01	0.0034	0.01	0.01	0.01	0.01	0.01	0.001	60
Core area (mm^2)	2.584×10^{-5}	N/A	N/A	NA	NA	N/A	6.84×10^{-7}	N/A	N/A	0.0313
Norm. power (mW)	0.399	2.367	0.0136	0.564	1.135	0.308	2.189	0.172	24	0.93
Norm. PDP (nJ)	1.777	18.936	4.553	12.124	24.86563	1.595	0.245	0.12	648	**0.137**

[a] Norm. power $= \frac{\text{Power consumption(mW)}}{\text{f}\times\text{Loading Capacitor(pF)}\times V_{dd}^2(V^2)}$

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