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A 2.71 fJ/conversion-step 10-bit 50 MSPS split-capacitor array SAR ADC for FOG systems

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ABSTRACT

This investigation demonstrates a 10-bit SAR-ADC with low power dissipation per conversion step at 50 MS/s sampling rate. The proposed ADC is featured with the split-capacitance array by using unity-gain amplifiers and designed for fibre optic gyroscope (FOG) systems. The buffers based on the unity-gain amplifiers replace the bridge capacitors of the split-capacitance array in conventional SAR ADCs to resist process variation and enhance linearity of the capacitor-array. Aside from those, improvements in time response, that is, settling time, and capacitor size have also been proved. The design was implemented using a typical 40-nm CMOS process. The INL (integral non-linearity) and the DNL (differential non-linearity) were found to be 0.56 LSB and 0.51 LSB, respectively. The SNDR and SFDR are 51.23 dB and 61.46 dB, respectively, at an input of 12.5 MHz showing ENOB to be 9.79 bits at a sampling rate of 50 MS/s.

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ADC; SAR; fibre optic gyroscope (FOG); INL; DNL; split-capacitance array; SNDR; SFDR

1. Introduction

Successive approximation register analog-to-digital converters (SAR-ADC) exhibit many attractive attributes, such as medium resolution, low power consumption, and mid-range sampling rate. These attributes are the reasons why SAR ADCs are used for applications, such as low-power systems (Kim et al., 2016; Liu et al., 2010; Tung & Huang, 2018), biomedical implants (Cheng & Tang, 2015; Hong & Lee, 2007; Wang & Hung, 2020), and fibre optic gyroscope (FOG) system (C.-T. C.-T. Chen et al., 2019).

A fibre optic gyroscope system makes use of optical fibre to measure angular movement based upon the process called the Sagnac Effect. When the gyro makes a rotation, the optical signal passing through the fibre optic cable experiences phase shift sensed by a photo detector. This then goes through digital conversion for further processing to get the rotational angle as depicted in Figure 1. The required sampling rate for a system with 0.5°/hr specification is 50 MS/s at 10 bits resolution for military applications.

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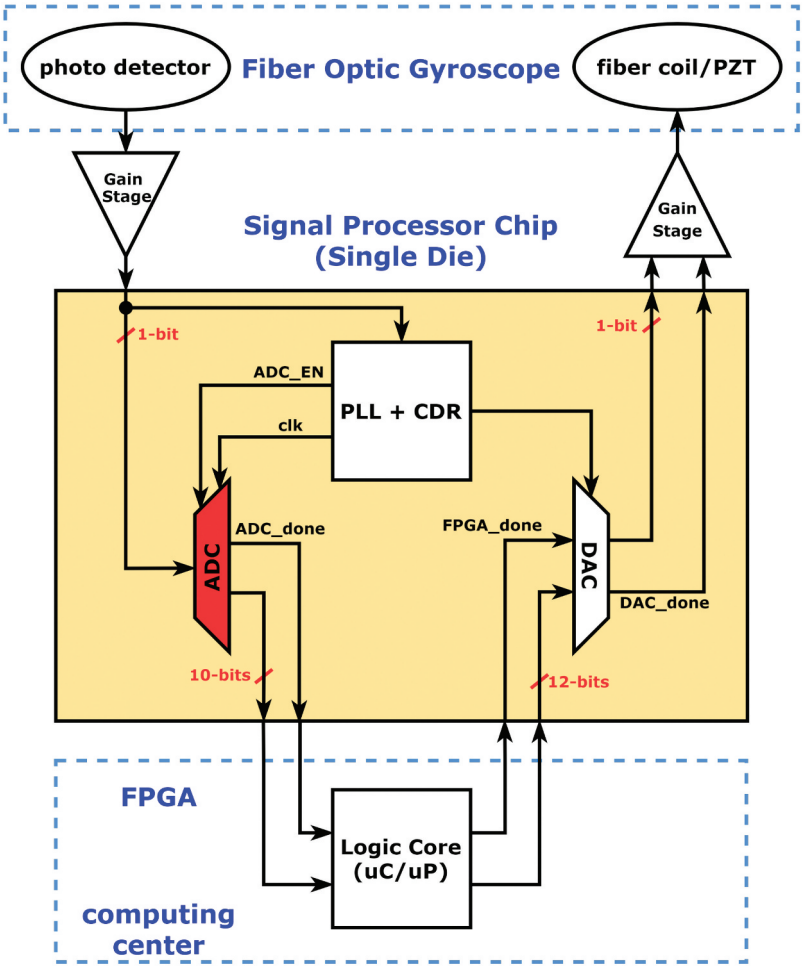

Figure 1. Block diagram of the FOG system.

Figure 2 shows the block diagram of a typical SAR ADC. It is composed of four main components: 1. SAR Control Logic, 2. Comparator, 3. Digital-to-Analog Converter (DAC), and 4. Sample-and-Hold (S/H) Circuit. Charge redistribution DACs are widely used in SAR ADCs because of the simplicity and low power consumption. Another advantage of using charge redistribution DACs is that it behaves as an S/H circuit, hence neither a chip space for an S/H nor an external S/H is required.

Figure 3(a) shows a conventional architecture of a charge redistribution SAR ADC. It uses a binary weighted DAC in this architecture. The output is obtained by a binary search correction algorithm, to which a high amount of energy is being used during search. Also in this design, the input load and area of the capacitor array increases as the number of bit increases. To reduce power consumption, a monotonic switching architecture shown in Figure 3(b) is proposed by Liu et al. (2010), reducing power loss by 81% and capacitance area by 50%. However, the total area and capacitance of the capacitor array is still exponentially increasing with the number of bits, limiting the operating speed and

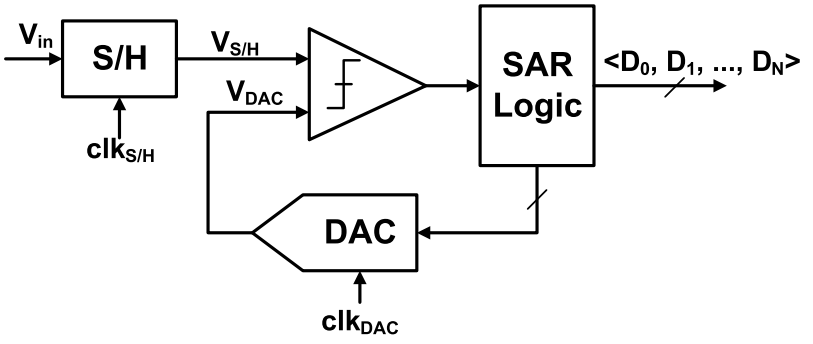

Figure 2. SAR ADC block diagram.

resolution of the ADC. Split-capacitance architecture is a solution to reduce the area and power consumption of the capacitor array. This is done by splitting the capacitor array into two or more sub-arrays inserting a bridge capacitor between the sub-arrays. The bridge capacitor has a fractional value, shown in Figure 3(c), to make the total weight of the LSB array equal to the lowest weight in the MSB array (Baker, 2019). Mismatch problems and complicated control techniques are needed if the bridge capacitor is not an integer-order multiple of the unit capacitance, such as in Tung and Huang (2018). In Figure 3(d), Agnes et al. (2008) proposed that the bridge capacitance equal the unit capacitance and removed the dummy capacitor. This method proves to make the weight of the LSB array equal the lowest bit of the MSB array. Unfortunately, a 1 LSB gain error is the least price to pay in this architecture. Both methods shown in Figure 3(c-d) are vulnerable to mismatch issues. Y. Y. Chen et al. (2009) proposed a calibration scheme to avoid gain error as well as improving the linearity for a split-capacitance architecture. This comes at a cost of an additional block and a more complex control circuit. Figure 3(e) proposed by Guo and Mirabbasi (2012) shows a new architecture combining the monotonic switching procedure and a modified switch capacitor array to compensate for the parasitic mismatch, sacrificing a larger area.

The above problems can be addressed by using unity gain buffers in splitting the capacitor array as proposed in this investigation. Through the introduction of the unity gain buffers as replacements for the bridge capacitor, the capacitor sizes and the time response of the capacitor array will be improved. Process variations causing linearity loss in the bridge capacitor has also been avoided.

2. 10-bit split-capacitor array SAR ADC using unity-gain buffers

The proposed 10-bit 50 MS/s SAR ADC architecture is shown in Figure 4. The proposed design is fully differential to minimise the noise effects coming from the substrate and the supply. It is composed of two capacitor arrays, namely, the most significant bit array (MSB Array) and the least significant bit array (LSB Array), serving as the digital-to-analog converters used for coarse and fine conversion, respectively. Two unity gain buffers are introduced to separate the coarse and fine conversion arrays replacing the bridge capacitor in those traditional split-capacitor arrays. By this, the total capacitance are realised with smaller sizes compared to traditional counterparts. The size reduction is

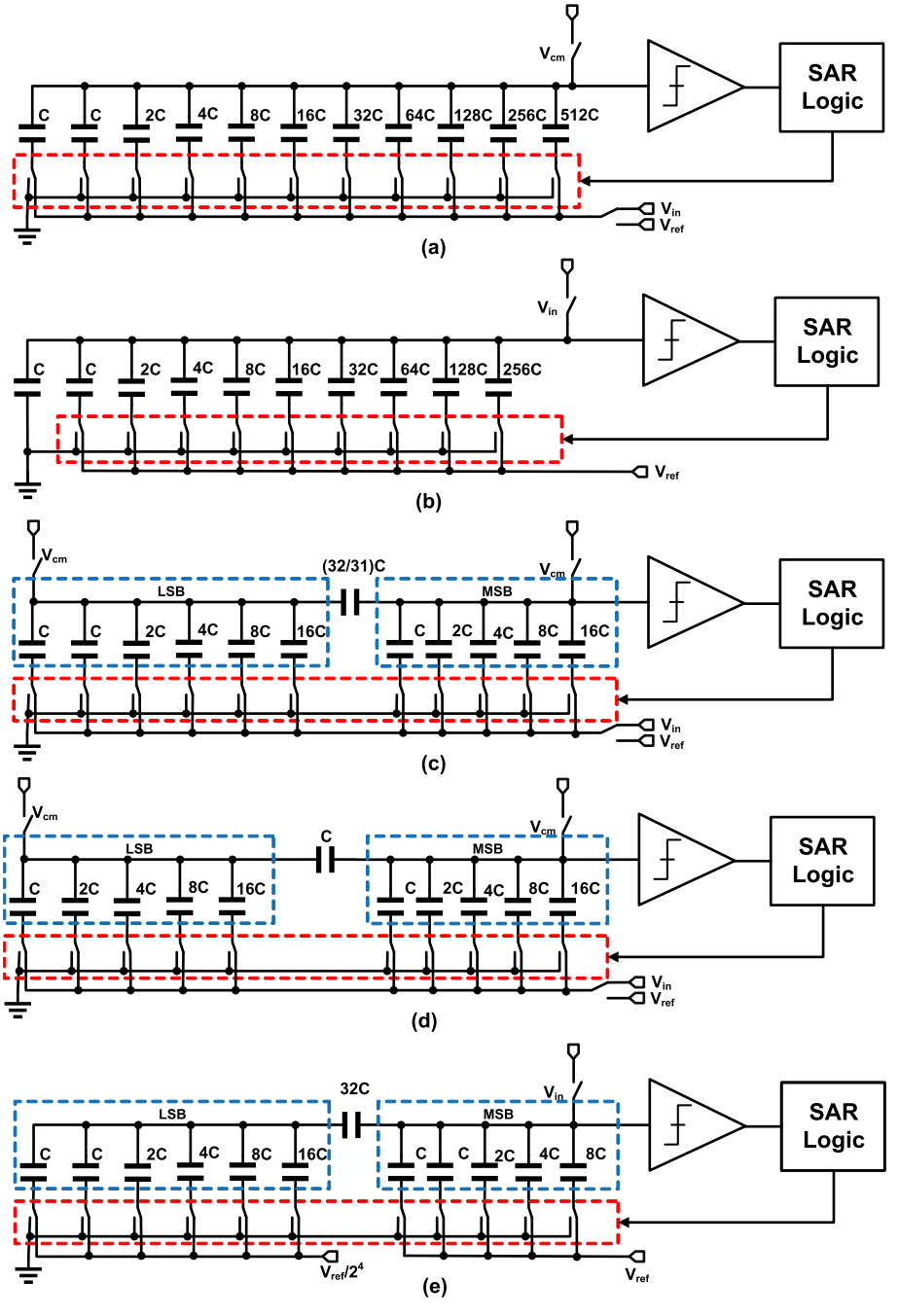

Figure 3. Charge-Redistribution Successive Approximation Register Analog-to-Digital Converter (SAR ADC) (a) Conventional Architecture, (b) Monotonic Architecture (Liu et al., 2010), (c) Split-Capacitance with Fractional Bridge Capacitor (Baker, 2019), (d) Split-Capacitance with Unit Bridge Capacitor (Agnes et al., 2008), (e) Parasitic Compensated Split-Capacitance (Guo & Mirabbasi, 2012).

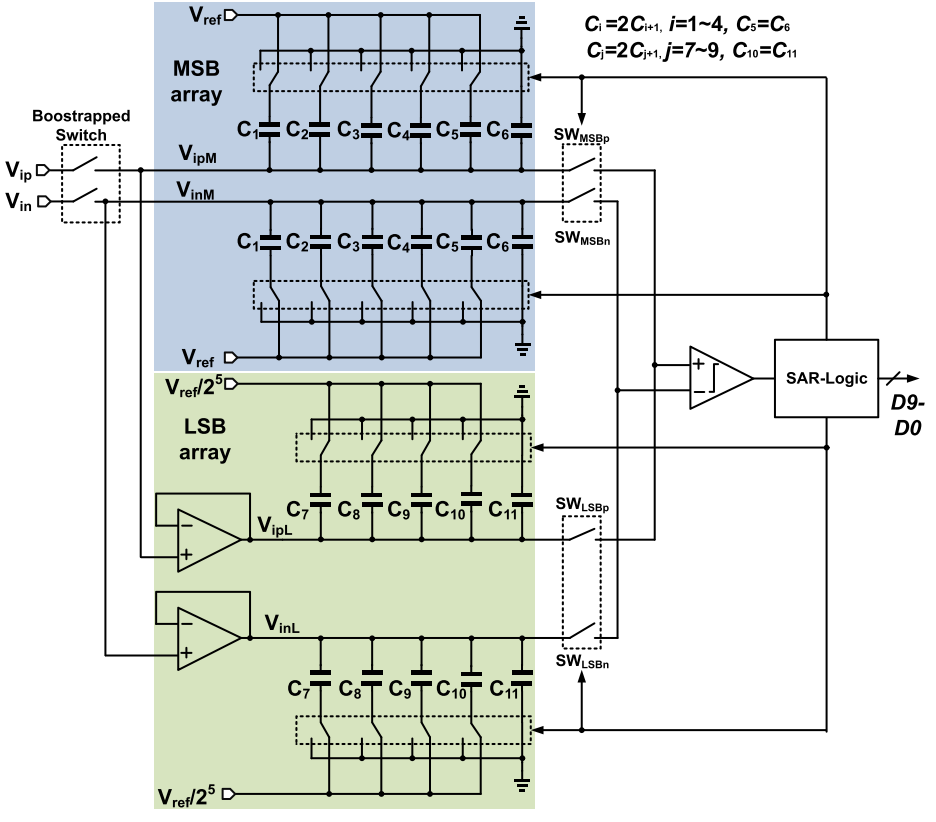

Figure 4. Proposed SAR-ADC architecture.

from 2^N to $(2^{N/2+1} + 2^{N/2})$ times the size of a unit capacitor generalised for N-bit resolution theoretically. For instance, the capacitor array exhibits 90.63% size reduction for the 10-bit resolution. All the circuit details will be disclosed in the following text.

Table 1 shows the comparison between the capacitance arrays of the different architectures presented in Figure 3. The values shown here for our design is based on single-ended versions for simplicity.

The fractional bridge capacitor (C_{br}) is designed to have a value shown in Eqn. (1). When N approaches a large value, C_{br} approaches C_u (unit capacitance).

$$C_{br} = \frac{2^{N/2}}{2^{N/2} - 1} C_u \tag{1}$$

Table 1. Comparison of capacitor arrays among different DAC architectures.

Architecture	Total Capacitance (for N-bit Resolution)	Total Capacitance (for $N = 10$)	Normalised Area
Binary-Weighted	$2^N C_u$	$1024C_u$	$\times$ 21.33
Monotonic	$2^{N-1} C_u$	$512C_u$	$\times$ 10.67
Fractional Bridge	$(2^{N/2+1} - 1)C_u + C_{br}$	$\approx 64C_u$	$\times$ 1.33
Unit Bridge	$(2^{N/2+1} - 1)C_u$	$63C_u$	$\times$ 1.31
Parasitic-Compensated	$2.5 \times 2^{N/2} C_u$	$80C_u$	$\times$ 1.67
This Work	$1.5 \times 2^{N/2} C_u$	$48C_u$	$\times$ 1

2.1. System operation

The proposed SAR-ADC timing waveform is presented in Figure 5. There are three phases in the timing waveform, (1) sampling, (2) coarse conversion, and (3) fine conversion phases.

(1) **Sampling phase**: When the sampling clock (Clks) is high, the bootstrapped sample-and-hold switches are on to perform sampling on the inputs Vip and Vin. When the sampling clock goes low, the system enters the coarse conversion mode.

(2) **Coarse conversion phase**: The sampled signals in the MSB array are then compared by the comparator when the conversion clock (Clkc) is high. When Clkc switches to low, the MSB array are then adjusted depending on the results from the SAR-logic ciruit. At the same time, voltage level of V_{ipM} and V_{inM} are updated and bit D9 is obtained. The process is repeated for another 5 Clkc cycles until bit D5 is generated. Switches, SW_{MSBp} and SW_{MSBn} shuts off, and the coarse conversion mode ends.

(3) **Fine conversion phase**: V_{ipM} and V_{inM} signals are then held at the MSB array. Simultaneously, SW_{LSBp} and SW_{LSBn} switches are on, entering the fine conversion mode. Now, the signals, V_{ipL} and V_{inL}, are then coupled to the LSB array for the comparing process driven by Clkc. Bit D0 is then obtained after 5 Clkc cycles. After obtaining D0, the sampling clock will then be high to reset the arrays to be ready for the next conversion.

2.2. Unit capacitance

The unit capacitance in this design is chosen using the criteria presented by Yue (2013). There are two constraints to be considered in selecting the unit capacitance of split-capacitance DAC, namely matching constraints and thermal noise constraints. Eqn. (2) is

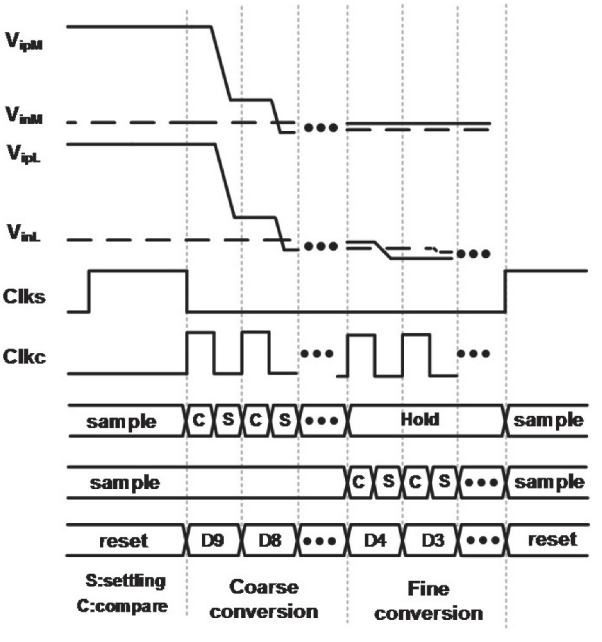

Figure 5. Timing waveform of the proposed SAR ADC.

used to determine the minimum capacitance required by matching constraints. The equation is derived at most 3.5 σ deviations to maintain high reliability to process variations. The parameter σ, in Eqn. (3), denotes the nominal capacitance variation determined by the process and size of the capacitance.

$$C_{m(min)} = \rho_c\{\frac{3.5k[2^{N+2}(\sqrt{2^N}-1)+(\sqrt{2^N}-1)\sqrt{2^N}]}{(\sqrt{2^N}-1)2^N}\}^2 \tag{2}$$

$$\sigma(\frac{\Delta C_{nom}}{C_{nom}}) = \frac{k}{\sqrt{WL}} \tag{3}$$

Eqn. (4) shows the formula to compute the minimum unit capacitance due thermal noise constraints. Thus, Eqn. (5) will be used to determine the final unit capacitance to be used in the DAC based on Eqn. (2) and (4).

$$C_{n(min)} = \frac{4KT \times 2^{N+4}}{V_{ref}^2} \tag{4}$$

$$C_{min} = \max\{C_{m(min)}, C_{n(min)}\} \tag{5}$$

where:

ρ_c – capacitive density of the capacitor
k – proportionality constant determined by the process
$_N$ – resolution
K – Boltzmann's constant
T – temperature in Kelvin
V_{ref} – reference voltage

Using the aforementioned formulas, the unit capacitance used in our ADC system is 3 fF MOM (Metal-Oxide-Metal) capacitor of which the area on silicon is 4.37 $\times$ 4.37 μm^2.

2.3. Sample-and-hold (S/H) circuit

Conventional SAR ADCs are normally sampled at the bottom plate of the capacitor arrays because of good linearity property. The signals are connected to the bottom plate of the capacitor while the top plates are reset with a fixed voltage. The power rails are normally selected as the reference voltage to avoid additional voltage levels in the circuit. Problems arises during full-range input sampling, the DAC output go beyond the rails (Zhang et al., 2012). This can be alleviated by decreasing the input range, sacrificing signal-to-noise ratio (SNR). Bottom plate sampling not suitable for low-voltage SAR ADCs because it requires larger number of charge pump-based switches (Harikumar, 2015; Harikumar et al., 2016).

SAR ADC design in the recent years have input signals connected to the top plates of the capacitor-array (Cheng & Tang, 2015; Liu et al., 2010; Mei et al., 2017; Song et al., 2016; Tung & Huang, 2018). Through this way, the input bandwidth and the settling speed are increased. In turn, power consumption and performance of the ADC experience improvement.

The sample-and-hold circuit used in this investigation is a combination of N- and P-type bootstrapped switches for sampling linearity improvement as presented in Figure 6. The N-type switches are M_{N505} and M_{N506} while the p-type switches are M_{P506} and M_{P507}. Upon using them simultaneously, an increase in sampling range is observed as well as the avoidance of the clock feed-through experienced by other switch configurations is achieved (Cheng & Tang, 2015). The N-type switches' bootstrapped circuit is composed of $M_{N501} \sim M_{N504}$, $M_{N507} \sim M_{N509}$, and M_{P510}. The transistors used on the P-type bootstrapped switch is configured to be symmetric to the N-type bootstrapped switch as described.

• **Sampling mode**: During sampling, Clks goes high, creating a closed loop path from the capacitor to M_{N507} giving enough gate voltage to turn M_{N505} and M_{N506} on. Once the loop is established, the gate drives of M_{N505} and M_{N506} is $V_{DD} + V_{in}$, easily crossing the threshold requirement of the switches.

• **Hold mode**: When the circuit is not sampling the input, Clks is logic low. M_{N501} and M_{N502} are conducting creating a path for the capacitor to be charged up to approximately V_{DD}.

The P-type bootstrapped circuit operates the same way. However, the linearity is poor at higher voltages so that the architecture proposed by Cheng and Tang (2015) using both the N- and P-type bootstrapped sampling circuit is adopted.

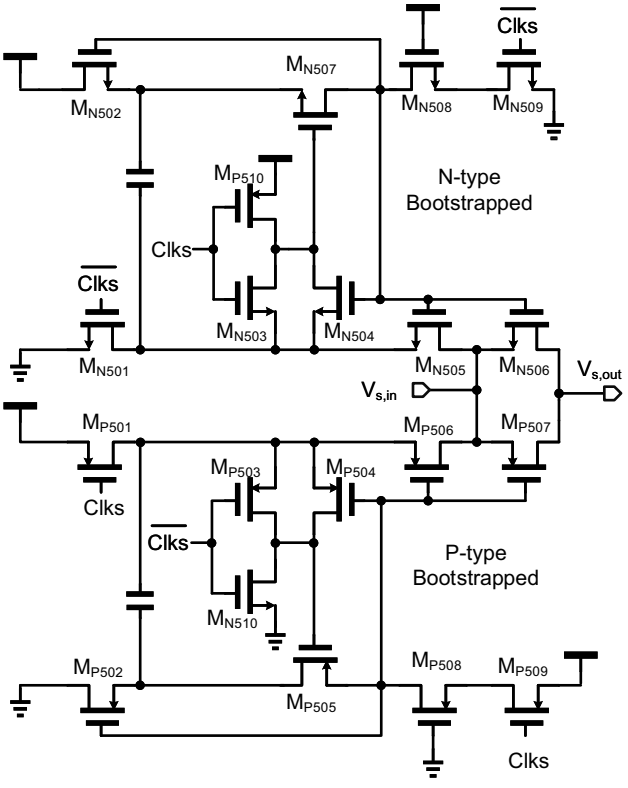

Figure 6. Bootstrapped switch schematic based on .Cheng and Tang (2015)

2.4. Comparator

One of the key R ADC are latch comparators. Non-idealities in a comparator will affect the ENOB and conversion speed of the SAR ADC. The non-idealities include kickback noise, clock feed-through, offset voltage, thermal noise, etc. Offset voltages are caused by mismatch and process variation. It can be reduced by means of calibration (Miyahara et al., 2008; Sathishkumar & Saravanan, 2018). Increasing the transistor size can be used to minimise thermal noise. However, it can result in higher kickback noise as well as clock feed-through. Kickback noise can destroy the analog input signals via capacitive path to the digital output. Isolation amplifiers are normally added to the comparator to partially reduce these problems. Kazeminia and Mahdavi (2019); Kazeminia et al. (2015) reported the usage of small-amplitude control signals to manage the operations of the comparator.

A dynamic comparator is used in this investigation for lower energy consumption, since this type of comparator does not generate bias currents when not in used to save static power consumption. The comparator is an integral part of the SAR ADC. Comparators suited for SAR ADC are those featured with low power consumption and high accuracy such as the dynamic comparator shown in Figure 7 (Liu et al., 2010). The advantage of this architecture is that when comparison is not required, it does not generate bias currents thus saving energy. This, however, has a problem of dynamic offset that can affect the performance resulting in a decrease in conversion linearity. One drawback in dynamic comparators is that some portions of the previous output remains in the comparator. A reset switch reported by Kazeminia and Mahdavi (2019) and Kazeminia et al. (2015) is added to the dynamic comparator to avoid this problem. The reset switch forces the differential output of the comparator be at zero volt between them. The comparator in Figure 7 has the same feature. Transistors MN603 and MN604 act as the reset switches to force the cross-coupled transistors to the ground when the comparator is turned off. This removes residual charges to affect the result before comparison. A rail-to-rail input range preamplier is coupled to the dynamic comparator to reduce this dynamic offset. The preamplifier is made up of parallel p- and n-type differential pairs to increase common-mode rejection capability by the sample-and-hold switches and the capacitor arrays (Hong & Lee, 2007). The schematic of the preamplifier is shown in Figure 8.

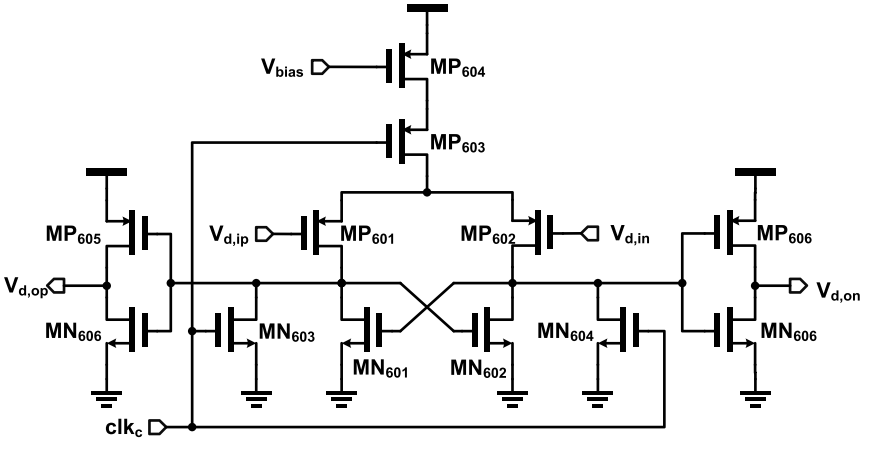

Figure 7. Dynamic Comparator.

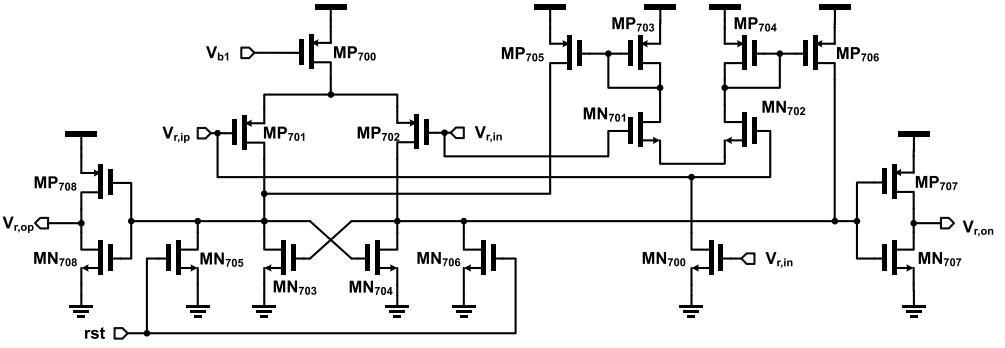

Figure 8. Railt-to-Rail preamplifier.

2.5. SAR control logic

Although the proposed design uses the split-capacitance topology, the control algorithm is much easier than that used in the traditional split-capacitor architectures because of the use of the unity-gain buffers. The SAR control logic circuit is shown in Figure 9. It is composed of a shift-register to serve as the state register controlling the data output buffers, and also the MSB and LSB array switches during the conversion. A 10-bit shift register consisted of positive edge-triggered D flip-flops with asynchronous set and reset inputs serves as the control circuit. Each flip-flop represents a state during each bit conversion, for example, S9 represents conversion for bit D9, and so on. The output buffer is controlled through its set input, turning the designated flip-flop on and outputs the resulting comparison result. The process repeats until D0 is obtained. Then, eoc (end of conversion) then becomes logic high indicating that the conversion has ended. After another Clkc cycle, the rst, namely reset signal, will be low to clear all the flip-flops ready for the next conversion.

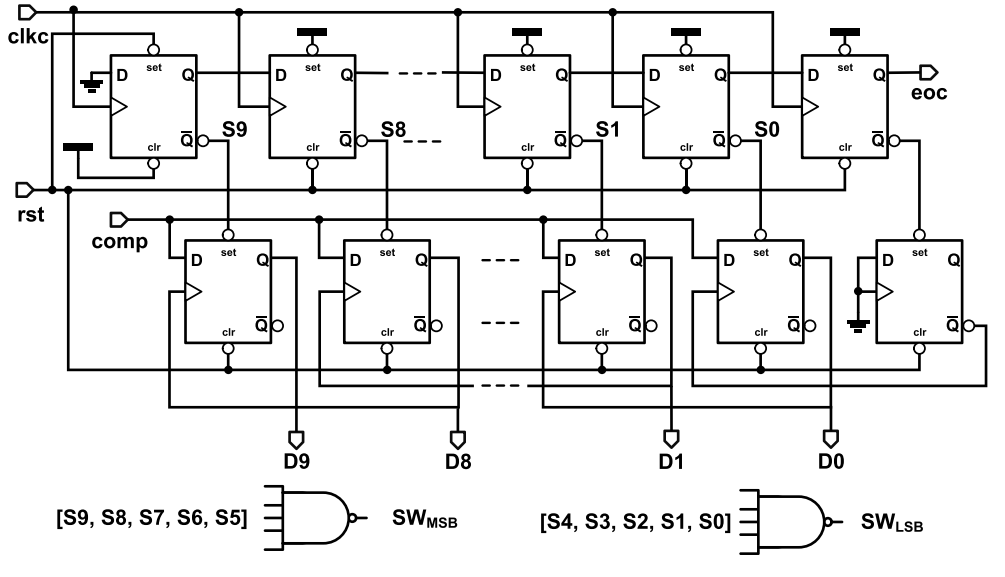

Figure 9. SAR control logic circuit.

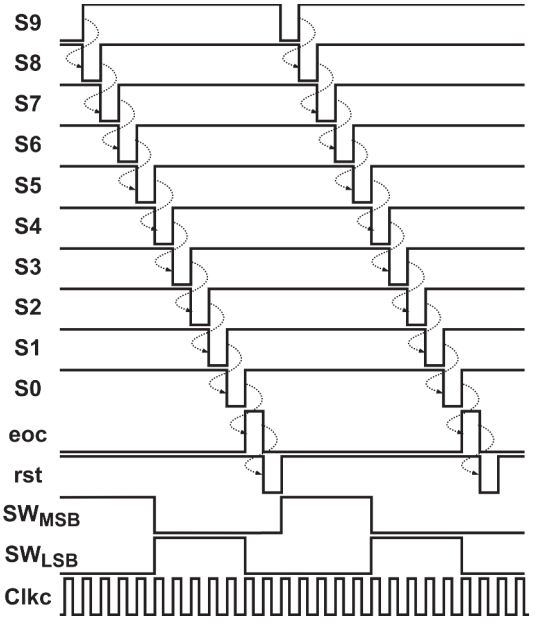

Figure 10. SAR control logic illustrative waveform.

Figure 10 shows an illustrative SAR control waveform. It shows the different state signals S9 ~ S0 along with other control signals. The signals SW $_{MSB}$ and SW $_{LSB}$, represents the coarse and fine conversion, respectively. The process took approximately 12 Clkc cycles per conversion.

2.6. Unity-gain buffer

Figure 11 shows the amplifier design used in the unity-gain buffer (Razavi, 2017). It has a very large input impedance to isolate any feedback signals coming from the LSB Array

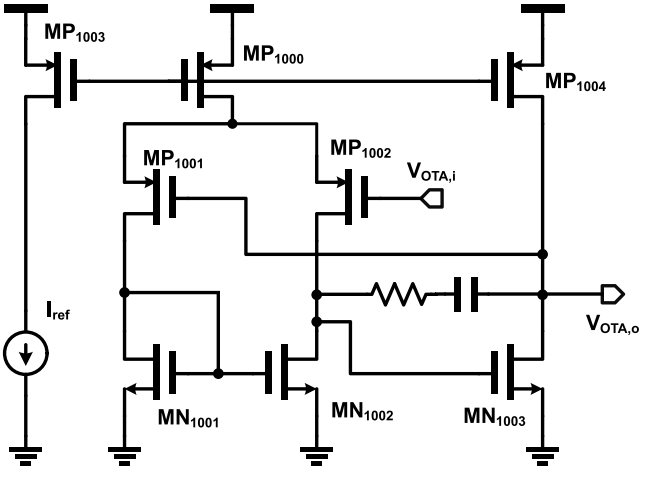

Figure 11. OTA schematic for the unity gain buffer.

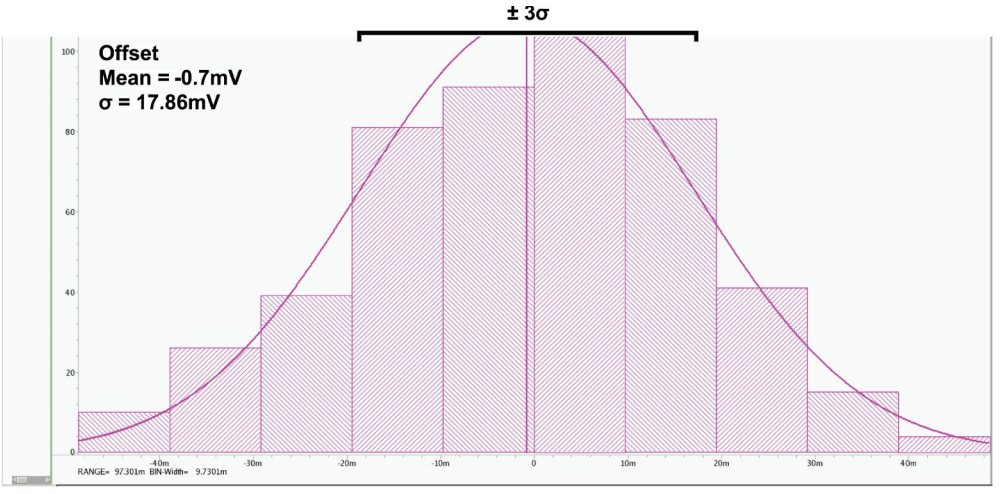

Figure 12. Monte carlo simulation (run = 500) of offset voltage of the unity gain buffer.

for accurate conversion. The unity-gain buffer proposed is composed of a cascaded operational transconductance amplifier with a 48-dB gain and a 179.1 MHz gain-bandwidth product at the typical-typical (TT) corner, 25 ° C, 0.9 V supply. The circuit is used to replace the bridge capacitor in traditional split-capacitor arrays. This configuration is a better way of splitting the capacitance in split-CDAC. This also made it possible to use a less complex control logic. Sampling is done synchronously for both arrays, therefore achieving the purpose of lowering the capacitor array size and reducing the unit capacitance.

One of the important parameters that affects the LSB array of the design is the offset voltage of the unity gain buffer, if it fed through the array. Theoretically, an offset voltage equal to $V_{ref}/2^5$ will produce at least 32 LSB error in the INL, DNL, or even the gain error of the array. The amplifier used for the unity gain buffer is simulated to generate 4.83 mV offset without the feedback. This offset can be reduced during operation by the Miller compensation using continuous-time feedback as proposed by Phan et al. (2005). A large RC filter was used as a feedback loop to cancel the DC offset caused by the amplifier. Figure 12 shows a 500 run Monte Carlo simulation of the offset voltage of the amplifier used as the unit buffer. It shows that both 0.7 mV mean and the worst case 17.86 mV offset voltage are less than $V_{ref}/2^5$ (= 28.125 mV) without Miller compensation.

3. Implementation and verification

The proposed SAR-ADC design is implemented using a typical 40-nm CMOS process. Figure 13 shows the overall layout of the design with 536.2 $\times$ 531.88 μm^2 area. Figure 14 (a-b) shows the MSB and LSB capacitor array layout floorplan, respectively, which were drawn in a symmetric way to have better matching and minimised unwanted effects due to process variations. The unit capacitance is a 3 fF MOM (Metal-Oxide-Metal) capacitor measuring 4.37 $\times$ 4.37 μm^2. Cn ($n = 1, 2, \cdots, 10$) refers to the nth capacitor while D denotes the dummy capacitors that are all connected to ground.

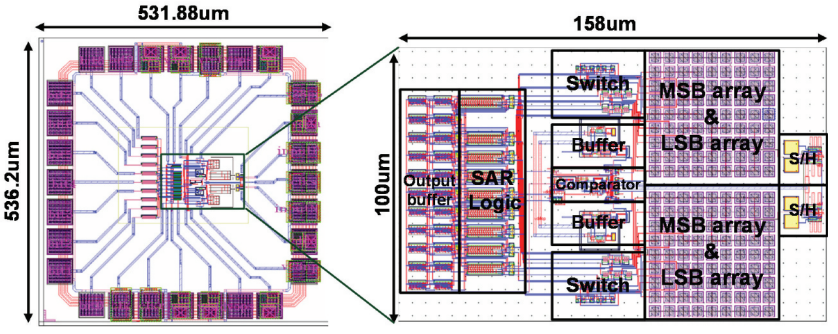

Figure 13. Layout of the proposed design.

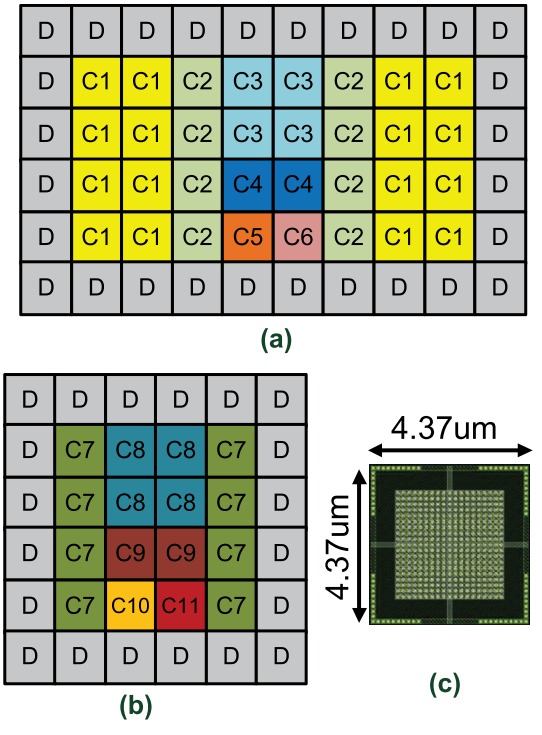

Figure 14. Layout floorplan of (a) MSB; (b) LSB capacitor array; (c) the layout view of the unit capacitor.

Figure 14(c) shows the layout view of the unit capacitor. To have a good performance of the capacitor array, the unity gain buffer must have a bandwidth of at least 25 MHz considering the 50 MS/s sampling frequency. Figure 15 shows the Bode plot of the amplifier used for the unity gain buffer. It shows a bandwidth of approximately 200 MHz with a 60 ° phase margin.

The worst-case INL and DNL are 0.56 and 0.51 LSB are shown in Fig. 16 and 17, respectively. The SAR ADC dynamic characteristic is also presented in the frequency domain through SNDR (Signal-to-Noise Distortion Ratio) and SFDR (Spurious-Free

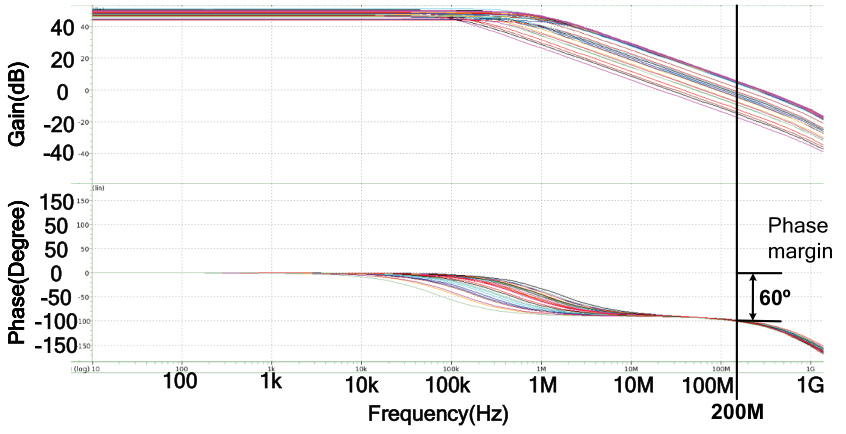

Figure 15. Bode plot of the unity gain buffer.

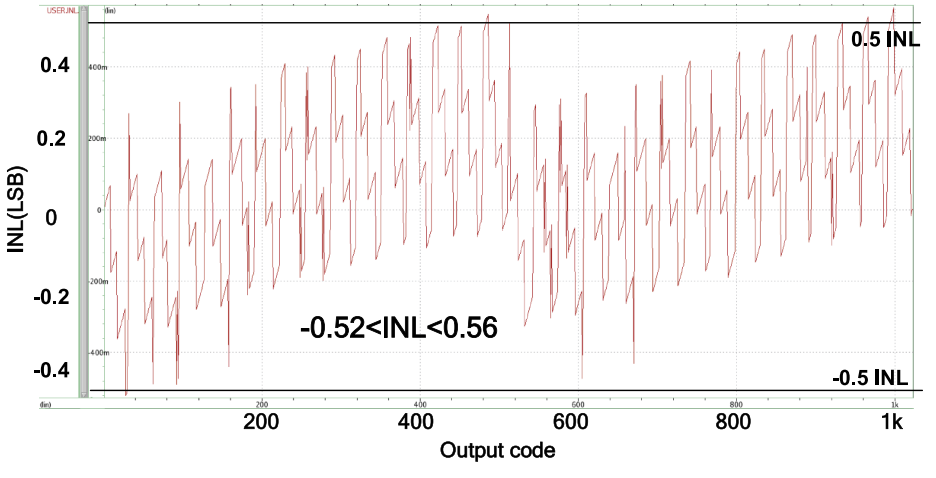

Figure 16. Worst-case simulated INL.

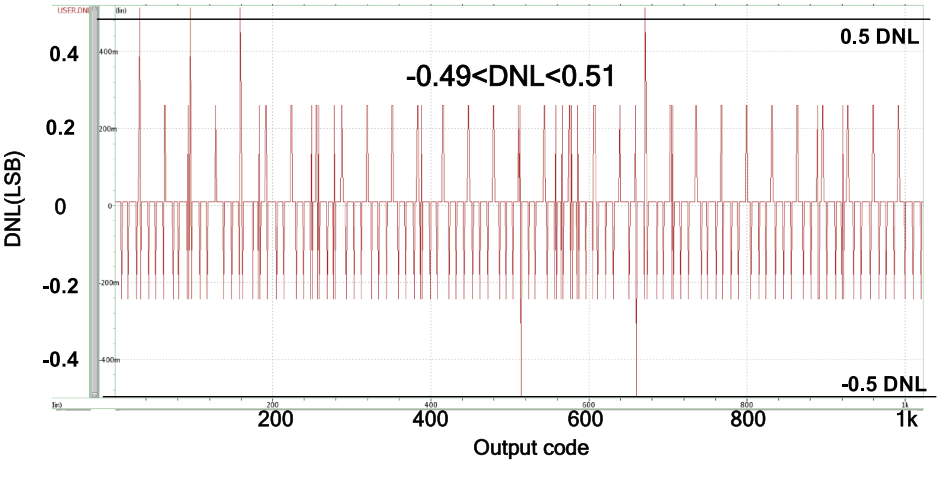

Figure 17. Worst-case simulated DNL.

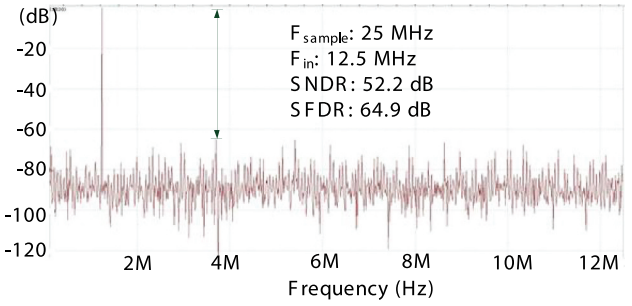

Figure 18. Frequency spectrum at 25 MS/s by all-PVT-corner post-layout simulation.

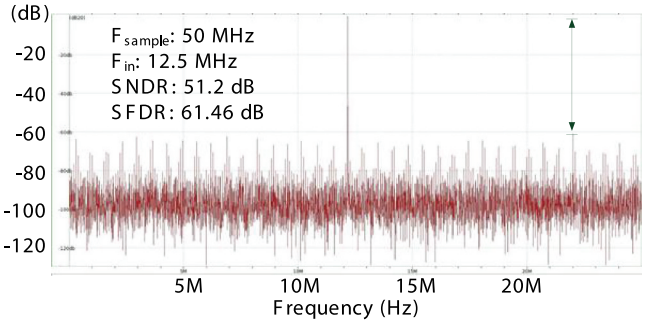

Figure 19. Frequency spectrum at 50 MS/s by all-PVT-corner post-layout simulation.

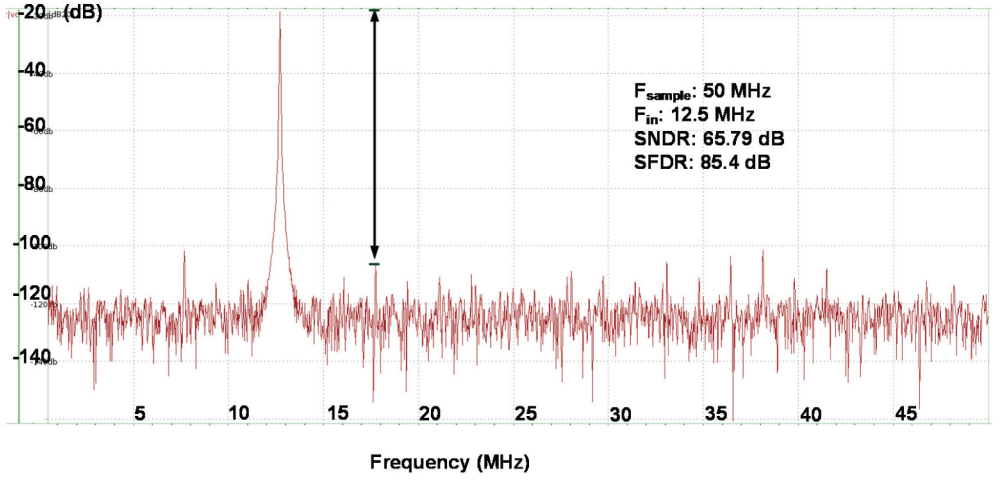

Figure 20. Frequency spectrum at 50 MS/s with an input of 12.5 MHz by all-PVT-corner post-layout simulation. (near Nyquist frequency).

Dynamic Range) visualised via the FFT spectrum. As shown in Figure 18, for a sampling rate of 25 MS/s, the SNDR and SFDR are 52.2 and 64.9 dB, respectively. For a sampling frequency of 50 Ms/s, the SNDR and SFDR are 51.2 and 61.46 dB, respectively, as shown in

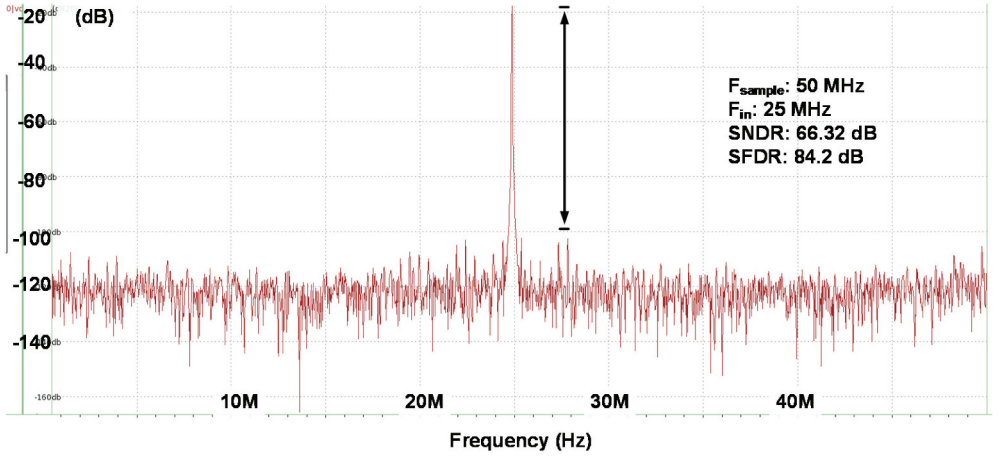

Figure 21. Frequency spectrum at 50 MS/s with an input of 25 MHz by all-PVT-corner post-layout simulation. (near Nyquist frequency).

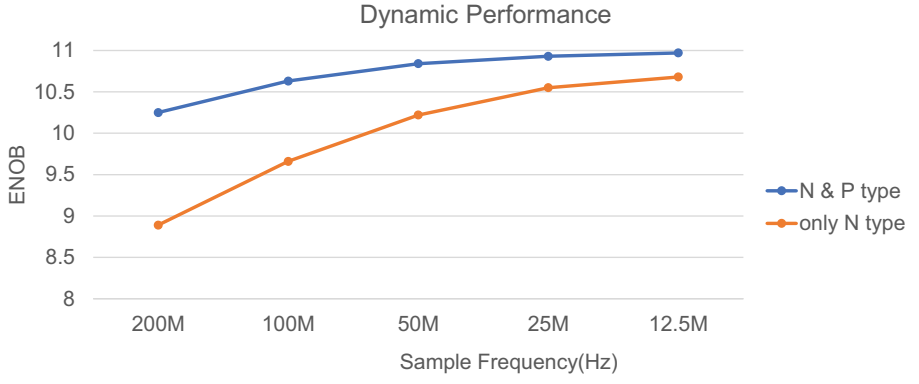

Figure 22. Bootstrapped switch dynamic performance.

Figure 19. For both simulations, the input signal is operating at 12.5 MHz frequency. Figure 20 and 21 shows frequency plots near the Nyquist frequency operating at 12.5 MHz and 25 MHz input, respectively.

Figure 22 shows the dynamic performance of the bootstrapped switches. It can be seen that using only N-type switch will not be good enough to obtain a high enough sampling rate near the Nyquist frequency. Hence, a good switch conductivity is improved by the use of complementary boosting. It can be seen from Figure 22 that the ENOB is $>$ 10 bits when the frequency is close to 50 MHz.

The performance comparison with other previous ADC works is summarised in Table 2. The proposed design consumes 120 μW overall power at 12.5 MHz, including the power used by the output buffers to drive a load of 60 pF. The comparator, unity-gain amplifiers, and SAR-Logic circuit consume 8 μW, 80 μW, and 10 μW of power, respectively. If the unity-gain amplifier is only used for fine-conversion mode, the power consumption can

Table 2. Comparison with several prior ADC works.

Publication	PRIME [1]	MWSCAS [2]	NORCAS [3]	ASSCC [4]	ISCAS [5]	AICSP [6]	EL [7]	TCAS-II [8]	Ours IJE
Year	2015	2015	2016	2016	2017	2019	2020	2020	2022
Verification	Simu.	Simu.	Simu.	Meas.	Simu.	Simu.	Meas.	Meas.	Simu.
Technology (nm)	90	65	180	45	130	500	180	40	40
V_{DD} (V)	1.8	1.2	1.8	1.1	1.2	5.0	1.8	1.0	0.9
Output Load (pF)	1.3	–	–	–	600	–	–	–	60
Resolution (bits)	10	12	8	10	8	14	12	12	10
Sampling Rate (MS/s)	150	20	1000	800	1000	17	50	12	50
Max. Freq. (MHz)	75	9.82	0.0043	400	491.2	8.5	10	1.4	25
SNDR (dB)	53	69.6	83	48	46.2	80	64.3	28.1	51.23
SFDR (dB)	60	71.6	95.7	56	56.5	95	–	72	61.46
ENOB (bits)	8.51	11.26	13.53	7.68	7.39	13.08	10.39	9.36	9.79
Power (mW)	15	2.1	0.0018	9.8	3.88	20.6	4.73	1.9	0.12
Core Area (mm^2)	–	–	–	0.015	0.018	1.7	0.017	0.013	0.015
Overall Chip Area (mm^2)	–	–	–	0.15	–	–	0.17	0.013	0.285
FOM * (fJ/step)	275	43.9	15.38	59.73	23.13	139.94	70.56	24.56	**2.71**

Note: * FOM $= \frac{\text{Power}}{\text{fs}\cdot 2^{\text{ENOB}}}$ (fJ/conv. step).
[1] (Elkafrawy et al., 2015)
[2] (Li et al., 2015)
[3] (K. K. Chen et al., 2016)
[4] (Song et al., 2016)
[5] (Zahrai et al., 2017)
[6] (song et al., 2016)
[7] (Park et al., 2020)
[8] (Roh et al., 2020)

be further decreased. The proposed design has the best performance in terms of required energy per conversion step according to the FOM comparison.

4. Conclusion

A 50-MS/s 10-bit SAR ADC is proposed for use in fibre optic gyroscope (FOG) systems in this study. The capacitor arrays are split employing unity gain buffers. The linearity of the capacitor array is improved with the addition of the unity gain buffers. Furthermore, the bridge capacitor's process variations are avoided. Also, the settling time and the size of the capacitor array are decreased. As a result, each conversion step has a conversion energy of 2.71 fJ.

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Disclosure statement

No potential conflict of interest was reported by the author(s).

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