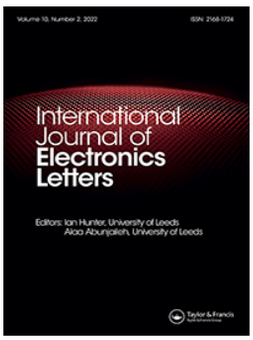

International Journal of Electronics Letters

ISSN: (Print) (Online) Journal homepage: https://www.tandfonline.com/loi/tetl20

Single-chip DC–DC buck converter design based on PWM with high-efficiency in light load

Chua-Chin Wang, Oliver Lexter July A. Jose, Pang-Yen Lou, Chung-Jye Hsu, Lean Karlo S. Tolentino & Ralph Gerard B. Sangalang

To cite this article: Chua-Chin Wang, Oliver Lexter July A. Jose, Pang-Yen Lou, Chung-Jye Hsu, Lean Karlo S. Tolentino & Ralph Gerard B. Sangalang (2022): Single-chip DC–DC buck converter design based on PWM with high-efficiency in light load, International Journal of Electronics Letters, DOI: 10.1080/21681724.2022.2068661

To link to this article: https://doi.org/10.1080/21681724.2022.2068661

Published online: 11 May 2022.

INTERNATIONAL JOURNAL OF ELECTRONICS LETTERS
https://doi.org/10.1080/21681724.2022.2068661

Taylor & Francis
Taylor & Francis Group

Single-chip DC–DC buck converter design based on PWM with high-efficiency in light load

Chua-Chin Wang[a,b], Oliver Lexter July A. Jose[a], Pang-Yen Lou[a], Chung-Jye Hsu[a], Lean Karlo S. Tolentino[a,c] and Ralph Gerard B. Sangalang[a,d]

[a]Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan; [b]Institute of Undersea Technology, National Sun Yat-Sen University, Kaohsiung, Taiwan; [c]Department of Electronics Engineering, Technological University of the Philippines, Ermita, Philippines; [d]Department of Electronics Engineering, Batangas State University, Batangas City, Philippines

ABSTRACT

This research illustrates a DC–DC buck converter with a pulse width modulation (PWM) feedback control loop and capable of power supply voltage range from VDD to 2.5× VDD, which is equivalent to 5–14 V. It is a single chip with area of 1.379 × 0.813 mm^2 using 0.5 μm HV CMOS process, where high voltage (HV) MOSFETs, a Dead-time detector, a PWM feedback loop, a control circuit and HV driving transistors are included. The main feature of our design is its capability of shutting off an optimal number of power MOSFETs during light load operation, resulting in a very high conversion efficiency. Most important of all, the optimal solution is analytically proved. The light load efficiency is raised from 31.71% by traditional methods to 67.94% by the proposed design.

ARTICLE HISTORY
Received 15 November 2021
Accepted 18 April 2022

KEYWORDS
DC-DC converter; buck converter; PWM; high voltage; light load

1. Introduction

Because of fast-paced evolution of semiconductor technologies, transistors as well as semiconductor devices are downsized rapidly and constantly. Transistor operating voltages are also reduced from 5 V to 3.3 V, 1.8 V, or even lower. Nevertheless, the operating voltage of existing or prior systems might be still 5 V, 12 V, or even higher. Therefore, DC–DC voltage converters are often required in many applications to supply and support lower operating voltages for devices fabricated by more advanced processes. The development of the converter and its control method are the power supply guarantee to its stability and precision.

Two of the most popular types of voltage converters are 'Switching Mode Power Supply (SMPS)' type (Whittington et al., 1992) (Mahmud et al., 2018) and 'Low Drop-Out Linear Regulator (LDO)' type (Rinc´on-Mora & Allen, 1998; Crepaldi et al., 2010). Traditionally, two SMPS methods have been reported to achieve the controller mechanism, i.e. 'Pulse-Frequency Modulator (PFM)' and 'Pulse-Width Modulator (PWM)' (Chen et al., 2017; Wang et al., 2011).

CONTACT Chua-Chin Wang ccwang@ee.nsysu.edu.tw Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan

Table 1. Control method comparison.

	PWM	PFM	PWM/PFM
Switching speed	Fast	Slow	Average
Output ripple	Small	Large	Average
Light load efficiency	Low	High	High
Compensation network difficulty	Low	Average	High
Cost	Low	Low	High

PWM is the earliest proposed control method, which compares with a reference voltage and the feedback voltage to adjust the duty cycle of the control signal and regulate the output of the DC–DC converter to achieve the auto-adjustment effect. It offers the advantages of a constant output voltage, predictable switching noise and easy filtering. However, due to the fixed frequency and the constant power consumption of the switch, it provides poor conversion efficiency that occurs when the load is light. The introduction of PFM tackles the problem of a light load in PWM by utilising the adjustment control signal. The frequency modulation techniques reduce the switching load during conversion. It does not require a complex converter architecture; hence, it eliminates the need for a control loop compensation network. However, the slow response and large output voltage ripple due to frequency changes result in electromagnetic interference that is difficult to control on this case. Either method has its own features and problems (Yu, 2003).

Some semiconductor companies, including Texas Instruments and Linear Technology, have proposed DC–DC converters using a variety of control approaches. The cost is substantially higher when the load is primarily used to automatically alter the control technique. Shown in Table 1 is the comparisons of different control methods.

Many prior works have presented DC–DC converters that provide high light-load efficiency. An ultra-low IQ buck converter (Lu et al., 2015) has 75% efficiency in light-load and a maximum of 95% for load up to 1 mA. However, it has only a maximum input and output voltage of 6 V and 2.5 V, respectively. A removed continuously-on comparator in clocked hysteresis control (Wu et al., 2017) improved the buck converter in light load up to 90% – nevertheless, it has only a maximum input voltage of 3.3 V and output of 1.6 V. An ACC, CV and MMPT energy harvester (Wang et al., 2021) operate in 10 V to 20 V with output up to 4.2 V using PWM and PFM to improve the conversion efficiency up to 98% but with low efficiency during light-load operation.

This research presented a DC–DC converter consisting of HV MOSFETs and driving transistors, dead-time detector, PWM feedback loop and control circuit. It provides an output of 5 V with input ranging from 10 to 14 V. The converter uses external signals to control power MOSFETs during light-load conversion, increasing conversion efficiency. A 0.5 μm HV CMOS process is used in fabricating the chip. Measurement results show a maximum of 91.68% conversion efficiency and a minimum of 67.94% conversion efficiency during light load.

2. DC–DC buck converter design for light load control

2.1. Analysis of conversion efficiency

An ideal DC–DC converter's main function is to provide high efficiency, excellent line, load regulation, etc. Notably, the efficiency is the top priority among these indexes. Efficiency, as defined in Eqn. (1), is the ratio of output power and input power. The power consumption which caused by power MOSFETs and internal control circuits is the difference between output power and input power. Thus, the efficiency of DC–DC converter would be quite high for a large over-loaded output current. On the other hand, when the load is light, the internal current consumption becomes relatively large, and the efficiency of the CD–DC converter will drop significantly.

$$\eta = \frac{P_{out}}{P_{out} + P_{in}} \times 100\ \% \tag{1}$$

where P_{out} is the output power and P_{in} is the input power.

Prior methods to achieve high efficiency include pulse skip modulation, PFM and burst mode. Nevertheless, the stated methods were proven to lessen the static and switching current frequency at the expense of large ripples interfering the output voltage (Mary et al., 2014).

$$\eta = \frac{R_{load}}{R_{load} + R_{on}} = \frac{1}{1 + R_{on}/R_{load}} \tag{2}$$

2.2. Proposed DC–DC converter

Referring to Figure 1, the proposed PWM-based DC–DC converter consists of five blocks, including buck converter core, error amplifier (EA), PWM circuit, dead-time circuit and light load control circuit. Notably, power MOSFET groups, including PMOS1 (HVP1), PMOS2 (HVP2), NMOS1 (HVN1) and NMOS2 (HVN2), are all HV devices provided by the foundry HV process, which can be integrated on silicon together with other circuits.

2.3. Buck converter core

For the sake to generate large output currents, this architecture uses synchronous rectification to reduce the loss of forward voltage drop caused by the traditional diode approach. The buck converter core in Figure 1 is composed of many power MOSFETs and those off-chip discretes, including L_{big} and C_{big}. When VC p and VC n are both low to turn on PMOS and shut off NMOS, MOSout must be equal to Vin to charge the off-chip inductor, L_{big}. As soon as those two control signals flip the states of PMOS and NMOS, inductor L_{big} starts discharging to pull down MOSout to ground. Therefore, by modulating the turn-on time of these power MOSFETs, namely duty cycle D, the output voltage is predictable as follows.

$$V_{out} = V_{in} \times \frac{D}{1 - D} \tag{3}$$

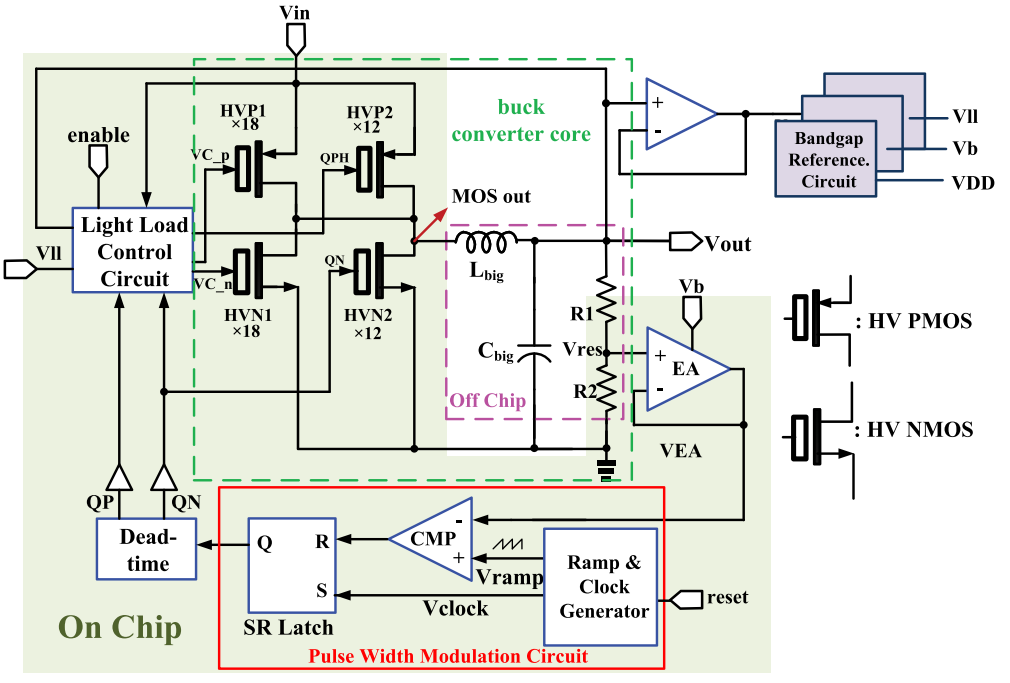

Figure 1. Proposed PWM-based DC–DC converter.

Also, EA is used to keep track the output voltage. As a consequence, PWM block plays the role of negative feedback control to stabilise the output voltage and reduce the ripple thereof. Dead-time circuit ensures that power PMOS and NMOS would not be turned on at the same time such that the unwanted DC power dissipation is reduced and the overall efficiency is boosted, since the timing control of the power MOSFET gate drives is critical. In addition, the limited bandwidth can filter high frequency signals to prevent small signals or noise from system oscillations.

The dead-time circuit is composed of an OR gate and an inverter in series. When the signal passes inverters, there would be an RC delay. The control signal Q generated by the PWM generates two non-overlapping control signals through the dead-time circuit. The purpose of this is to prevent the power transistors HVP1, HVP2, HVN1 and HVN2 from being turned on at the same time to avoid additional losses and improve conversion efficiency.

2.4. Light load control circuit

Light load control circuit is the feature of the proposed converter design. Referring to Figures 1 and 2, high voltage buffer raises the control signal QPH and VC p to the input voltage for completely turning off the P-type power MOS to prevent excess power loss. The major energy losses, i.e. conduction loss and switch loss, are formulated as Eqn. (4), (5), (6), (7; Kim & Rinc´on-Mora, 2009; Park et al., 2015; Mary et al., 2014).

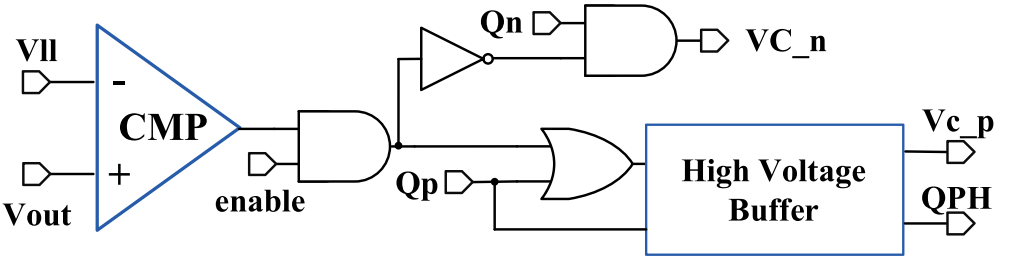

Figure 2. Light load control circuit.

$$\text{Conduction Loss} = \left\{ I_o^2 + \frac{\left[d_{mp}(1-d_{mp})V_{in}\right]^2}{12 \cdot L_{big}^2 \cdot F_{sw}^2} \right\} R_{on} \tag{4}$$

$$\textit{Switch Loss} = C_{g,eq} \cdot V_{in}^2 \cdot F_{sw} + I_o \cdot F_{sw} \cdot \left[(V_{in} + 2 \cdot V_{DN}) \cdot t_{over} + 2 \cdot V_{DN} \cdot t_{DT}\right] \tag{5}$$

$$R_{on} = \frac{L}{\mu_p \cdot C_{ox} \cdot W \cdot V_{od}} \tag{6}$$

$$C_{g,eq} = W \cdot L \cdot C_g \tag{7}$$

where W is the width and L is the length of the MOSFETs, C_{ox} is the gate oxide capacitance, F_{sw} is the switching frequency, d_{mp} is the duty cycle of PMOS, V_{DN} is the diode voltage, t_{over} is the overlap time, t_{DT} is the dead time and V_{od} is the overdrive voltage. Apparently, the loss of the DC–DC buck converter load is dominated by switch loss in a light load scenario. Therefore, one strategy of high efficiency is to reduce the frequency in such a scenario to cut the loss, which is the theoretical base of PFM. However, the control circuit of this strategy will be very complicated. Another approach is to reduce $C_{g,eq}$. The design of this research adopts the latter one. That is, when the converter detects the light load operation, certain power MOSFETs are shut off to minimise $C_{g,eq}$ and consequently reduce the switching loss. Therefore, the loss analysis is then simplified as follows.

∵ t_{over}, t_{DT} and V_{DN} are small, Switch Loss ≅ $C_{g,eq} \cdot V_{in}^2 \cdot F_{sw}$

∴ Power Loss = Conduction Loss + Switch Loss

$$P_{loss} = \left\{ I_o^2 + \frac{\left[d_{mp}(1-d_{mp})V_{in}\right]^2}{12 \cdot L_{big}^2 \cdot F_{sw}^2} \right\} R_{on} + C_{g,eq} \cdot V_{in}^2 \cdot F_{sw} \tag{8}$$

By Eqn. (6) and (7), power loss is re-organised as follows.

$$\begin{aligned} \text{Power Loss} = {} & \textit{Ploss, tot} \\ = {} & \left\{ I_o^2 + \frac{\left[d_{mp}(1-d_{mp})V_{in}\right]^2}{12 \cdot L_{big}^2 \cdot F_{sw}^2} \right\} \frac{L}{\mu_p \cdot C_{ox} \cdot W \cdot V_{od}} + W \cdot L \cdot C_g \cdot V_{in}^2 \cdot F_{sw} \end{aligned} \tag{9}$$

$P_{loss,tot}$ is simplified as follows.

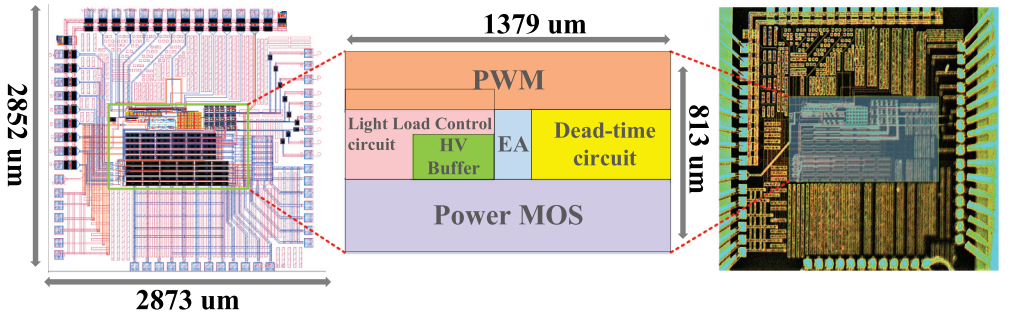

Figure 3. Layout and diephoto of the proposed converter.

$$P_{loss,tot} = \alpha \frac{1}{W} + \beta W \tag{10}$$

where $\alpha = \left\{ I_o^2 + \frac{\left[d_{mp}\left(1-d_{mp}\right)V_{in}\right]^2}{12 \cdot L_{big}^2 \cdot F_{sw}^2} \right\} \frac{L}{\mu_p \cdot C_{ox} \cdot V_{od}}, \beta = L \cdot C_g \cdot V_{in}^2 \cdot F_{sw}$

Thus, the power loss will be the minimum where the slope of $P_{loss,tot}$ equals to zero.

$$\frac{d}{dW} P_{loss,tot} = 0, \Rightarrow \alpha \frac{-1}{W^2} + \beta = 0, W = \sqrt{\frac{\alpha}{\beta}} \tag{11}$$

3. Simulation and measurement

The proposed PWM-based DC–DC converter design is fabricated on silicon die using TSMC UVH 0.5 μm CMOS process, as shown in Figure 3. The chip size is 2873.075 × 2852.497 μm^2, and the core area is 1379 × 813 μm^2.

3.1. Simulation results

Figure 4 shows the post-layout simulation of the proposed DC–DC converter with an input voltage of 13 V and output resistance (Rout) = 50 Ω. When switching to light load mode, it can be seen in the output waveform that the output voltage drops slightly. The settling time of the overall output voltage is 728 μs.

3.2. Measurement results

Figure 5 shows the measurement setup for the DC–DC converter. The ITECH IT6333A is used as a power supply. The output waveform is monitored using a Lecroy WaveRunner 610Zi, and the output voltage is measured with a Fluke 289 RMS Multimeter. An input of 13 ramp wave provides a regulated DC output voltage equal to 5.06 V, as shown in Figure 6.

Figure 7(a-d) shows regulated DC voltage, given different input of 10 V, 11 V, 12 V and 13 V, respectively.

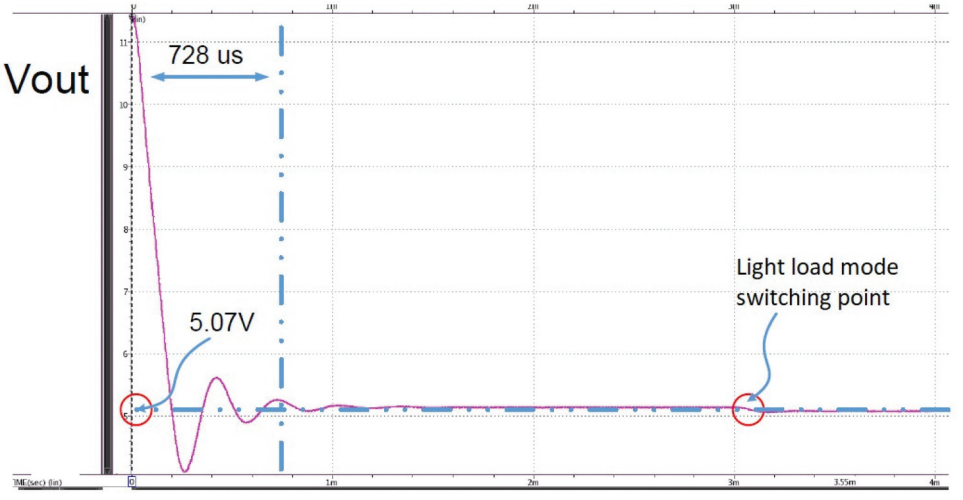

Figure 4. Post-layout simulation output waveform.

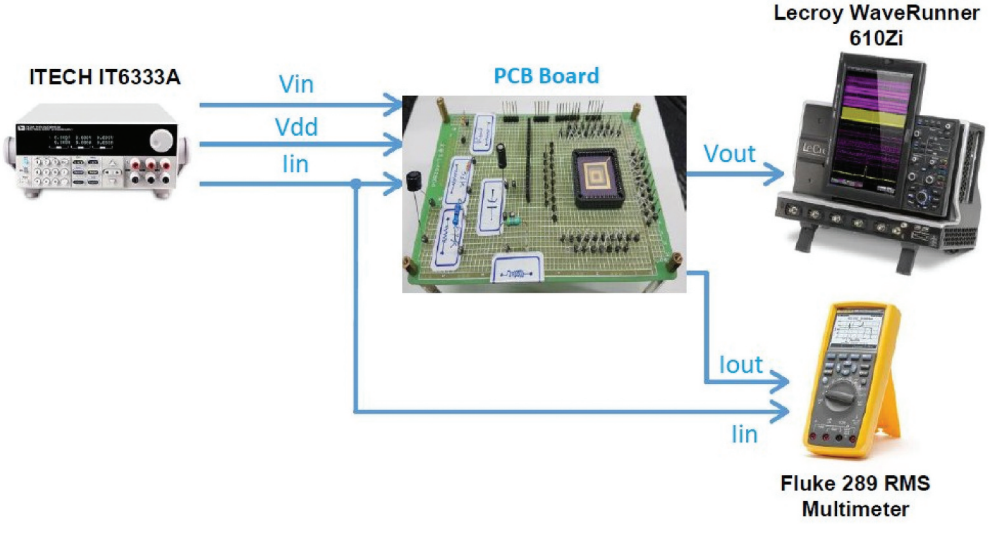

Figure 5. Measurement setup.

3.3. Performance analysis

The table of comparison between the DC–DC converter specification, post-layout simulation, and actual measurement for input and output voltage, output current and efficiency is shown in Table 2.

With reference to Figure 1, the number of power MOSFET pairs is 30 and the maximum current is set to 0.5 A.

According to Eqn. (4)-(7), the number of turn-on MOSFETs is found to affect the efficiency significantly. Apparently, an optimal number of 11 will give the highest efficiency as shown in Figure 8. By the derivation of Eqn. (8)–(11), the optimal number for power loss can be found, which is 12. The similarity of these two results justifies the

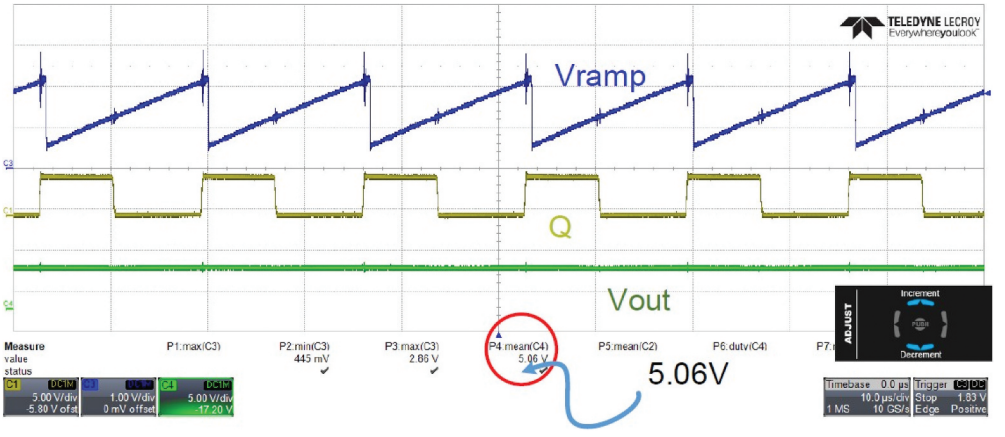

Figure 6. Output waveform (Vin = 13 V).

Table 2. Input pattern and expected output of test 1.

	Specification	Post-layout simulation	Measurement
Input voltage (V)	11 ~ 14	11 ~ 13	11 ~ 13
Output voltage (V)	5 ± 0.1	5 ± 0.1	4.96 ~ 5.04
Output current (V)	0.5	0.489	0.49
Efficiency (peak, %)	>90	91.68	69.7
Switching frequency (kHz)	60	60	60

correctness of the theory addressed in Eqn. (4)–(11). Therefore, the total 30 power MOSFETs are divided into two groups, where 18 MOSFETs are driven by the output of light load control circuit. It will be shut off if the light load is detected. The other 12 MOSFETs are directly driven by the outputs of dead-time circuit, which means they will be always on regardless the load situation.

As we addressed at the very beginning, the efficiency is the most important performance index to be enhanced. Figure 9 shows the efficiency comparison of the proposed design vs. traditional DC-DC converters with the same power MOSFETs but no light load control. When the load becomes 4 mA, our design at the worst case of all-PVT-corner simulation and on-silicon measurement still maintains 67.94% efficiency, while the traditional counterpart is 31.71% by simulation. The power dissipation of the proposed design is 110 mW at 60 KHz clock rate.

3.4. Comparison with the state of art

The overall performance of this paper in comparison with several recent DC–DC converters is tabulated in Table 3. Our design has the edge of the largest input high voltage range and the best efficiency for peak operation and light load operation. The figure of merit (FOM) is defined as follows.

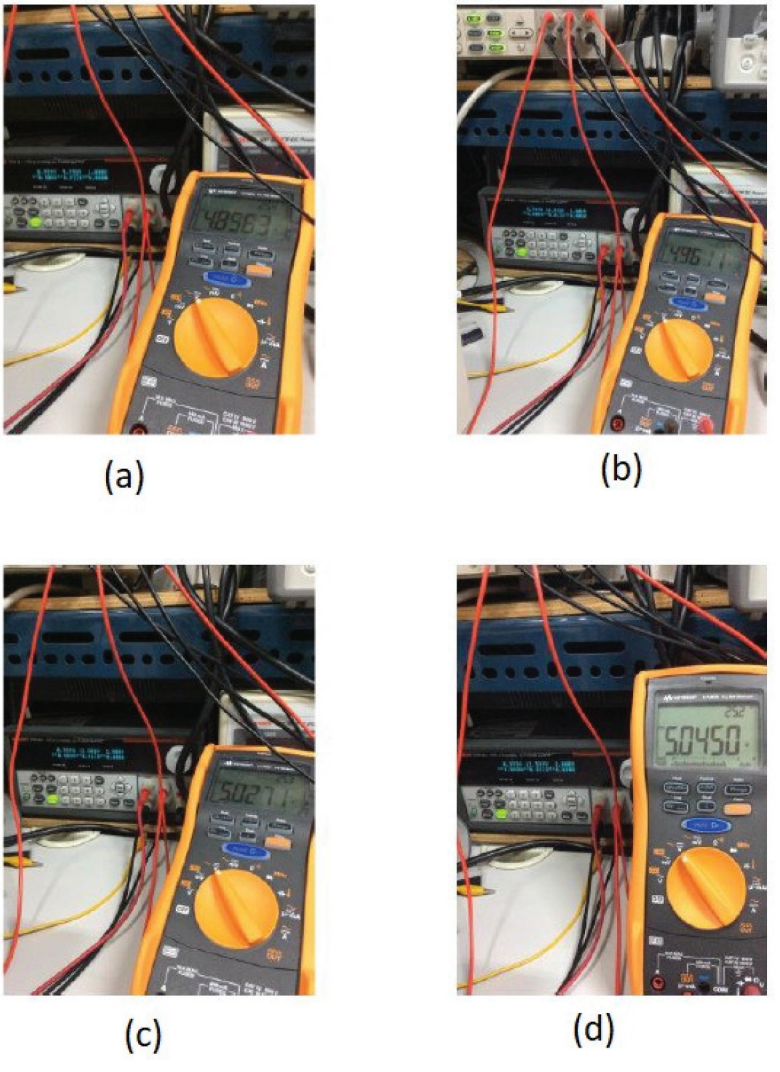

Figure 7. Regulated DC voltage for input (a) 10 V, (b) 11 V, (c) 12 V and (d) 13 V.

$$\text{FOM} = \frac{\text{Max.Input Voltage} \times \text{Max. } I_{out} \times \text{Efficiency}}{^{*}\text{Normalized Core are}} \tag{12}$$

$$^{*}\text{Normalized Core area} = \frac{\text{Core area}}{\text{Process}^2}$$

Among all the recent works, our design has the highest FOM.

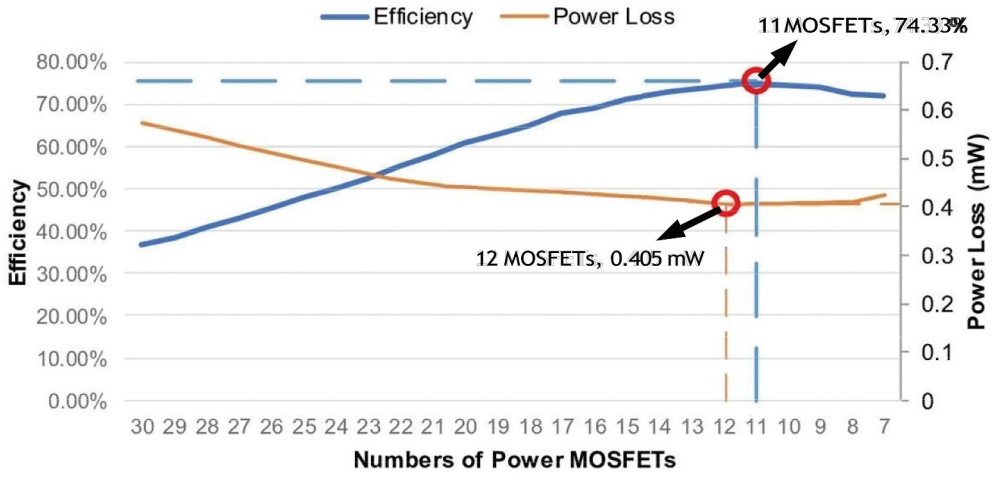

Figure 8. Efficiency and power loss vs. total number of power MOSFETs.

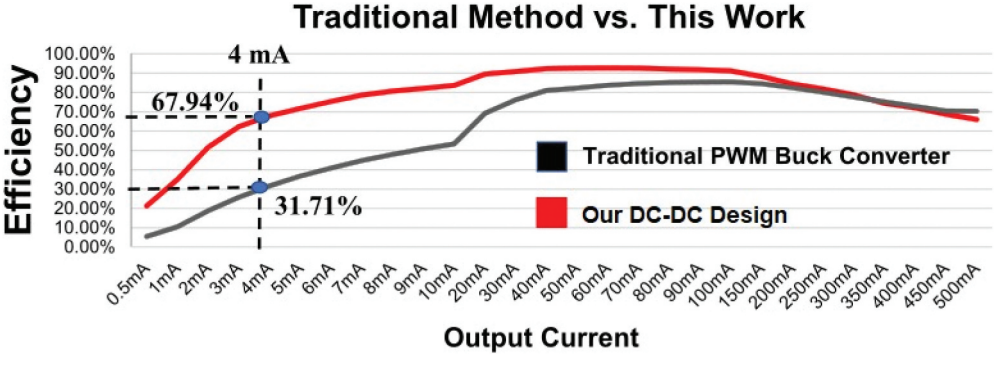

Figure 9. Efficiency comparison.

Table 3. Comparison with prior DC–DC converters.

	VLSI[a]	CICC[b]	CICC[c]	MEJ[d]	SPIES[e]	This work
Year	2015	2015	2017	2019	2020	2021
Process (μm)	0.35	0.18	0.18	0.18	0.5	0.5
Input range (V)	2.2~6	3	2.4~3.3	0.5~1	4~20	10~14
Output range (V)	2.5	1	1.5~1.6	1.8/1.2	2.5~4.2	5
Max. I_{out}	100 mA	1 uA	10 mA	40 mA	324 mA	0.5 A
Settling time	N/A	N/A	N/A	N/A	N/A	< 500 us
Efficiency (%)	95	87	90.4	91	98	91.68
Light load (%)	78	N/A	90.4	N/A	N/A	≥ 67.94
Core area (mm^2)	2.88	2.42	0.71	2.752	12.53	1.287
FOM	2×10^{-2}	3×10^{-8}	1×10^{-3}	1.3×10^{-3}	0.26	1.26

[a]Lu et al. (2015)
[b]El-Damak and Chandrakasan (2015)
[c]Wu et al. (2017)
[d]Liu et al. (2019)
[e]Lee et al., (2020)

4. Conclusion

This investigation demonstrates a novel design of DC–DC buck converter featured with the shutdown of optimal number selection of power MOSFETs when the light load operation is detected. Thanks to the reduction of the gate capacitance, the switching loss is reduced such that the efficiency is enhanced. Most importantly, the optimal light load efficiency is found by the derivation of analytic equations and then achieves the best efficiency in the given wide input voltage range. The proposed lightload control method and circuit design have been granted US patent 'DC–DC Converter' Wang and Hsu (2020), which also justifies the outstanding performance of this work.

Acknowledgments

The authors are appreciative to TSRI (Taiwan Semiconductor Research Institute) in Tainan, Taiwan, for providing EDA tool assistance and considerate chip measurement services.

Disclosure statement

No potential conflict of interest was reported by the author(s).

Funding

This work was partially supported by Ministry of Science and Technology (MOST), Taiwan, under grant MOST 110-2241-E-110-004- and MOST 110-2218-E-110-008-.

ORCID

Ralph Gerard B. Sangalang http://orcid.org/0000-0002-4120-382X

References

Chen, Y., Yu, B., Wang, J., & Li, C. (2017, October). A buck DC-DC converter with a novel PWM/PFM hybrid-mode auto-change technique. In *2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC)* (pp. 1–2). IEEE.

Crepaldi, P., Pimenta, T., & Moreno, R. (2010, December). A CMOS low drop out voltage regulator. In *2010 International Conference on Microelectronics*, (pp. 208–211). IEEE.

El-Damak, D., & Chandrakasan, A. P. (2015, June). Solar energy harvesting system with integrated battery management and startup using single inductor and 3.2nW quiescent power. In *2015 Symposium on VLSI Circuits (VLSI Circuits)*, (pp. C280–C281). IEEE.

Kim, S., & Rinc´on-Mora, G. A. (2009, August). Achieving high efficiency under micro-watt loads with switching buck DC-DC converters. *Journal of Low Power Electronics*, *5*(2), 229–240. https://doi.org/10.1166/jolpe.2009.1023

Lee, T.-J., Su, P.-K., & Wang, C.-C. (2020, September). 20V HV energy harvesting circuit with ACC/CV Mode and MPPT control for a 5 W solar panel. In *2020 2nd International Conference on Smart Energy Systems and Technologies (SPIES)*, (pp. 205–208). IEEE

Liu, L., Chen, C., Liao, X., Huang, W., Mu, J., & Zhu, Z. (2019, May). A low cross-regulation and high-efficiency SIDO boost converter with near-threshold start-up. *Microelectronics Journal*, *87*(1), 22–32. https://doi.org/10.1016/j.mejo.2019.03.010

Lu, D., Yao, S., & Shao, B. (2015, September). A 110nA quiescent current buck converter with zero-power supply monitor and near-constant output ripple. In *2015 IEEE Custom Integrated Circuits Conference (CICC)*, (pp. 1–4). IEEE.

Mahmud, M. W. B., Alam, A. Z., & Rahman, D. A. (2018, September). Improvement of active power factor correction circuit for switch mode power supply using fly back and boost topology. In *2018 7th International Conference on Computer and Communication Engineering (ICCCE)*, (pp. 437–440). IEEE.

Mary, N. M. S., Maity, A., & Patra, A. (2014, January). Light load efficiency improvement in high frequency DC-DC buck converter using dynamic width segmentation of power MOSFET. In *2014 27th International Conference on VLSI Design and 2014 13th International Conference on Embedded Systems*, (pp. 563–568). IEEE.

Park, S.-Y., Cho, J., Lee, K., & Yoon, E. (2015, December). A PWM buck converter with load-adaptive power transistor scaling scheme using analog-digital hybrid control for high energy efficiency in implantable biomedical systems. *IEEE Transactions on Biomedical Circuits and Systems*, *9*(6), 885–895. https://doi.org/10.1109/TBCAS.2015.2501304

Rinc´on-Mora, G., & Allen, P. (1998, January). A low-voltage, low quiescent current, low drop- out regulator. *IEEE Journal of Solid-State Circuits*, *33*(1), 36–44. https://doi.org/10.1109/4.654935

Wang, C.-C., Chen, C.-L., Sung, G.-N., & Wang, C.-L. (2011, May). A high-efficiency DC-DC buck converter for sub-2×VDD power supply. *Microelectronics Journal*, *42*(5), 709–717. https://doi.org/10.1016/j.mejo.2011.02.004

Wang, C.-C., & Hsu, C.-J. (2020, February 25). *DC-DC buck converter* (US Patent No.10574142B1). U.S. Patent and Trademark Office.

Wang, C.-C., Jose, O. L. J., Su, P. K., Tolentino, L. K., Sangalang, R. G., Velasco, J., & Lee, T.-J. (2021, December). An adaptive constant current and voltage mode P&O-based maximum power point tracking controller IC using 0.5-*μm HV CMOS*. *Microelectronics Journal*, *118*(1), 105295. https://doi.org/10.1016/j.mejo.2021.105295

Whittington, H. W., Flynn, B., & Macpherson, D. (1992). *Switched mode power supplies: Design and construction*. Research Studies Press.

Wu, C.-S., Takamiya, M., & Sakurai, T. (2017, May). Buck converter with higher than 87% efficiency over 500nA to 20mA load current range for IoT sensor nodes by clocked hysteresis control. In *2017 IEEE Custom Integrated Circuits Conf. (CICC)* (pp. 1–4).

Yu, T.-Y. (2003). *A high-efficiency synchronous CMOS switching regulator with PWM/PFM-Mode Operation*. (M.S. Thesis). National Chiao-Tung University.