Tutorial: Design of High-Speed Nano-Scale CMOS Mixed-Voltage Digital I/O Buffer With High Reliability to PVTL Variations

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(Invited Paper)

***Abstract*—Ever since the reliability issues caused by I/O (input/output) compatibility among chips fabricated using different processes were raised during mid-2000, on-silicon mixed-voltage I/O buffer with wide voltage tolerance has been considered a better solution than using signal level converters to shrink PCB size, number of discretes, and power consumption. However, various external voltages on I/O pad result in body effect, leakage, hot-carrier degradation, and gate-oxide overstress in stacked transistors of mixed-voltage I/O. What even worse is that slew rate (SR) was also found deteriorated by PVT (Process, Voltage, Temperature) variations. A complete mixed-voltage I/O buffer design flow using nano-scale CMOS processes will be introduced in this tutorial based on previously developed buffers. Besides circuit design methodology, the reliability design consideration for the buffers, including ESD, PVT detection, and slew rate auto-adjustment will be discussed as well.**

***Index Terms*—Digital I/O buffer, mixed-voltage mode, PVTL detection, slew rate, auto-adjustment.**

I. Introduction

THANKS to the fast CMOS technology development toward nano-scale nodes recently, lower fabrication cost, lower supply voltage, and lower power consumption for electronic products are achieved. However, many PCB-based systems are still equipped with chips fabricated by prior CMOS processes using different digital voltage levels, e.g., 1.8, 3.3, or even 5.0 V. Thus, the digital data exchange among chips fabricated by different generations of CMOS nodes becomes an issue. Though it can be resolved by adding level converters, the penalty is extra area overhead, circuit complexity, and power consumptions. Therefore, an I/O buffer with mixed voltage tolerance, as shown in Fig. 1, has been deemed as another solution to exchange signals with different logic voltage levels [2], [3], [4], [21].

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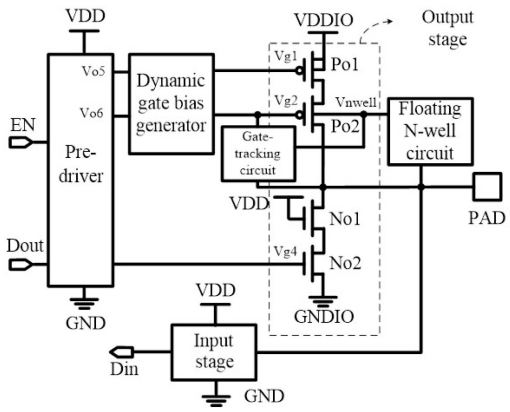

Fig. 1. An exmaple of prior mixed-voltage I/O buffers [21].

Many researches have identified some problems of these mixed-voltage buffers, including compatibility of multiple voltage level [21], [33], SR adjustment [22], [23], [24], [25], and reduction of PVT variation and leakage impact [26], [28], [29], [30], [31], [32]. Meanwhile, ESD issue of nano-scale I/O buffers has also drawn attention [21], [27]. Particularly, SR demand becomes very hard for the nano-scale CMOS buffers to meet certain interfacing standards, e.g., DDR4. PVT variations are unavoidable issues, which will directly result in ΔSR, where ΔSR is the range of SR affected by these variations. Therefore, SR auto-adjustment circuit is usually combined with PVT detectors to minimize the SR variations. Last but not least, the leakage starts deteriorating the performance of I/O buffers fabricated by advanced nano-meter technologies. One of the features of this tutorial is a leakage detection circuit and the associated compensation mechanism are included to reduce various leakage impact on the buffer.

This tutorial based on mixed-voltage I/O buffer designs developed over 10 years [1]–[20] means to demonstrate how a reliable mixed-voltage I/O buffer is developed so that readers can easily follow and stay away all of the mentioned issues.

II. Nano-Scale Mixed-Voltage Digital I/O Buffer Design

As shown in Fig. 2, a nano-scale mixed-voltage digital I/O buffer comprises one outward path and one inward path. The

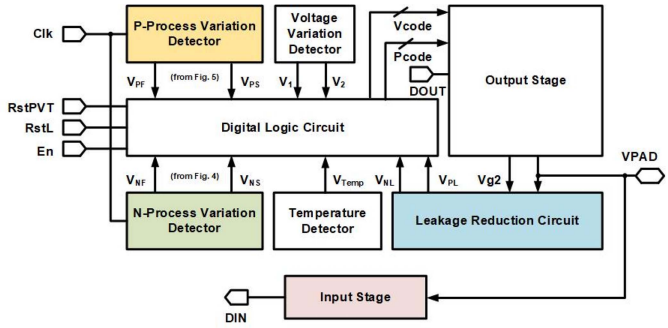

Fig. 2. Generic nano-scale mixed-voltage digital I/O buffer.

TABLE I
COMPARISON OF VARIATION FACTORS ON SLEW RATE

VDD (V)	Corners	Temp. (°C)	ΔRise (V/ns)	ΔFall (V/ns)	Ratio (Rise/Fall)
1±0.1	TT	25	2.08	1.93	4.1/3.64
1	others	25	1.78	1.74	3.63/3.28
1	TT	0-100	0.49	0.53	1/1

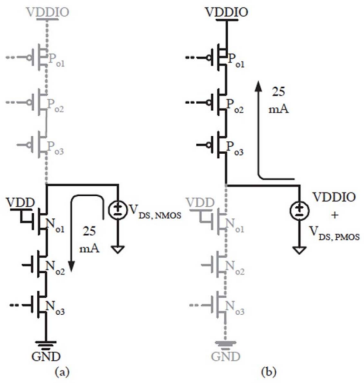

Fig. 3. Equivalent ESD circuit model [5].

former consists of several detectors, namely Process Variation Detector, Temperature Detector, Voltage Variation Detector and Leakage Detector, Digital Control Circuit, and Output Stage. The latter, by contrast, is composed of an Input Stage, perhaps with a calibration logic. All these circuits will be briefly introduced and designed step by step.

A. Design Considerations

Cost and performance are hard to be attained at the same time for an I/O buffer design. Several tradeoffs might be considered before the realization, assuming the CMOS technology node is already selected.

• Is anti-temperature variation needed? In fact, if the temperature impact on SR variation is compared with those of process and voltage impact, as shown in Table I. The result by a Monte-Carlo simulation (100 times) shows that given 1V, TT, 25°C as a typical circumstance, where each simulation change one variable (P, V, or T) a time to see the difference caused by each variation. When the impact of each variation is assumed as the ratios both at rising and falling edges, the impact of voltage and process variations is 3 times larger than that of the temperature. Therefore, the temperature detection could be ignored from I/O designs, when the area cost is one major consideration [17], [18].

• ESD protection [5]: From the measurement results of several previous works, the ESD strength of the stacked output stage with their current driving ability higher than 25 mA can be equalized to 2 kV for HBM (human body model) and 200 V for MM (machine model). In other words, if the required ESD protection is lower than these voltages, the large ESD circuit might not be needed. Fig. 3 (a) and (b) show the simplified circuit with ESD consideration through symmetrical discharging path and charging path, respectively. The sizes of the power transistors for ESD protection in the output stage can be estimated as addressed in [5].

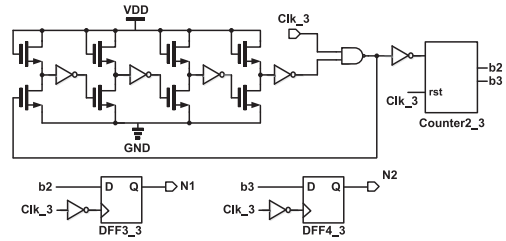

Fig. 4. Step 1 - N-Process Variation Detector [20].

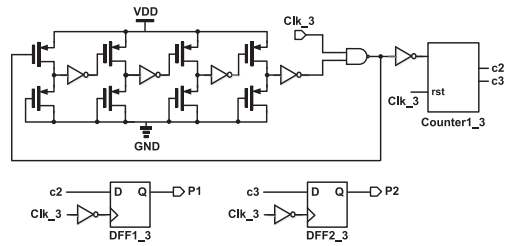

Fig. 5. Step 1 - P-Process Variation Detector [20].

B. Outward Path

This is the core of the entire I/O buffer, which is also called output buffer, consisting of N- and P-PVT Variation Detectors, Leakage Reduction Circuit, Digital Logic Circuit, and Output Stage. The design preferably starts from PVT Variation Detectors toward Output Stage.

1) Step 1 - Process Variation Detectors: Apart from many prior mixed-voltage buffer designs using delay-based approaches to find out only 3 (FF, TT, SS) corners, we encourage designers to separate PMOS and NMOS detections using dual process detectors. Referring to Fig. 4, the schematic of N-Process Variation Detector is shown, while the counter part, namely P-Process Variation Detector, is given in Fig. 5 [13], [14], [20]. They will generate 2-bit code, respectively, to Digital Control Circuit as shown in Fig. 2, denoting one of (SS, SF, TT, FS, FF) corners. That is, (N2, N1) in Fig. 4 are coupled to (V_{NF}, V_{NS}), and (P2, P1) in Fig. 5 to (V_{PF}, V_{PS}) in Fig. 2.

2) Step 2 - Voltage Variation Detector: The schematic of Voltage Variation Detector is shown in Fig. 6 [9], [14], [16]. It is a string of diode-connected PMOS transistors divided into three groups corresponding to three subranges from VDD to GND: VDD $\sim$ V_A, V_A $\sim$ V_B, V_B $\sim$ GND. Voltage level

TABLE II
FUNCTION TABLE OF VOLTAGE VARIATION DETECTOR

Voltage Level	V_1	V_2
+10% VDD	Logic 0	Logic 0
VDD	Logic 1	Logic 0
-10% VDD	Logic 1	Logic 1

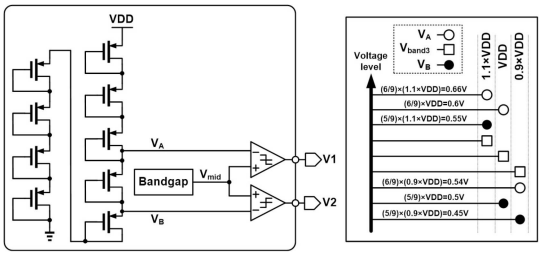

Fig. 6. Step 2 - Voltage Variation Detector [16].

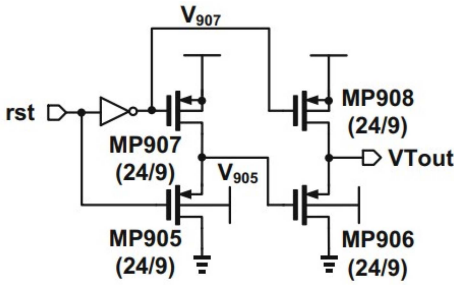

Fig. 7. Step 3 - Temperature Detector [8].

is also revealed in the right part of Fig. 6. Notably, V_A and V_B generate $\frac{6}{9}$ and $\frac{5}{9}$ VDD, respectively. It is easy to tell what the voltage variation is by such a configuration, since the variation of VDD between ±10% VDD can be directly sensed. Therefore, when it comes to ±10% VDD variations, the output voltage of the bandgap circuit will be fluctuated between +1.49% and −1.26%. Detailed function is summarized in Table II.

3) Step 3 - Temperature Detector: A very simple but reliable Temperature Detector is given in Fig. 7 [8], [11], [15]. This circuit takes advantage of two source followers to generate 2 × Vthp. The main difference from prior process or temperature variation detectors is that the bulks of MP905 and MP906 in this detector are coupled to VDD so that the body effect of each PMOS will affect the output, VTout. Therefore, by detecting the variations of Vthp posed on VTout, the temperature variation can be estimated [8].

4) Step 4 - Output Stage: Output stage in Fig. 2 is in charge of driving external loads such that it comprises large driving transistors, gate drive generators (Vg1, Vg2 generators), and Pre-driver [12]–[20]. Pre-driver is basically an encoder which receives digital codes to generate corresponding enable signals. Vg1 and Vg2 Generators are voltage level shifters elevating the enable signals to a level high enough to active the large PMOS driving transistors. The size calculation of these driving transistors is feasible provided that the slew rate and current requirements are given [16], [20].

5) Step 5 - Leakage Detection/Compensation: As addressed early, the buffers fabricated using advanced

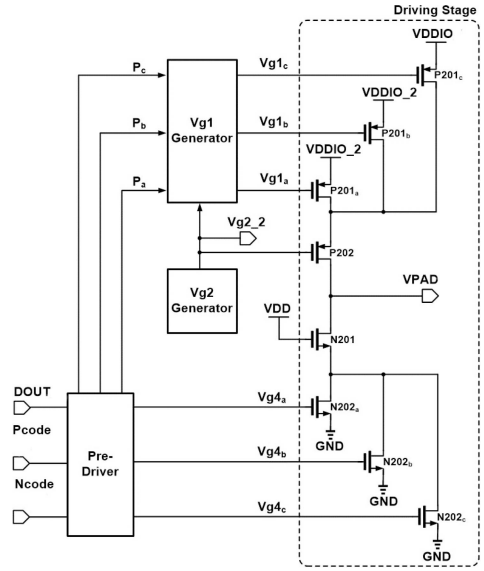

Fig. 8. Step 4 - Output stage with multiple current sources [16].

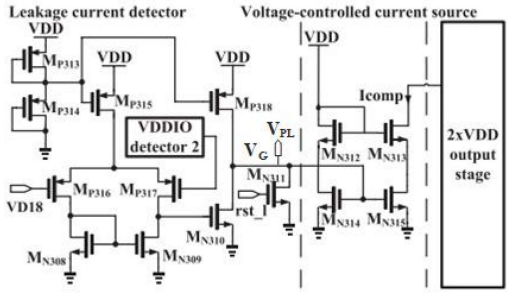

Fig. 9. Step 5 - Leakage Detection/Compensation [13].

CMOS technologies are bothered by leakage causing the loss of driving currents. Referring to Fig. 9, the leakage detection/compensation circuit comprises two subcircuits: a voltage-controlled current source, and a leakage current detector [12], [13], [15].

• Leakage current detector: Assuming that I_{leak} is the gate leakage current of P202 in Fig. 8, namely the always-on large PMOS, the voltage variation (V_{leak}) of P202 gate drive caused by the leakage current times the input resistance of P202. This voltage is called VD18 in Fig. 9, which is compared with a reference bias generated by VDDIO detector 2. (VDDIO detector 2 is a replica of Voltage Detector to estimate the voltage of the external signal, i.e., VDDIO).

• Voltage-controlled current source: I_{comp} is the compensation current coupled to P202 gate drive (in Fig. 8), namely coupled to I_{leak}. If VD18 is higher than the output of VDDIO detector 2, V_G is pulled up to raise the drain currents in the current mirror, i.e., MN312 and MN313. Notably, the drain current of MN313 is I_{comp}. If VD18 is lower, the operation is reversed. That is, a negative feedback loop from the P202 gate drive to the error amplifier (MP316, MP317) is used to regulate the current in the mirror composed of MN312-MN315. V_G is also coupled to V_{PL} in Fig. 2 for the leakage detection. If there is another leakage detection circuit to monitor the gate

V_{PS}	V_{PF}	V_{PL}	Pcode[2]	Pcode[1]	Pcode[0]	Process
0	0	0/1	0	0	1	Slow
0	1	0/1	0	1/0	1	Typical
1	1	0/1	1/0	1/0	1	Fast
V_{NS}	V_{NF}	V_{NL}	Ncode[2]	Ncode[1]	Ncode[0]	Process
0	0	0/1	0	0	1	Slow
0	1	0/1	0	1/0	1	Typical
1	1	0/1	1/0	1/0	1	Fast

Fig. 10. Step 6 - Encoder table for Digital Control Circuit [14].

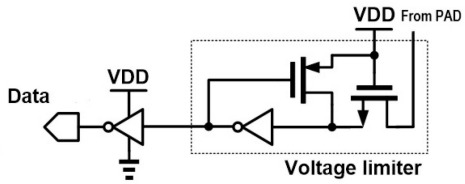

Fig. 11. Step 7 - Input Buffer (simple) [1], [2].

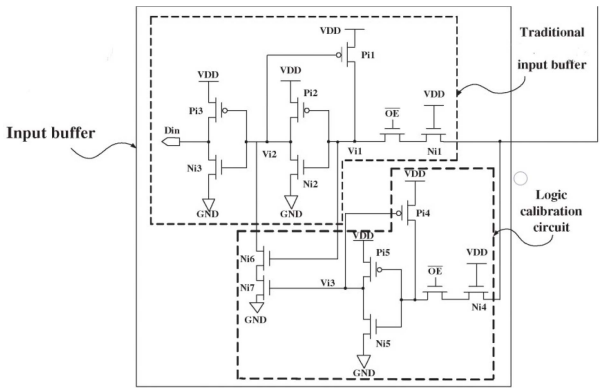

Fig. 12. Step 7 - Input Buffer (with calibration) [3].

drive of N201 in Fig. 8, namely another an always-on device, the V_G in this circuit is coupled to V_{NL} in Fig. 2.

6) Step 6 - Digital Control Circuit: Referring to Fig. 2, the last part in the outward path is Digital Control Circuit [12]–[20]. It is basically a big encoder logic circuit, receiving those codes from N- and P-Process Variation Detectors, Voltage Variation Detector, and, Temperature Detector, and then decide which pair(s) of driving transistors are turned on. The guideline is to turn on more current paths in "slow" corners, and vice versa. A typical truth table of Digital Control Circuit in Fig. 2 is shown in Fig. 10 [14].

C. Inward Path - Step 7

A typical input buffer is shown in Fig. 11, where one always-on NMOS device is used as a resistor to reject large input current so that the core circuit is protected. However, the simple input buffer might result in logic error problem if it is used in 3-voltage-mode I/O buffer or more voltage modes. With reference to the example in Fig. 12 realized using 3.3 V CMOS process, when $\overline{OE}$ is logic high to turn on the corresponding NMOS transistors, the input buffer is activated. Then, when VPAD = 0.9 or 1.2 V, Vi2 would be biased at 3.3 V, and Din is at 0 V to cause a logic error, since the switching voltage of the inverter, Pi2 and Ni2, is higher than 1.2 V. The logic error can be resolved by adding the logic calibration circuit in the bottom of Fig. 12. When VPAD = 1.2 or 0.9 V, Vi3 is biased at 3.3 V to turn on Ni7 such that Vi2 can be pulled to 0 V by Ni7 and the feedback loop composed of Pi1, Pi2, and Ni2. Then, the logic error can be corrected.

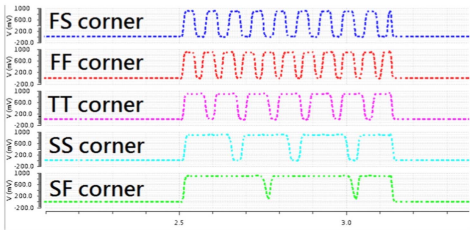

Fig. 13. An exmaple of sub-circuit timing (Process Variation detectors).

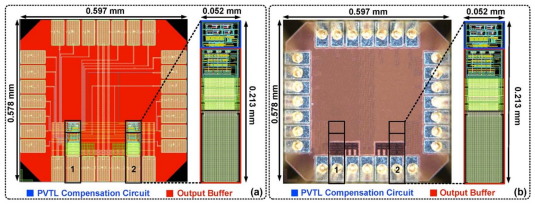

Fig. 14. Layout out and die photo of an I/O buffer.

III. I/O Buffer Design Validation

A buffer realized using a typical 28-nm CMOS process is used as an example to show what kind of validation is required to ensure the quality.

A. Simulation and Analysis

The major steps for the buffer design simulations include: pre-layout, all-PVT-corner post-layout, and Monte-Carlo simulations.

• *Pre-layout simulation for each sub-circuit:* It is to make sure all sub-circuits demonstrate functionality correctly in time domain. For instance, Fig. 13 is the timing simulations of Fig. 4 and 5. Apparently, the pulse count is different in various corners, which proves that the corners can be differentiated by counting the pulses in a given period. One issue frequently ignored by designers is to add the pad load during the simulations. According to our experience, 20 pF is the minimum to added at the output. For certain special cases, 60 pF might be needed for simulations to match the outcome given by real measurements or applications.

• *Post-layout all-PVT-corner simulation:* The lefthand side of Fig. 14 is the layout, where two buffers are in the same chip. The PVTL detection and the associated SR auto-adjustment in one buffer can be enabled externally and individually, namely "experimental group". By contrast, the other buffer is used as "control group", which has the same size but can not be enabled with PVTL detection. All parasitic resistance (R) and capacitance (C) must be extracted and annotated in post-layout simulations after the layout in done. The all-PVT-corner simulation of the buffer is demonstrated in Fig. 15. The corners to be simulated must least cover (SS, SF, TT, FS, FF)×(0.9 VDD, VDD, 1.1 VDD) ×(0°C, 25°C, 75°C). Apparently,

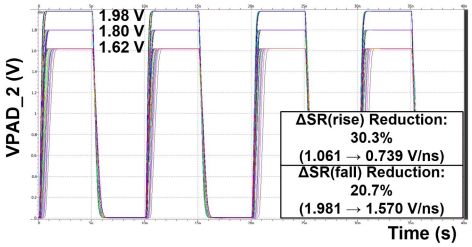

Fig. 15. Post-layout all-PVT-corner simulations.

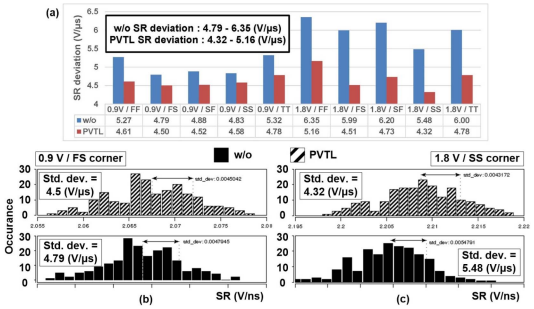

Fig. 16. Monte-Carlo simulations.

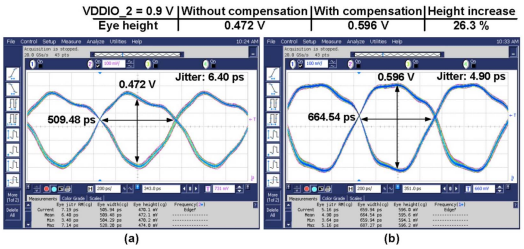

Fig. 17. Waveform of on-silicon measurement (eye diagram).

Fig. 15 not only shows that the functionality is good, also gives information regarding the maximal and minimal SRs of the digital signal's edges.

- *Monte-Carlo simulation [13], [15], [17], [20]:* To further justify the performance of the PVTL detection and SR auto-adjustment, Monte-Carlo analysis is carried out at least 200 times, preferably over 1000 times, to find out the mean and deviation at different corners. Their SR histogram should look like Fig. 16, where the comparison between with and without PVTL detection is apparently demonstrated. The SR variation is evidently narrower when the PVTL detection is enabled. This fact confirms the effectiveness of the PVTL auto-adjustment strategy.

B. On-Silicon Measurement

The final step is to measure the performance on silicon after the chip is fabricated. Three types of measurement instrument are needed at least: power supply, function generator, and oscilloscope. The I/O buffer chip is preferably mounted on PCB instead of bread board to eliminate possible ground noise. Since we already design 2 identical buffers on the same die (with and without PVTL detection), they must be measured simultaneously to attain fair comparison. Fig. 17 is the comparison of eye diagrams, while Fig. 18 is to find out the maximum data rate. To ensure the reliability and repeatability,

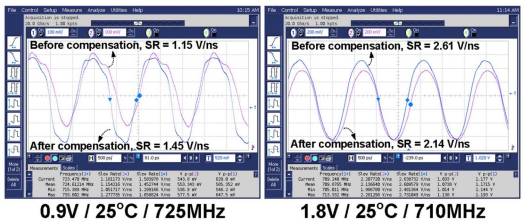

Fig. 18. Waveform of on-silicon measurement (maximum speed).

6 chips are encouraged to be measured 6 times individually such that we will have a conclusive result based on these observations.

IV. Conclusion and Remarks

All of the design, simulation, measurement steps in this tutorial have been verified repeatedly in my team over 10 years. The developed buffers are realized by CMOS nodes from 0.35 μm to 28 nm, speed from 100 MHz to over 800 MHz, and SR from 1.5 V/ns to 6.0 V/ns. The significance of mixed-voltage I/O buffers is that they are always needed because new chips still co-exist with prior legacy chips.

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