A Slew Rate Enhanced 2×VDD I/O Buffer With Precharge Timing Technique

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***Abstract*—This brief proposes a 2×VDD I/O buffer featured with precharge timing control to auto-adjust the slew rate. The stacked PMOS and NMOS transistors are widely used in the output stage of the 2×VDD I/O buffer to avoid the gate oxide overstress issue. However, it is hostile to the slew rate besides facing the hot carrier problem in the transient state. The precharging technique is proposed in this brief to improve the SR and avoid the hot carrier problem. The proposed design is carried out using a typical 40 nm CMOS process. The core area is 0.014 mm^2. The measured SR is improved to 2.81 V/ns. The measured eye height and eye width are 0.929 V and 0.904 ns, respectively, for VDDIO at 1.8 V.**

***Index Terms*—Mixed-voltage, I/O buffer, slew rate, eye height, and eye width.**

I. Introduction

VOLTAGE level translators are widely used to transfer data in multi-voltage systems, e.g., smart phone, portable devise, smart card reader, and telecommunication equipment [1], [2]. In order to reduce the system complexity, mixed-voltage I/O buffers are used as the interface among different voltage levels [3]–[13]. Stacked PMOS and NMOS transistors are employed in the output stage to avoid the overstress of gate driving due to the high voltage at VDDIO [3]–[6]. When the process comes to the nano-meter scale, the slew rate varies dramatically with the PVT (process, voltage, and temperature) corners. To improve the quality of transmission signals, the SR (slew rate) auto-adjustment techniques are used to reduce the SR variation in the mixed-voltage I/O buffers [7]–[10]. However, some of these works adjust the SR by only detecting 3 process corners (TT, FF, and SS) [8]–[10]. Besides, it takes more than 100 cycles to complete the process detection [9]. Recently, the 5 process corners (TT, FF, SS, FS, and SF) detection technique in one cycle is utilized in the mixed-voltage I/O buffers [11]–[13]. However, the problem of the hot carrier degradation caused by the floating voltage is ignored. The floating voltage results in the instant drain-source voltage over the tolerant voltage and might further reduce the usage life of the devices.

In order to resolve the hot carrier degradation caused by the floating voltage, this work proposes a precharging technique to give a stable voltage at the floating node. Besides, the timing control circuit is used to make sure the function correctness. Besides, the precharging circuit could also improve the SR. The simulation results show that the floating node can be biased to a determined voltage. The SR is measured to be 2.81 V/ns on silicon. The eye height and eye width are measured to be 0.929 V and 0.904 ns, respectively, for VDDIO at 1.8 V.

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II. 2×VDD I/O Buffer With Precharge Timing Control

Fig. 1 shows the block diagram of the proposed 2×VDD I/O buffer, which is composed of a PVT decider, Voltage/Timing controller, and Input/Output stage. The PVT detector detects the PVT corners including 5 process corners using the method in the prior work [13], [14]. It generates the signals, PS, PF, NS, and NF, which repreasent the slow and fast corners of PMOS and NMOS transistors, to Digital logic control circuit, respectively. The control signals, V_{gn}[3:1], and level-shifted control signals, V_{gp}[3:1], are then obtained. With the signal, VD, which is switched depending on the level of VDDIO, Voltage/Timing controller adjusts the appropriate voltage level and the timing of the control signals for the design. Pre-driver 1 and Pre-driver 2 provide gate drives for the Output Stage. The proposed precharging technique is used in the Output Stage, the Input Stage, and Voltage-Level Shifter (VLC) to eliminate the hot carrier degradation.

A. Output Stage

Fig. 2 reveals the schematic of the Output Stage. M_{p1a}, M_{p2}, M_{n2}, and M_{n1a} are stacked to avoid the gate oxide overstress for VDDIO at 2×VDD. M_{p1b}, M_{p1c}, M_{n1b}, and M_{n1c} are used to adjust the SR according to the signals, PS, PF, NS, and NF, as shown in Table I. When slow corners are detected, three current paths would be used. Only one current path is turned on for the fast corners. M_{p3} and M_{n3} carry out the precharging control to avoid the instant overstress. The non-overlap timing control is required for the gate drive signals, V_{gp1x} and V_{gn1x},

TABLE I
FUNCTION TABLE OF THE CONTROL OF THE SR COMPENSATION

Mode	Corners	PS NS	PF NF	D_1 D_2	V_{gp1a}	V_{gp1b}	V_{gp1c}	V_{gn1a}	V_{gn1b}	V_{gn1c}
Rx	-	-	-	-	1	1	1	0	0	0
Tx	Fast	1	1	0/1	1/0	1	1	1/0	0	0
Tx	Typical	0	1	0/1	1/0	1/0	1	1/0	1/0	0
Tx	Slow	0	0	0/1	1/0	1/0	1/0	1/0	1/0	1/0

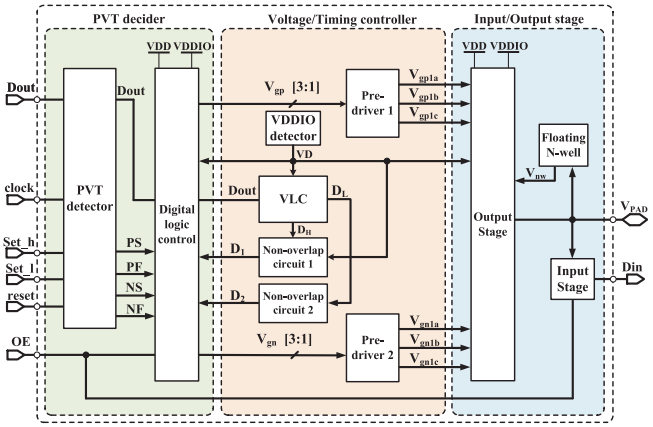

Fig. 1. Block diagram of the proposed 2×VDD I/O buffer with precharge timing control.

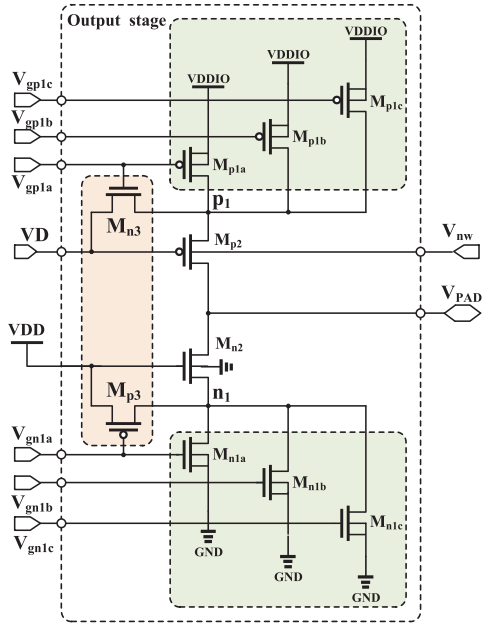

Fig. 2. Schematic of the proposed Output Stage with precharged devices.

as shown in Fig. 3. V_{gp1x} and V_{gn1x} denote for V_{gp1a}~V_{gp1c} and V_{gn1a}~V_{gn1c}, respectively.

When V_{PAD} transitions from 0 to 2×VDD for VDDIO at 1.8 V, V_{gn1x} changes from VDD to 0 first. It turns on M_{p3} such that n_1 is driven to VDD and V_{PAD} is at VDD-V_{th}. At the same time, V_{gp1x} is still at 2×VDD to turn on M_{n3} and keep p_1 at VDD through M_{n3}. Because n_1 and p_1 are both biased at a determined voltage, the instant drain-source overstress is avoided. Then, V_{gp1x} changes from 2×VDD to VDD to turn

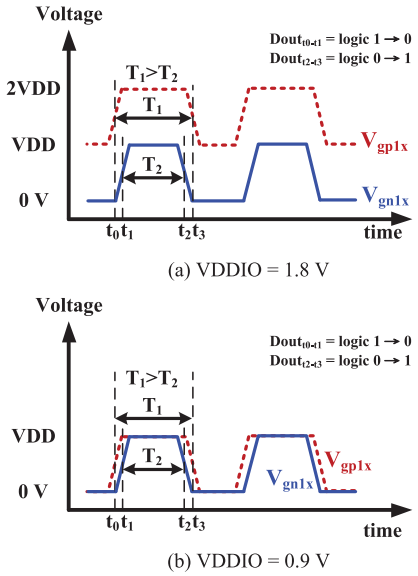

Fig. 3. Waveform of the gate drive voltages.

M_{n3} off and turn M_{p1x} on. V_{PAD} is, thus, pulled to 2×VDD. The entire process is summarized in following steps.

$$\text{Firstly, } V_{gn1x} = 0 \rightarrow M_{p3} \text{ on, and } M_{n1x} \text{ off}$$
$$\rightarrow n_1 = \text{VDD},\ V_{PAD} = \text{VDD} - V_{th} \text{ (Precharged)} \quad (1)$$
$$\text{Secondly, } V_{gp1x} = \text{VDD} \rightarrow M_{n3} \text{ off, and } M_{p1x} \text{ on}$$
$$\rightarrow p_1 = 2 \times \text{VDD},\ V_{PAD} = 2 \times \text{VDD} \quad (2)$$

With the additional current path through M_{p3}, the SR is improved as follows.

$$\text{SR}_{\text{rise}} = \frac{V}{T} = \frac{I}{C_L} \approx \frac{I_{p1x} + I_{p3}}{C_L}, \quad (3)$$

where I_{p1x} and I_{p3} stand for the current through M_{p1x} and M_{p3}, respectively. For the falling edge of output signal, V_{PAD} becomes from 2×VDD to 0. This process is expressed as follows.

$$\text{Firstly, } V_{gp1x} = 2 \times \text{VDD} \rightarrow M_{n3} \text{ on, and } M_{p1x} \text{ off}$$
$$\rightarrow p_1 = \text{VDD},\ V_{PAD} = \text{VDD} + V_{th} \text{ (Pre-discharged)} \quad (4)$$
$$\text{Secondly, } V_{gn1x} = \text{VDD} \rightarrow M_{p3} \text{ off, and } M_{n1x} \text{ on}$$
$$\rightarrow n_1 = 0,\ V_{PAD} = 0 \quad (5)$$

Similarly, the SR is improved by I_{n3}.

$$\text{SR}_{\text{fall}} = \frac{V}{T} = \frac{I}{C_L} \approx \frac{I_{n1x} + I_{n3}}{C_L} \quad (6)$$

I_{n1x} and I_{n3} indicate the current through M_{n1x} and M_{n3}, respectively.

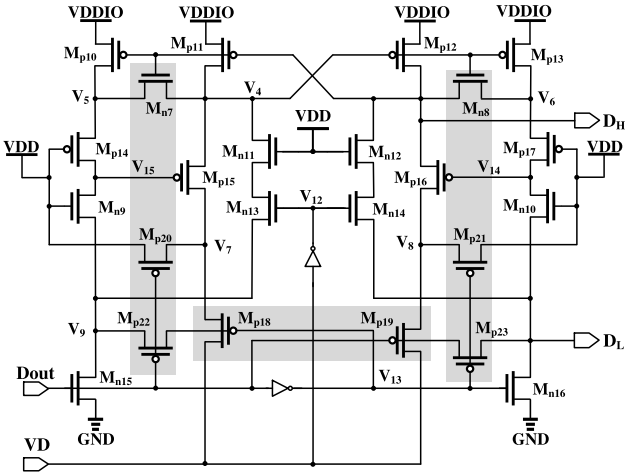

Fig. 4. Schematic of Voltage Level Converter (VLC).

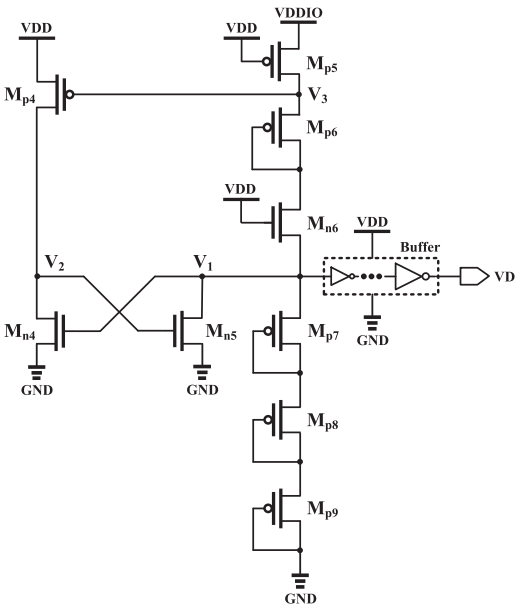

Fig. 5. Schematic of the VDDIO Detector.

B. Voltage/Timing Controller

1) Voltage Level Converter (VLC): The schematic of VLC is shown in Fig. 4. When VDDIO is at 2×VDD, VD is biased at VDD. Dout controls $M_{p18\sim19}$ and $M_{n15\sim16}$ such that D_H is pulled high by the cross-coupled PMOS transistors and possesses the voltage level from VDD to 2×VDD. When VDDIO is at VDD, VD becomes 0 V. Dout controls $M_{n11\sim16}$ to determine the logic value of D_H, which is from 0 V to VDD by the cross-coupled $M_{p11\sim12}$. Notably, $M_{n7\sim8}$ and $M_{p18\sim23}$ provide the precharge path to drive $V_{5\sim9}$ and D_L to a determined voltage such that the proposed design avoids the instant overstress problem and eliminates the leakage current through $M_{p15\sim16}$.

2) VDDIO Detector: VDDIO Detector is shown in Fig. 5. When VDDIO is at 2×VDD, M_{p5} is turned on and the voltage of V_3 is high enough to turn M_{p4} off. Thus, V_1 is equal to the summation of the threshold voltages of $M_{p7\sim9}$ and V_2 is pulled to 0. Thus, VD of VDD is obtained. Notably, M_{p4} should be realized by the thick oxide device to avoid the overdive hazard

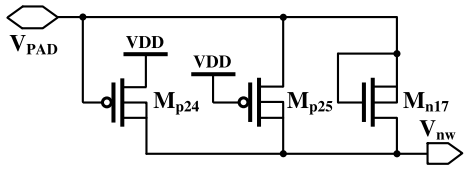

Fig. 6. Schematic of Floating N-well Circuit.

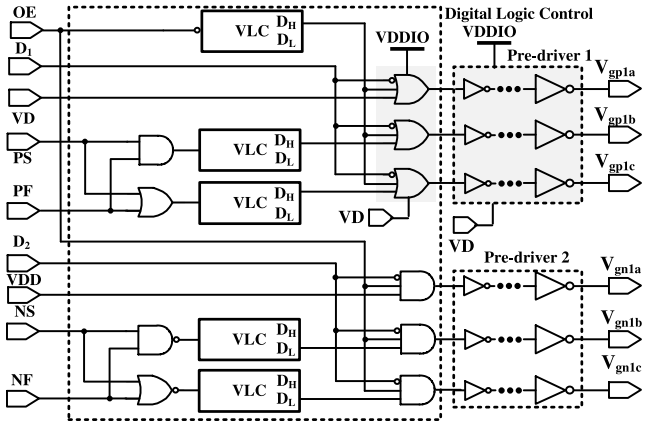

Fig. 7. Schematic of Digital Logic Control and Pre-drivers.

when VDDIO is at 2×VDD. When VDDIO is at VDD, V_3 is equal to VDD-V_{th}, which turns M_{p4} on. It pulls V_2 and V_1 to VDD and 0 V, respectively. Thus, VD of 0 V is generated. The cross-coupled transistors, M_{n4} and M_{n5}, improve the function correctness in all-corner simulation. The Buffer in Fig. 5 provides the required driving current.

3) Non-Overlap Circuit: In order to generate the required non-overlap signals as shown in Fig. 3, two Non-overlap circuits are used. Non-overlap circuit 1 operates at voltage between VDD and VDDIO. Non-overlap circuit 2 is from 0 V to VDD.

C. Floating N-Well Circuit

Referring to Fig. 6 shows the schematic of Floating N-well Circuit. When V_{PAD} is at 2×VDD, M_{p25} is turned on such that V_{nw} is 2×VDD. Thus, the parasitic diode of M_{p2} in Output Stage is turned off such that the leakage path could be removed. Notably, $V_{th,n17}$ is chosen smaller than the turn-on voltage of the parasitic diodes of M_{p24}, M_{p25} and M_{p2} to avoid the leakage current path induced when V_{PAD} is at VDD.

D. Digital Logic Control and Pre-Driver

Fig. 7 shows the schematic of Digital Logic Control Circuit, Pre-driver 1 and Pre-driver 2. Digital Logic Control Circuit converts the signals, PS, PF, NS, NF, D_H, and D_L to V_{gp1x} and V_{gn1x}, as shown in Table I. The inputs, VD and VDD, are used to generate the required timing for V_{gp1x} and V_{gn1x}.

E. Input Stage

Fig. 8 is the schematic of Input Stage. Unlike the traditional design, Inverting Schmitt Trigger is used to improve the immunity to the noise. Besides, M_{n19} provides the precharge path to drive V_{10} at VDD when VDDIO is 2×VDD. It

TABLE II
PERFORMANCE COMPARISON OF OUTPUT BUFFER

	[9]	[10]	[8]	[12]	[13]	This work
Year	2003	2010	2013	2017	2019	2019
Publication	JSSC	TCAS-II	TCAS-I	TCAS-II	TCAS-II	TCAS-II
Process (nm)	180	180	90	40	40	40
VDD (V)	3.3	1.8	1.2	0.9	0.9	0.9
VDDIO (V)	3.3	1.8	2.5	0.9/1.8	0.9/1.8	0.9/1.8
Process Corners	3	3	3	5	5	5
Lock Cycles	>100	1	1	1	1	1
Max. Date Rate (MHz)	25	1000	125	500/250	700/650	400/500
Measured Max. SR (V/ns)	2.86	2.25	2.14	1.54	1.698	2.81
Measured Eye Height (V)	N/A	N/A	N/A	0.378/0.378	0.538/0.710	0.915/0.929
Measured Eye Width (ns)	N/A	N/A	N/A	0.760/0.458	0.610/0.686	1.16/0.904
Core area (mm^2)	0.162	0.009	N/A	0.01	0.011	0.014
Mixed voltage mode	No	No	Yes	Yes	Yes	Yes
FOM†	N/A	N/A	N/A	1.44/0.43	2.09/2.88	3.03/3.00

†$\text{FOM} = \frac{\text{Data Rate} \times \text{Eye Height} \times \text{Eye Width}}{\text{Core Area}}$.

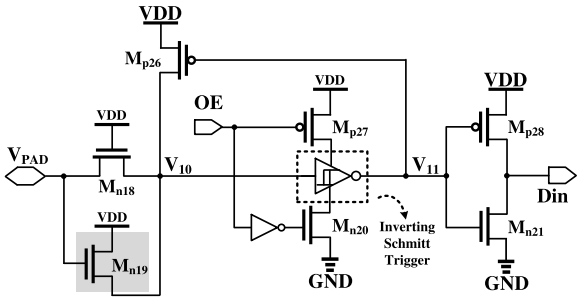

Fig. 8. Schematic of Input Stage.

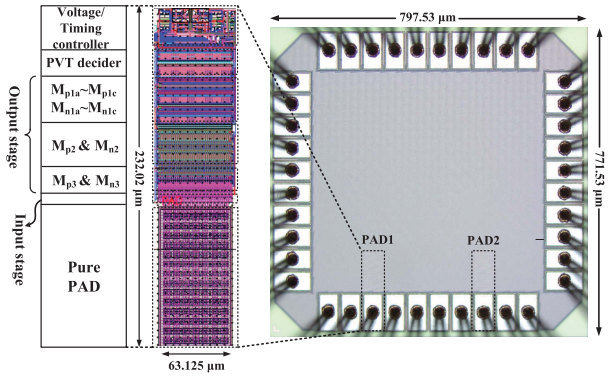

Fig. 9. (a) Layout and (b) diephoto of the 2xVDD I/O Buffer.

avoids the hot carrier degradation at M_{n18}. A leakage current path through M_{p26} and M_{n18} could be avoided by giving a specific logic 1 at V11 when OE is at logic 1.

III. IMPLEMENTATION AND MEASUREMENT

The proposed design is carried out using TSMC 40 nm CMOS process. Fig. 9 shows the layout and diephoto. The core area of a single I/O buffer is $232.02 \times 63.125\ \mu m^2$, The whole chip size is $797.53 \times 771.53\ \mu m^2$. The output stage is drawn with the finger layout style and dual layers of metal (M3 and M4) are used simultaneously for increasing the current density. Fig. 10 shows the simulated waveforms of p_1, n_1 and V_{PAD} in different PVT corners. The signals, p_1 and n_1 are pre-discharged and precharged, respectively, to a determined

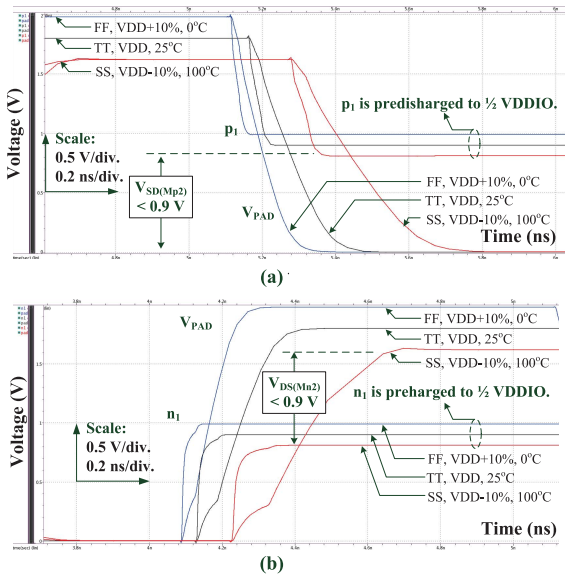

Fig. 10. Simulated waveforms of (a) p_1 and (b) n_1 in different PVT corners.

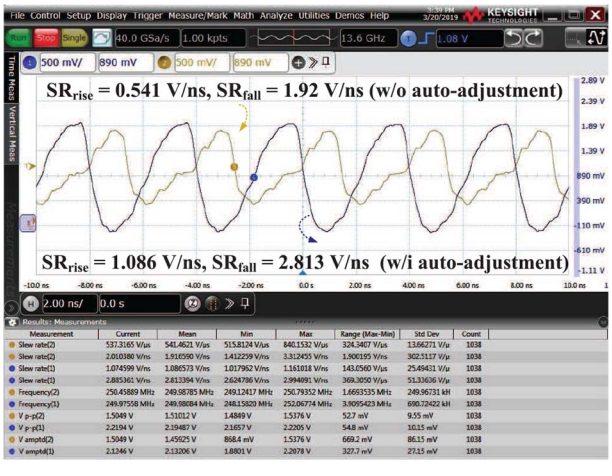

Fig. 11. Measured waveforms of output signal, V_{PAD}, for VDDIO at 1.8 V with the loads of 50 Ω.

voltage to avoid the hot carrier degradation. Fig. 11 reveals the measured V_{PAD} for VDDIO at 1.8 V. After the detection and self-adjustment, the SR is 1.086 and 2.813 V/ns for the

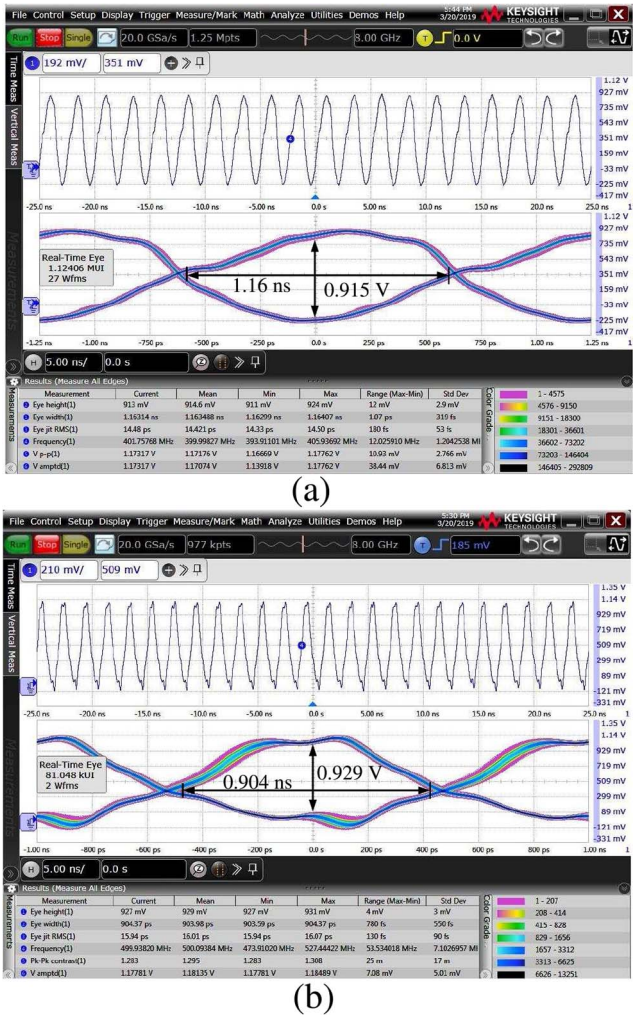

Fig. 12. Measured eye diagram of V_{PAD} for (a) VDDIO at 0.9 V and (b) VDDIO at 1.8 V with the loads of 50 Ω.

rising edge and falling edge, respectively. The SR is improved by 46.5% for the worst case of falling edge. Fig. 12 shows the measured eye diagram at 400 and 500 MHz for VDDIO at 0.9 V and 1.8 V, respectively. The eye height and eye width are 0.915 V and 1.16 ns, respectively, for VDDIO at 0.9 V. For VDDIO at 1.8 V, the eye height and width are 0.929 V and 0.904 ns, respectively. Table II shows the comparison with several prior works. By considering FOM including the data rate, eye height, eye width, and core area, the proposed design demonstrates the best performance.

IV. Conclusion

This investigation proposes a 2×VDD I/O buffer with precharge timing technique. The precharge technique drives the nodes to determined voltages in Output Stage, the VLC, and the Input Stage to avoid the hot carrier degradation. Beside, it provides an additional charging path to improve the SR. The measured results verify that the circuit could improve the overall SR and eye diagram performance.

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References

[1] MAX13000E. *Ultra-Low-Voltage Level Translators*. Accessed: May 2011. [Online]. Available: https://www.maximintegrated.com/en/products/interface/level-translators/MAX13000E.html

[2] *TXS0101, 1-Bit Bidirectional Level-Shifting,Voltage-Level Translator With Auto-DirectionSensing for Open-Drain and Push-Pull Applications*. Accessed: May 2008. [Online]. Available: http://www.ti.com/lit/ds/symlink/txs0101.pdf

[3] D.-Y. Chen, "Design of a mixed 3.3 V and 5 V PCI I/O buffer," in *Proc. Int. Conf. ASIC*, Oct. 1996, pp. 336–339.

[4] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of mixed-voltage I/O buffer by using NMOS-blocking technique," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2324–2333, Oct. 2006.

[5] A.-J. Annema, G. J. G. M. Geelen, and P. C. de Jong, "5.5-V I/O in a 2.5-V 0.25-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 528–538, Mar. 2001.

[6] B. Serneels, T. Piessens, M. Steyaert, and W. Dehaene, "A high-voltage output driver in a 2.5-V 0.25-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 576–583, Mar. 2005.

[7] T.-J. Lee, W. Lin, and C.-C. Wang, "Slew rate improved 2×VDD output buffer using leakage and delay compensation," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Jun. 2014, pp. 1–2.

[8] M.-D. Ker and P.-Y. Chiu, "Design of 2×VDD-tolerant I/O buffer with PVT compensation realized by only 1×VDD thin-oxide devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 10, pp. 2549–2560, Oct. 2013.

[9] S.-K. Shin, S.-M. Jung, J.-H. Seo, M.-L. Ko, and J.-W. Kim, "A slew-rate controlled output driver using PLL as compensation circuit," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1227–1233, Jul. 2003.

[10] Y.-H. Kwak, I.-H. Jung, and C.-W. Kim, "A Gb/s+ slew-rate/impedance-controlled output driver with single-cycle compensation time," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 2, pp. 120–125, Feb. 2010.

[11] T.-J. Lee, T.-Y. Tsai, W. Lin, U.-F. Chio, and C.-C. Wang, "A dynamic leakage and slew rate compensation circuit for 40-nm CMOS mixed-voltage output buffer," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 11, pp. 3166–3174, Nov. 2017.

[12] C.-C. Wang, Z.-Y. Hou, and K.-W. Ruan, "2 × VDD 40-nm CMOS output buffer with slew rate self-adjustment using leakage compensation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 7, pp. 812–816, Jul. 2017.

[13] T.-J. Lee, T.-Y. Tsai, W. Lin, U.-F. Chio, and C.-C. Wang, "A slew rate and leakage compensated 2×VDD I/O buffer using deterministic P/N-PVT variation detection method," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 1, pp. 116–120, Jan. 2019.

[14] C.-C. Wang, Z.-Y. Hou, and S.-W. Huang, "40-nm 2×VDD digital output buffer design with DDR4-compliant slew rate," in *Proc. IEEE Asia–Pacific Conf. Circuits Syst. (APCCAS)*, 2018, pp. 279–282.