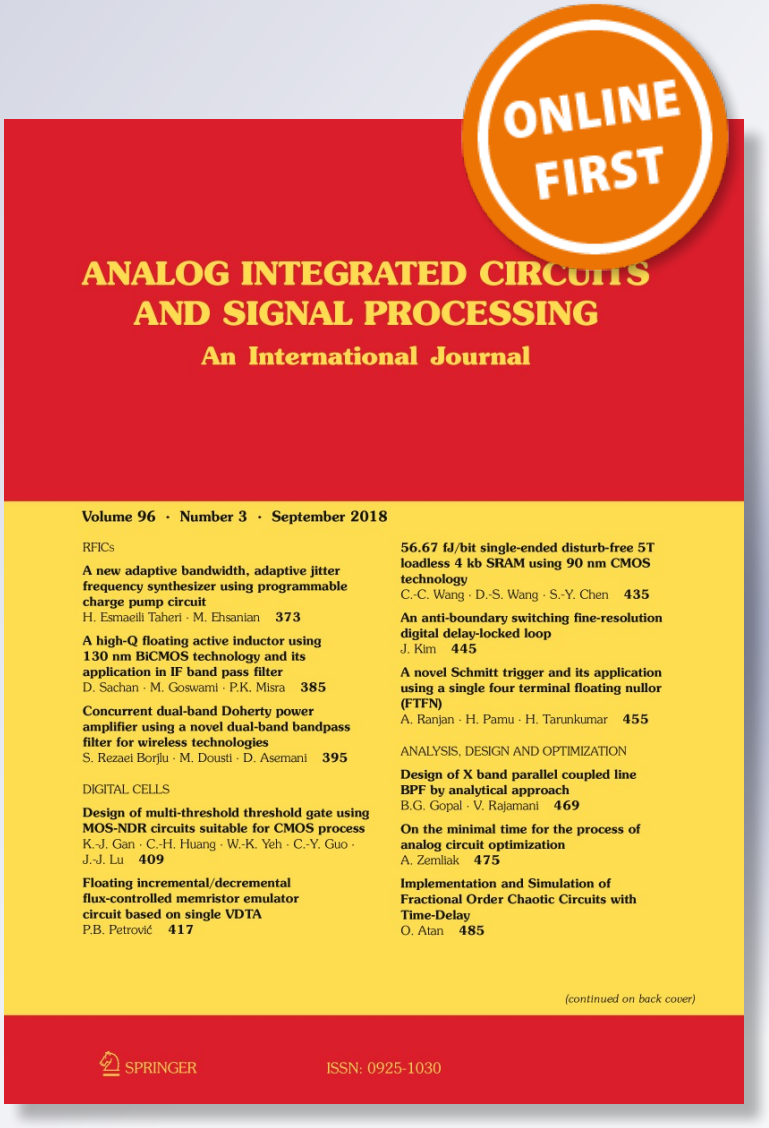
A 90-nm CMOS 800 MHz 2$$\times$$ × VDD output buffer with leakage detection and output current self-adjustment

Chua-Chin Wang, Tsung-Yi Tsai & Wei Lin

Analog Integrated Circuits and Signal Processing
An International Journal

ISSN 0925-1030

Analog Integr Circ Sig Process
DOI 10.1007/s10470-018-1285-3



Springer

Analog Integrated Circuits and Signal Processing
https://doi.org/10.1007/s10470-018-1285-3

A 90-nm CMOS 800 MHz 2×VDD output buffer with leakage detection and output current self-adjustment

Chua-Chin Wang[1] · Tsung-Yi Tsai[1] · Wei Lin[1]

Received: 27 January 2018 / Revised: 10 July 2018 / Accepted: 3 August 2018

Abstract
This work presents a 800 MHz 2×VDD output buffer with PVTL (Process, Voltage, Temperature, Leakage) detection techniques to reduce slew rate (SR) variation. The threshold voltage (Vth) of MOS transistors varying with PVT is detected such that Output buffer will turn on different current paths correspondingly to decrease or increase the compensation current. Moreover, the slew rate is adjusted by Delay buffer and the leakage current sensor which compensates the dynamic and static currents, respectively. Most important of all, a deterministic sizing optimization method for the output transistors is reported and analyzed. The proposed design realized using a typical 90 nm CMOS process shows that the maximum data rate is 450/800 MHz given supply voltage 1.0/1.8 V with PCB and SMA connectors. The SR variation is reduced over 43% after the compensation of the leakage detection. The core area of the prototype is 0.056 × 0.439 mm^2, and the power consumption is 68.9/98.5 (μW/MHz) at 450/800 MHz, respectively.

Keywords PVTL variation · I/O buffer · Threshold voltage detection · Floating N-well circuit · Gate-oxide reliability · Slew rate compensation · Mixed-voltage tolerant

1 Introduction

Slew rate (SR) performance and data rate are required in many I/O design buffers, e.g., ATA, PCI, PCI-express, UDMA [1], etc. However, conventional I/O buffers, e.g. [2], were focused on multi-voltage tolerance with gate-oxide overstress problems rather than SR behaviors under several environmental variations, namely, process, voltage, temperature (PVT), and leakage. Mixed-voltage I/O buffers are always bothered by the mentioned variations, which have been proved to severely degrade the IC performance. It has also been demonstrated that the performance of IC is more reliable with PVT compensations [3]. However, as nanometer technology keeps developing, the thickness of gate oxide becomes thinner which in turn causes a significant leakage current in nano-scale output buffer design.

Analog output buffers based on push–pull and rail-to-rail topology have also been reported in [4] and [5]. However, their data rate and SR are not adequate for high speed digital output buffers. Mixed-signal output buffer demonstrated in [6] utilized stacked MOS transistors, floating N-well circuit, and gate-tracking circuit to avoid over-stress problem and the leakage current from drain to bulk, respectively, where there is no compensation mechanism to cope with different PVT variation hazards. On the other hand, they still cannot the find out the variations at FS and SF corners. A PT (process, temperature) sensor and a PV (process, voltage) sensor were proposed in [7] and [8] to compensate variation. However, both sensors don't achieve complete PVT compensations. Another I/O buffer with a PVT variation detector, an encoder, and a 2×VDD buffer was reported in [9]. However, it can only detect three corners, namely TT, FF, SS. An I/O buffer composed of analog PVT sensors, and a stacking-transistor output buffer was proposed to reduce the PVT variation impact [10, 11]. However, not only is its data rate not good enough to meet certain interface requirement, it also lacks of a

✉ Chua-Chin Wang
ccwang@ee.nsysu.edu.tw

Tsung-Yi Tsai
zack@vlsi.ee.nsysu.edu.tw

Wei Lin
andrew@vlsi.ee.nsysu.edu.tw

[1] Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan

Published online: 13 August 2018

leakage current sensor for those I/O buffers fabricated using advanced CMOS processes. Referring to [12], although leakage compensation has been added in this I/O design, the speed of data rate still has a lot room to be improved.

Therefore, this investigation demonstrates an I/O buffer which can transmit/receive 2×VDD voltage with PVTL compensation. Furthermore, the PVTL compensation may be a useful technique to meet the recent high-speed serial interface standards such as [13] and [14].

2 2×VDD output buffer circuit design

Figure 1 shows the block diagram of the proposed output buffer with PVTL compensation, consisting of PVT sensor, PVT decider, Leakage Current sensor, and Output buffer. PVT sensor monitors the different variations to generate corresponding signals. PVT decider quantifies the generated signals to deliver corresponding compensation codes. Output buffer receives the compensation codes to adjust slew rate by turning on or off corresponding current paths, or to maintain the stability of gate bias voltage. Notably, the clock is an external signal with 100 MHz pulse. The details of all the blocks mentioned in the above will be disclosed in the following text.

2.1 PVT sensor

PVT sensor consists of four major blocks [15], i.e., PMOS Process sensor, NMOS Process sensor, Voltage and Temperature sensor (VT sensor), and Leakage Current sensor. Process sensors and VT sensor have a similar architecture with minor differences.

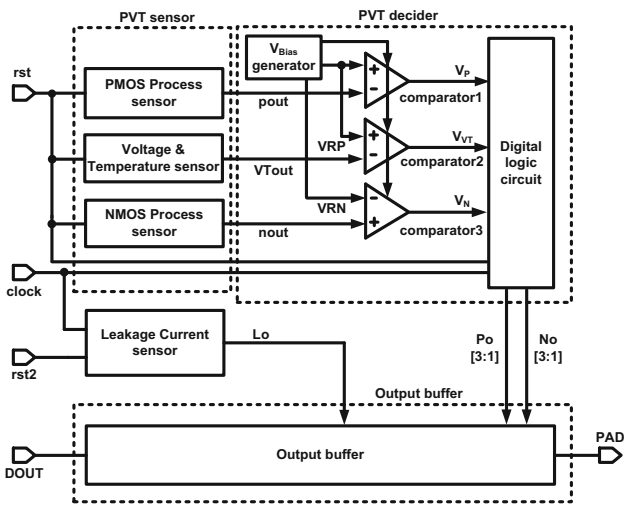


Fig. 1 Block diagram of the proposed 2×VDD output buffer

2.1.1 PMOS and NMOS process sensor

Figure 2(a), (b) shows the schematic of PMOS and NMOS Process sensor, consisting of 4 PMOS or NMOS transistors, MP901–MP904 or MN901–MN904, respectively. The detailed functionality of PMOS Process sensor is given as follows.

1. When the reset (rst) is logic 1 (= 1.0 V), it turns on MP903, MP904, and shuts down MP901. Therefore, it pulls V_{901} up to VDD to cause the voltage dropping across V_{901} and the gate of MP901 (rst) smaller than Vthp, and then it turns off MP902. Simultaneously, pout is then charged to VDD.
2. When the reset (rst) is pulled down to logic 0 (= 0 V), it turns off MP903, MP904, and turns on MP901. V_{901} is then discharged to Vthp, namely the threshold voltage of MP901.
3. Then, after a repeated cycle of step (1) and (2), pout will be discharged to 2×Vthp, which means to amplify PMOS process variation.
4. Finally, the output voltage, pout, is then coupled to the following PVT decider to determine which PMOS process corner is.

The steps of NMOS Process sensor is similar to those of PMOS counterpart. The extraction of threshold voltage (Vthn) will differentiate NMOS process corners with distinct voltages.

2.1.2 Voltage and temperature sensor

The schematic of Voltage and Temperature sensor is shown in Fig. 2(c). This circuit is similar to Process sensors, which uses two source followers to generate 2×Vthp. The main difference is that the bulks of MP905 and MP906 in VT sensor are coupled to VDD so that the body effect of each PMOS will affect the output, VTout. Therefore, by detecting the variations of Vthp, the temperature and voltage variations also can be detected simultaneously.

2.2 PVT decider

Referring to Fig. 1 again, the functionality of PVT decider is to receive the outputs of the sensors and generate 2 digital codes, namely Po[3:1] and No[3:1], which indirectly adjust the compensation of Output buffer. PVT decider is composed of 3 comparators, a V_{Bias} generator, and a Digital logic circuit. Notably, Digital logic circuit comprises a 6-bit counter, D flip-flops (DFFs), and an Encoder. When the output voltage of each sensor is over the reference voltage individually, the comparators generate V_P, V_{VT}, and V_N, respectively, to stop the counting of corresponding DFFs (registers). Encoder will generate

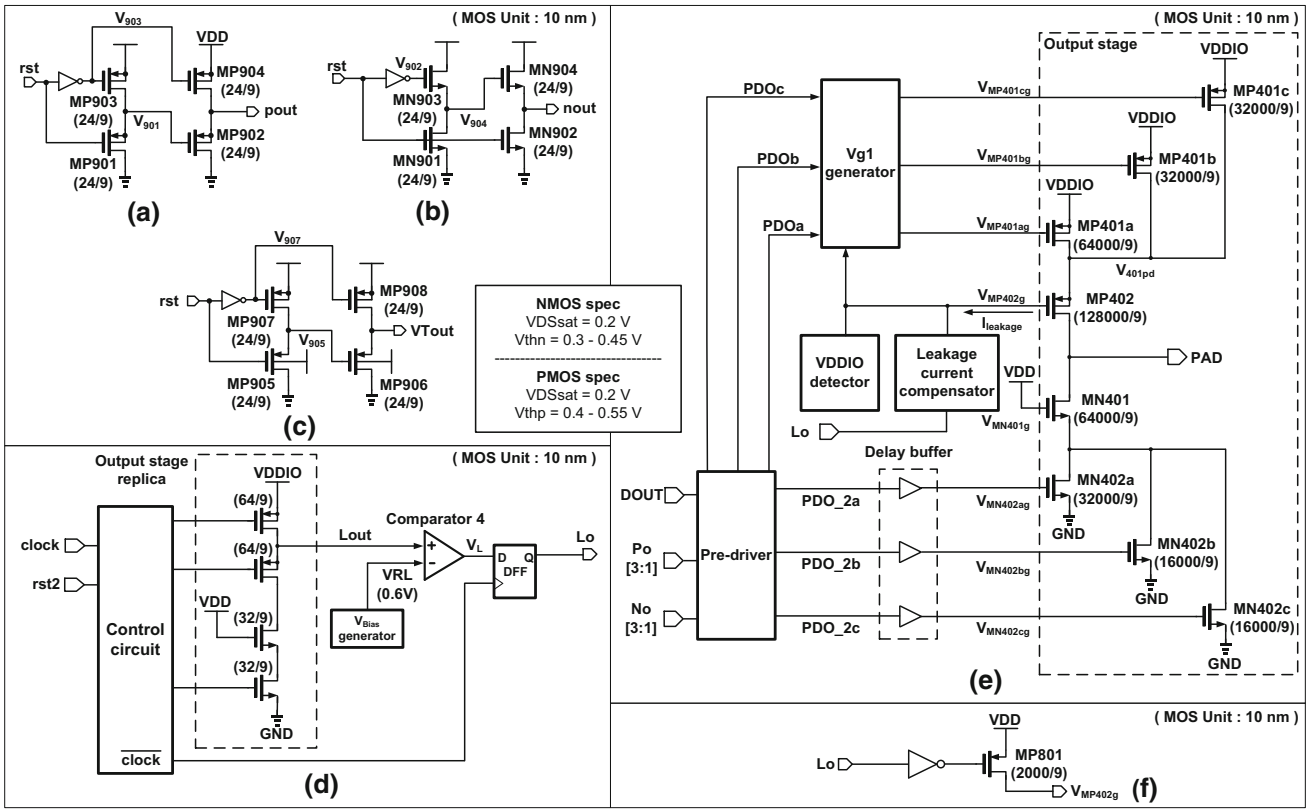


Fig. 2 **a** PMOS Process sensor, **b** NMOS Process sensor, **c** voltage and temperature sensor, **d** leakage current sensor, **e** output buffer, and **f** leakage current compensator. (Note: the unit of width or length is 10 nm)

Po[3:1] and No[3:1] based on the count of DFFs, where the outputs code will switch on or off the corresponding compensation current paths in Output buffer.

2.3 Leakage compensation technique and output buffer

Referring to Fig. 2(d), Leakage Current sensor is used to generate Lo. It consists of a Control circuit, an Output stage replica and a D-type flip-flop (DFF). Regardless of VDDIO (either 1.0 V or 1.8 V), the characteristics of Output stage replica and Output stage are identical, where the transistor size of the former is scaled down to $\frac{1}{1000}$ of the corresponding transistor in the latter. Notably, there are also a Vg1 generator, and a VDDIO detector in Control circuit just like those in Output Buffer. Therefore, by monitoring the voltage variation of replica circuit, the over-voltage hazard will be detected by the comparator. Lo is pulled up to logic 1 when an over-voltage problem occurs, and vice versa. Output buffer in Fig. 2(e) consists of Delay buffers, a Vg1 generator, an Output stage, a VDDIO detector, a Leakage current compensator, and a Pre-driver. Notably, the Pre-driver receives input signals, DOUT, Po[3:1], No[3:1], and then generates 6 control signals, PDOa–c, and PDO_2a–c. PDOa–c are coupled to Vg1 generator to shift up voltage levels such that the gate drives, $V_{MP401ag}$–$V_{MP401cg}$, are translated to appropriate voltage drives for MP401a–MP401c, respectively. PDO_2a–c are coupled to Delay buffer to delay the turn-on of the corresponding different current sink paths. Leakage current compensator is activated to stabilize the bias voltage, V_{MP402g}, when Lo is logic 1. More details will be disclosed in the next subsection. VDDIO detector will generate corresponding gate voltage to drive bias voltage V_{MP402g} based on the detected VDDIO voltage level. Since Vg1 generator, Pre-driver, VDDIO detector, and Output stage can be realized using prior circuits [6, 7]. ESD hazard is also considered by using stacked MOS in Output buffer. According to the prior research, i.e. Section II-F in [16], the ESD strength of the stacked output stage can resist 2 kV for HBM (human body model) and 200 V for MM (machine model), if the current driving capability is higher than 25 mA. Since the widths of PMOS and NMOS in our output stage are larger than those in [16], (1280 μm vs. 720 μm, 640 μm vs. 180 μm), our design will at least provide the same ESD protection capability, if not higher. Three featured designs of this investigation are highlight as follows.

2.3.1 Leakage compensation mechanism

Before introducing Leakage Current sensor design, what kind of leakage currents we are dealing with, and how we manage to carry out the compensation should be addressed. According to [17], the gate leakage current I_{GC}, which is the combination of I_{GCD} and I_{GCS}, is expressed as follows,

$$I_{GC} = \frac{J_{G0} \cdot W \cdot L \cdot (1 - e^{B^* \cdot K \cdot L})}{B^* \cdot K \cdot L}, \quad (1)$$

where J_{G0} is the current density of gate leakage, W and L are the width and length of MOS transistor, respectively, K is the parameter correlated to threshold voltage, and B^* is the parameter with thickness of oxide and the voltage between gate and source. Notably, I_{GC} is then proportional

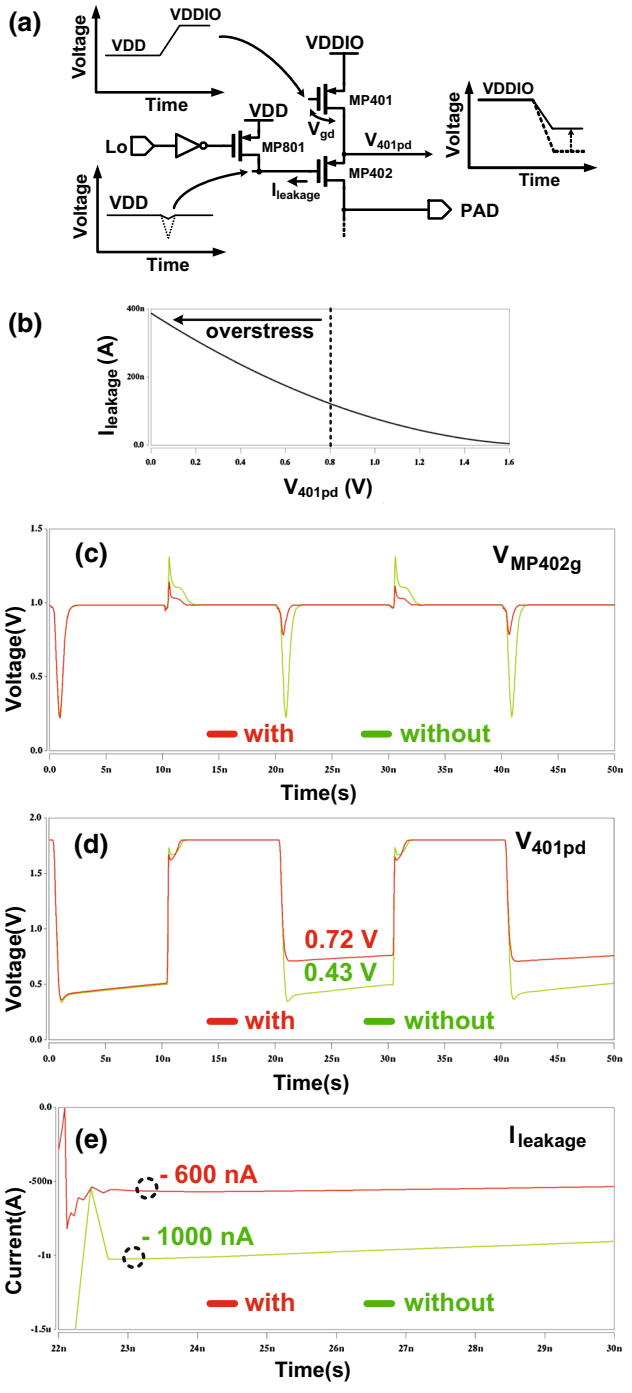


Fig. 3 **a** Timing diagram of output stage's PMOSs with leakage compensation, **b** the gate leakage of MP401 vs. V_{401pd}, **c** simulation of V_{MP402g}, **d** simulation of V_{401pd}, and **e** simulation of $I_{leakage}$

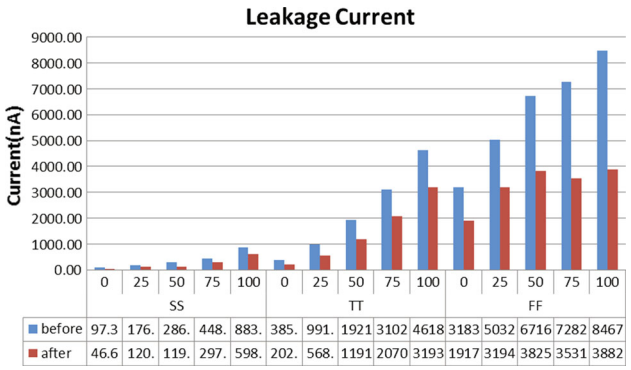


Fig. 4 Statistics of gate leakage current at different PVT corners

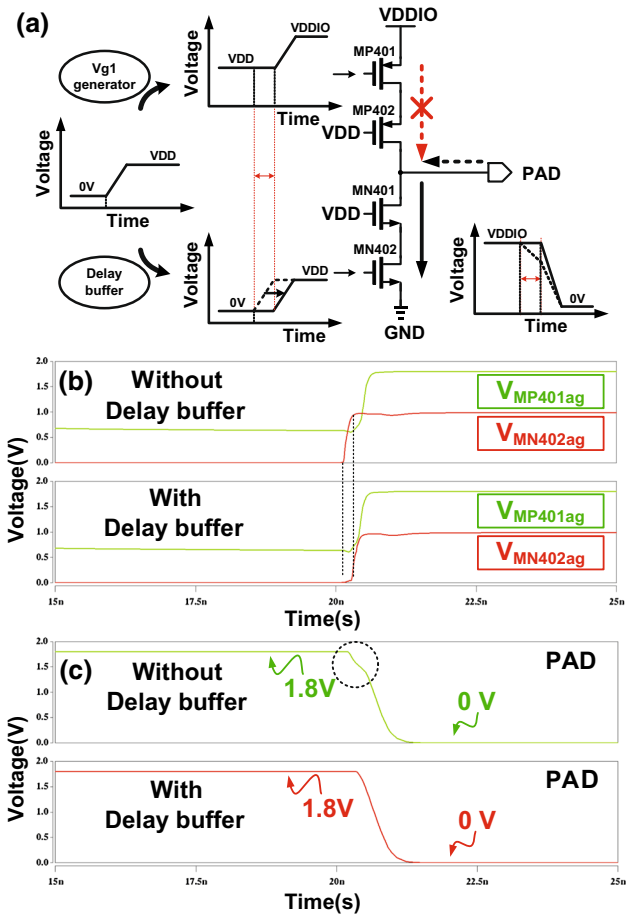


Fig. 5 **a** SR enhancement after using delay buffer, **b** gate voltage simulations of $V_{MP401ag}$ and $V_{MN402ag}$, and **c** simulation of PAD

to transistor's width. If the width of MOS size is enlarged to achieve better SR performance, the price to pay is poor efficiency and redundant power loss.

As depicted in Fig. 2(f), Leakage current compensator is simply composed of a PMOS transistor and an inverter. The width of MP801 is 20 um in this work, which is enough to serve as a stabilizer maintaining the voltage level of V_{MP402g}, but will not become a current supplier. Notably, when VDDIO = 1.8 V and Lo is logic 1, V_{MP402g}

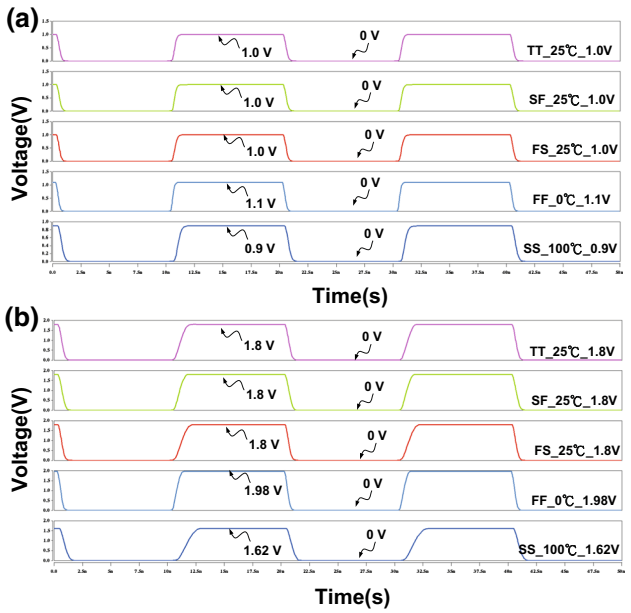


Fig. 6 Worst-case transient response among all PVT corners when VDDIO = **a** 1.0 V or **b** 1.8 V

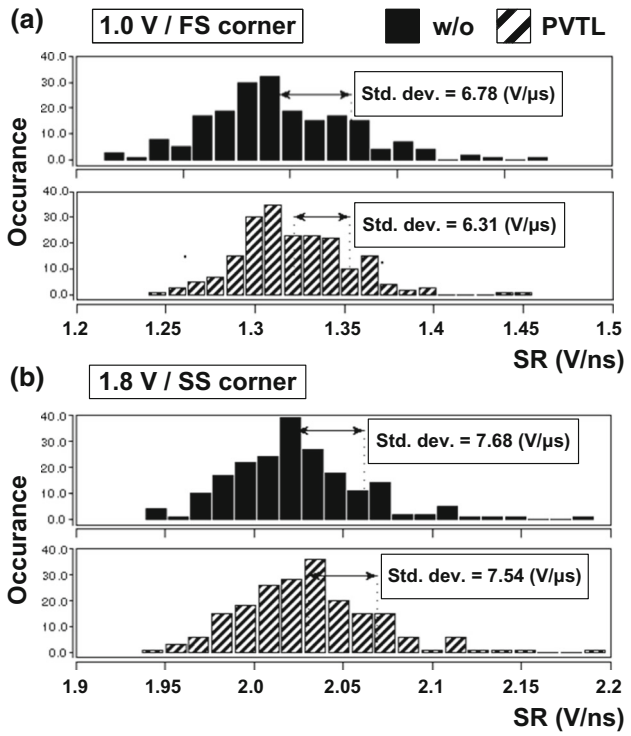


Fig. 7 Worst-case Monte Carlo simulation results of SR deviations when VDDIO = **a** 1.0 V or **b** 1.8 V

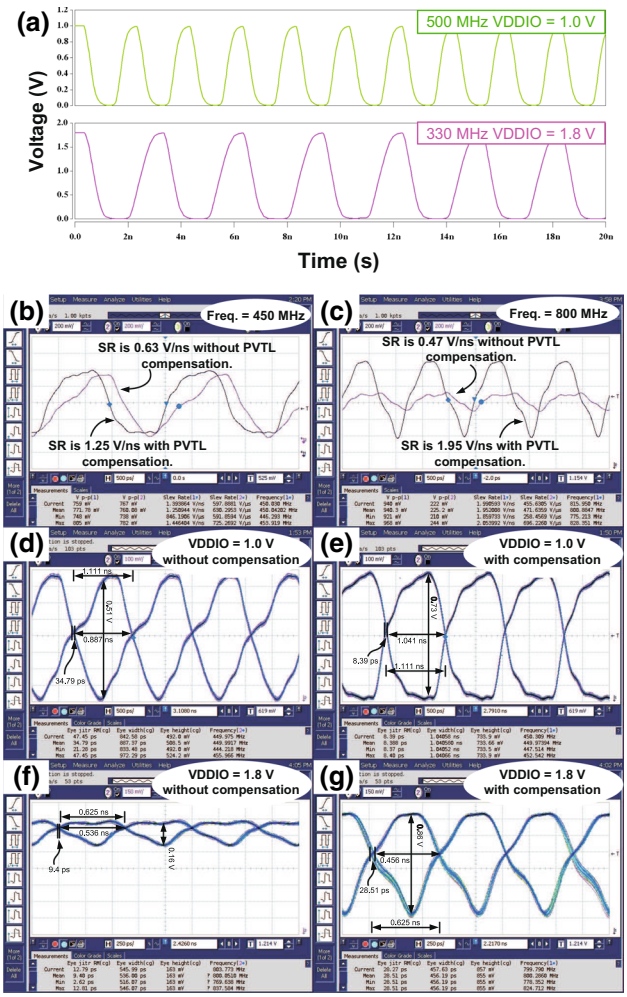


Fig. 8 **a** Simulation transient response of VPAD under different given VDDIO. **b**, **c** SR measurement with/without PVTL compensation for VDDIO = 1.0/1.8 V. **d**–**g** Eye diagrams of PAD with/without PVTL compensation for VDDIO = 1.0/1.8 V

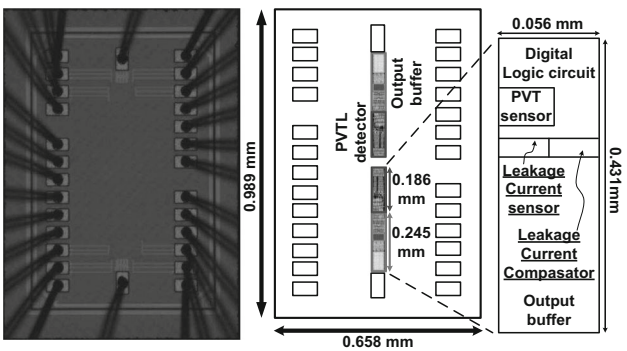


Fig. 9 Die photo and the block description of the proposed design

Table 1 Without/with PVTL compensation results at different VDDIOs

VDDIO	1.0 V	1.8 V
Data rate (MHz)	450	800
Eye jitter (ps)	34.79 → 8.39	9.4 → 28.51
Eye width (ns)	0.887 → 1.04	0.536 → 0.46
Eye height (V)	0.51 → 0.73 (43.1%)	0.16 → 0.86 (437.5%)
SR improvement (V/ns)	0.63 → 1.25 (98.4%)	0.47 → 1.95 (314.9%)
Power per MHz (μW/MHz)	55.6 → 68.9	125.3 → 98.5

is pulled up to 1.0 V to increase the stability. The static leakage current will then be reduced.

Referring to lower left corner of Fig. 3(a), an unstable gate drive of MP402 (dotted line), which might be caused by the disturbed parasitic capacitors, will make V_{gd} of MP401 increase in a short period. As a result, V_{401pd} will be much lower than VDD to cause overstress problem and severe gate leakage of MP401. $I_{leakage}$ of MP401 vs. V_{401pd} is depicted in Fig. 3(b). MP801 is the stabilizer driven by $\overline{Lo}$ as shown in lower left corner of Fig. 3(a) (solid line). The voltage drop of MP402 gate drive is reduced after compensation, which will maintain the voltage level of V_{401pd} quite steady. Therefore, V_{gd} of MP401 will be clamped within a tolerant voltage to enhance the SR.

Referring to Fig. 3(c–e), the simulation results of V_{MP402g}, V_{401pd}, and $I_{leakage}$ are revealed, respectively. Red lines denote the waveforms with leakage compensation, while green lines are those without leakage compensation by contrast. The voltage drop of green line in Fig. 3(c) forces V_{401pd} in Fig. 3(d) to be 0.43 V, which leads significant gate-oxide leakage current around 1000 nA in Fig. 3(e). However, the voltage drop of red line in Fig. 3(c) is smaller with leakage compensation. The overstress of V_{401pd} in Fig. 3(d) has been reduced to 0.72 V, which causes smaller leakage current around 600 nA in Fig. 3(e). Therefore, with the leakage compensation technique, the leakage of gate-oxide is surely reduced. Figure 4 shows the statistics of gate leakage current at different PVT corners.

2.3.2 Delay buffers

The function of Delay buffers is to reduce the dynamic leakage current. Referring to Fig. 2(e) again, Delay buffers are composed of inverter chains, where the symbols in the figure is for the sake of readability. Referring to Fig. 5(a), the dotted line indicates before adding Delay buffers, where the gate drive signal of MN402x (x = a, b, c) leads

Table 2 Performance Comparison of Output Buffers

	[9] *TCAS-I*	[6] *TCAS-I*	[7] *TCAS-I*	[4] *TCAS-I*	[5] *EL*	[11] *MEJ*	[8] *ISCAS*	[12] *EL*	This work
Year	2013	2013	2013	2014	2012	2013	2016	2017	2018
Process (μm)	0.09	0.09	0.18	0.5	0.35	0.04	0.09	0.09	0.09
Supply voltage (V)	1.2	1.2	0.9	5	3.3	0.9	1.0	1.0	1.0
Buffer type	Mixed	Mixed	Mixed	Analog	Analog	Mixed	Mixed	Mixed	Mixed
Transmitting voltage mode (V)	1.2 /2.5	1.2/2.5	0.9/1.8/ 3.3	0–5	0–3.3	0.9/1.8	1.0/2.0	1.0/1.2 / 1.8	1.0/1.8
Load Capacitor (pF)	15	20	20	1000	200	20	20	20	20
Data rate (MHz)	125	400/ 352	75/95/120	0.05	0.05	500/460	800/500	400/630/ 510	450/800
Slew rate (V/ns)	2.1–3.4	N/A	1.28–2.79	7.04×10^{-3}	2.75×10^{-3}	N/A	N/A	N/A	1.25/1.95
Process corners	Only TT FF SS	N/A	All corners	N/A	N/A	All corners	All corners	All corners	All corners
Compensation	PVT	N/A	PT	N/A	N/A	PVT	PV	PVTL	PVTL
Power (mW)	N/A	0.78	0.427	N/A	N/A	N/A	3.45	N/A	2.36
Worst FOM†	0.405	1.140	1.178	0.003	0.002	0.409	2.025	2.295	3.6

$FOM^{\dagger} = \frac{Process^2 \times Datarate}{Transmittingvoltagemode}$

those of MP401x (x = a, b, c) to result in NMOS transistors turned on before PMOS transistors turned off. Therefore, it will cause the current flowing through MP401 and MP402 to disturb the output signal of PAD and degrade the SR. However, after adding Delay buffers as the compensation mechanism, the comparison is shown in Fig. 5(b), (c) which shows that the delay of gate signals is shorten to increase the slew rate.

3 Implementation and measurement

The proposed buffer is fabricated using TSMC 1P6M 90 nm CMOS process without any thick-oxide device. Figure 6(a, b) show the worst-case waveforms of each corner including voltage and temperature variation when VDDIO = 1.0 V or 1.8 V, respectively. Figure 7(a, b) are the 200 times Monte Carlo histograms when VDDIO = 1.0 V or 1.8 V, respectively. Figure 7(a) shows that 1.0 V has the worst-case in FS corner, where the standard deviation increases from 6.78 (V/μs) to 6.31 (Vμs). On the other hand, Fig. 7(b) shows that 1.8 V has the worst-case in SS corner, where the standard deviation increases from 7.68 (V/μs) to 7.54 (V/μs). Figure 8(a) shows the simulation transient response of VPAD under different given VDDIO. Figure 8(b, c) show the voltages of PAD between with PVTL compensation and without PVTL compensation given VDDIO = 1.0/1.8 V, respectively. The SR is 0.63/0.47 (V/ns) before compensation and 1.25/1.95 (V/ns) after compensation, when VDDIO is 1.0/1.8 V, respectively. Eye diagrams of output buffer in different scenarios are given in Fig. 8(d–g). The height of the eye is improved by 43.1%/437.5% when VDDIO = 1.0/1.8 V, respectively. Figure 9 is the die photo of our design, where the overall area is 0.989 × 0.658 mm^2. The area of PVTL detector (PVT sensor + PVT decider + Leakage Current sensor) and Output buffer are 0.186 × 0.056 mm^2 and 0.245 × 0.056 mm^2, respectively. The overall measurements are tabulated in Table 1. Regarding comparison with prior works, it is tabulated in Table 2. Notably, our work is the only one to attain PVTL compensation and achieve maximum data rate 800 MHz when VDDIO = 1.8 V.

4 Conclusion

In the proposed design, the 2×VDD output buffer using PVTL detection is fabricated and realized with TSMC 1P6M 90 nm CMOS process. With the proposed compensation technique, the height of the eye diagram at 800 MHz is 0.86 V, where the height was 0.16 V before compensation by contrast. Besides, Leakage current compensator stabilizes the gate voltage of MP402g and prevents the PMOS transistors in Output stage from overvoltage hazards. Moreover, the benefits of leakage current compensation actually enhance the 1.95 (V/ns) slew rate and 800 (MHz) data rate, respectively.

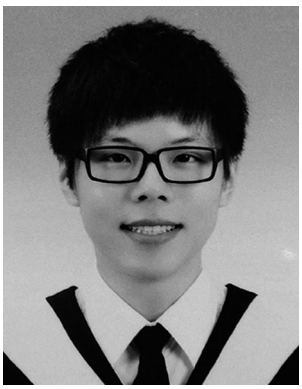
Acknowledgements The research was partially supported by Ministry of Science and Technology, Taiwan, under Grant MOST-105-2218-E-110-006- and MOST 107-2218-E-110-004-. The authors would like to convey thanks and gratefulness to CIC (Chip Implementation Center), Taiwan, for the assistance of thoughtful chip fabrication.

References

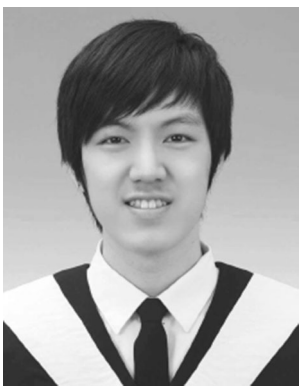
1. Shin, S.-K., Jung, S.-M., Seo, J.-H., Ko, M.-L., & Kim, J.-W. (2003). A slew rate controlled output driver using PLL as compensation circuit. *IEEE Journal of Solid-State Circuits*, *38*(7), 1227–1233.
2. Lee, T.-J., Chang, T.-Y., & Wang, C.-C. (2009). Wide-range 5.0/3.3/1.8-V I/O buffer using 0.35-m 3.3-V CMOS technology. *IEEE Transactions on Circuits and Systems—I: Regular Papers*, *56*(4), 763–772.
3. Razavi, B. (2001). *Short-channel effects and device models. Design of analog CMOS integrated circuits* (pp. 599–600). New York City: Mcgraw-Hill.
4. Grasso, A. D., Marano, D., Esparza-Alfaro, F., Lopez-Martin, A. J., Palumbo, G., & Pennisi, S. (2014). Self-biased dual-path push–pull output buffer amplifier for LCD column drivers. *IEEE Transactions on Circuits and Systems—I: Regular Papers*, *61*(3), 663–670.
5. Kim, J.-S., Lee, J.-Y., & Choi, B.-D. (2012). Slew-rate-enhanced rail-to-rail buffer amplifier for TFT LCD data drivers. *Electronics Letters*, *48*(15), 924–925.
6. Wang, C.-C., Chen, C.-L., Tseng, H.-Y., Hou, H.-H., & Juan, C.-Y. (2013). A 800 Mbps and 12.37 ps jitter bidirectional mixed-voltage I/O buffer with dual-path gate-tracking circuit. *IEEE Transactions on Circuits and Systems—I: Regular Papers*, *60*(1), 116–124.
7. Wang, C.-C., Chen, C.-L., Kuo, R.-C., Tseng, H.-Y., Liu, J.-W., & Juan, C.-Y. (2013). On-chip process and temperature monitor for self-adjusting slew rate control of 2×VDD output buffers. *IEEE Transactions on Circuits and Systems—I: Regular Papers*, *60*(6), 1432–1440.
8. Tsai, T.-Y., Teng, Y.-L., & Wang, C.-C. (2016). A nano-scale 2×VDD I/O buffer with encoded PV compensation technique. In *Proceedings of IEEE international symposium on circuits and systems (ISCAS)* (pp. 598–601).
9. Ker, M.-D., & Chiu, P.-Y. (2013). Design of 2× V_{DD}-tolerant I/O buffer with PVT compensation realized by only 1× V_{DD} thin-oxide devices. *IEEE Transactions on Circuits and Systems—I: Regular Papers*, *60*(10), 2549–2560.
10. Bazes, M. (2004). Output buffer impedance control and noise reduction using a speed-locked loop. In *IEEE international solid-state circuits conference on digest of technical papers* (pp. 486–541).
11. Wang, C.-C., Lu, W.-J., Juan, K.-W., Lin, W., Tseng, H.-Y., & Juan, C.-Y. (2015). Process corner detection by skew inverters for 500 MHz 2×VDD output buffer using 40-nm CMOS technology. *Microelectronics Journal*, *46*(1), 1–11.
12. Wang, C.-C., Tsai, T.-Y., Lee, T.-J., & Ruan, K.-W. (2017). 2×VDD output buffer with 36.4% slew rate improvement using leakage current compensation. *Electronics Letters*, *53*(2), 62–64.

13. Bae, W., & Jeong, D.-K. (2015). A power-efficient 600-mVpp voltage-mode driver with independently matched pull-up and pull-down impedances. *International Journal of Circuit Theory and Applications*, *43*(12), 2057–2071.
14. Saxena, S., Nandwana, K., & Hanumolu, P. K. (2014). A 5 Gb/s energy-efficient voltage-mode transmitter using time-based de-emphasis. *IEEE Journal of Solid-State Circuits*, *49*(8), 1827–1836.
15. Chen, C.-L., Tseng, H.-Y., Kuo, R.-C., Wang, C.-C. (2012). A slew rate self-adjusting $2\times$ V_{DD}VDD output buffer with PVT compensation. In *International symposium on VLSI design, automation, and test (VLSI-DAT)* (pp. 1–4).
16. Wang, C.-C., Kuo, R.-C., & Liu, J.-W. (2010). 0.9 V to 5 V Bidirectional mixed-voltage I/O buffer with an ESD protection output stage. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *57*(8), 612–616.
17. Cao, K.-M., Lee, W.-C., Liu, W., Jin, X., Su, P., Fung, S. K. H., An, J. X., Yu, B., & Hu, C. (2000). BSIM4 gate leakage model including source–drain partition. In *International electron devices meeting* (pp. 815–818).

Chua-Chin Wang received the Ph.D. degree in Electrical Engineering from SUNY (State University of New York) at Stony Brook, USA, in 1992. He then joined Department of Electrical Engineering, National Sun Yat-Sen University, Taiwan, and became a full professor since 1998. He was Chairman of Department of Electrical Engineering, National Sun Yat-Sen University during 2009–2012. Dr. Wang's research interests include memory and logic circuit design, communication circuit design, and interfacing I/O circuits. Particularly, he applies most of his research results on biomedical, memories, consumer electronics, and wireless communication applications, such as implantable ASIC/SOC, DVB-T/H and NTSC TV circuits, low power memory, high speed digital logic, etc. He has won the Outstanding Youth Engineer Award of Chinese Engineer Association in 1999, and NSC Research Award from 1994 to 1999. In 2000. He co-founded Asuka Semiconductor Inc., which is an IC design house located in renowned Hsinchu Scientific Park, Taiwan, and became Executive Secretary in 2005. In 2005, he was awarded with Best Inventor Award in National Sun Yat-Sen University, Taiwan. In 2006, he won Distinguished Engineering Professor Award of Chinese Institute of Engineers and Distinguished Engineer Award of Chinese Institute of Electrical Engineering in the same year. He also won Distinguished Electrical Engineering Professor Award of Chinese Institute of Electrical Engineers in 2007. In 2008, he won Outstanding Paper Award of 2008 IEEE Inter. Conf. of Consumer Electronics. In 2009, he again won Best Inventor Award. He was elevated to be Distinguished Professor of National Sun Yat-Sen University in 2010. He became IET Fellow in 2012. Prof. Wang has served as program committee members in many international conferences. He was Chair of IEEE Circuits and Systems Society (CASS) for 2007–2008, Tainan Chapter. He was also the founding Chair of IEEE Solid-State Circuits Society (SSCS), Tainan Chapter for 2007–2008, and the founding Consultant of IEEE NSYSU Student Branch. He is also a member of the IEEE CASS Multimedia Systems & Applications (MSA), VLSI Systems and Applications (VSA), Nanoelectronics and Giga-scale Systems (NG), and Biomedical Circuits and Systems (BioCAS) Technical Committees. He is a senior member of IEEE since 2004. He was Chair of IEEE CASS Nanoelectronics and Giga-scale Systems (NG) Technical Committee for 2008–2009. Since 2010, he has been invited to be Associate Editors of IEEE Trans. on TCAS-I and TCAS-II. Currently, he is also serving as Associate Editor of IEICE Transactions on Electronics, and Journal of Signal Processing. Dr. Wang was General Chair of 2007 VLSI/CAD Symposium. He was General Co-Chair of 2010 IEEE Inter. Symp. on Next-generation Electronics (2010 ISNE). He is General Chair of 2011 IEEE Inter. Conf. on IC Design and Technology (2011 ICICDT), and General Chair of 2012 IEEE Asia-Pacific Conference on Circuits & Systems (2012 APCCAS).



Tsung-Yi Tsai was born in Taiwan, Kaohsiung in 1988. He received the B.S. degree in Electrical Engineering and the M.S. degree in VLSI Design Laboratory from National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2014. He is currently working toward Ph.D. degree in electrical engineering at National Sun Yat-Sen University. His current research interests are VLSI design, high voltage mixed-signal circuit design, automobile system design, and interfacing I/O circuits.



Wei Lin was born in the United States of America in 1990. He received the B.S. degree in Electrical Engineering from National Sun Yat-sen University in 2013, and currently pursuing the M.S. degree in Electrical Engineering from National Sun Yat-sen University since 2013. His current research interests are VLSI design, high voltage mixed-signal circuit design, automobile system design, and interfacing I/O circuits.