A Dynamic Leakage and Slew Rate Compensation Circuit for 40-nm CMOS Mixed-Voltage Output Buffer

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***Abstract*— This paper proposes a 40-nm CMOS 2 × VDD buffer with slew rate (SR) variation compensated and dynamic leakage reduction during signal transitions. By using the dual variation detectors, five process corners for both nMOS and pMOS could be detected. Thus, the SR deviations will be significantly reduced by controlling the switches of the output stage accordingly. Besides, leakage reduction circuit will shut down current paths to reduce dynamic leakage after signal transitions are completed. This buffer design is implemented using the typical 40-nm CMOS process, where the active area is 0.052 × 0.213 mm^2. The measured worst case of SR variation improvement is 20.8% and 54.9% when VDDIO is 0.9 and 1.8 V, respectively. The peak dynamic leakage is reduced to 41.0% and 37.5% at 0.9 and 1.8 V, respectively.**

***Index Terms*— Dynamic leakage reduction, I/O buffer, mixed-voltage tolerant, process–voltage–temperature (PVT) variation, slew rate compensation.**

I. Introduction

With the fast development of the portable devices, advanced CMOS technologies become the major trend because of low power, high speed, and miniature size. However, the side effects, e.g., severe process–voltage–temperature (PVT) variations and large leakage current, arise in advanced CMOS processes [1]– [3].

For the development of mixed-voltage output drivers, the reliability issue caused by the HV signals is the main concern [4]–[9]. When it comes to the nanoscale CMOS process, the SR variation caused by PVT variations and large leakage current (occurred in the mixed-voltage output buffer) becomes a new and serious problem [2]. In order to compensate the SR variation, the multiple current paths are used [10]. However, the PVT corners are not detected directly in the previous work [10]. The phase-locked loop (PLL)-based PVT detection circuit was used to detect three process corners of typical–typical (TT), fast–fast (FF), and slow–slow (SS) [11]–[14]. However, it requires multiple clock cycles. Another delay-cell-based PVT detection circuit with one cycle was presented for the three-corner detection of TT, FF, and SS [15]–[17]. To cover the five process corners of TT, FF, SS, fast–slow (FS), and slow–fast (SF), the skewed delay cells-based detection circuits were presented [18], [19]. It requires lots of control signals, and the area is too large. Besides, the problem of leakage current is not considered in these prior works [18], [19]. To compensate the dynamic leakage current and the SR variation caused by PVT variations, including five corners of TT, FF, SS, FS, and SF, the dual PVT variation detection circuits using only one cycle are proposed in this paper. After compensation, the SR variation is improved by 20.8% and 54.9% for VDDIO at 0.9 and 1.8 V, respectively. Leakage reduction upon signal transition is at least 37.5%. The data rate is measured on silicon to be 725/710 MHz when the supply voltage is 0.9/1.8 V, respectively.

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II. 2 × VDD Output Buffer Circuit Design

Fig. 1 shows the block diagram of the proposed output buffer with a PVTL compensation circuit, a leakage reduction circuit, and the output stage. The PVTL compensation circuit is composed of dual PVT variation detectors and one digital logic circuit.

The PVTL corner is defined by the corner signals, NF, NS, PF, and PS, as well as the leakage detection signals, V_{NL} and V_{PL}. Then, the digital logic circuit generates corresponding control codes, Pcode[3:1] and Ncode[3:1], based on the truth table in Fig. 1 to control the three parallel paths of pMOS and nMOS transistors in the output stage, respectively. Thus, the SR variation and dynamic leakage current could be compensated. Notably, Clk is a 100-kHz square wave signal. En is the enabling signal of the PVTL compensation circuit. RstPVT and RstL are in charge of the compensation of PVT variation and leakage reduction, respectively.

N-PVT variation detector detects the PVT corners for nMOS by two steps. In the first step, a discharging signal, V_{N1}, is generated with the slope of the falling edge dependent on the PVT corners. However, the falling speed of the slow corner is not enough to reach the reference voltage V_N. Therefore,

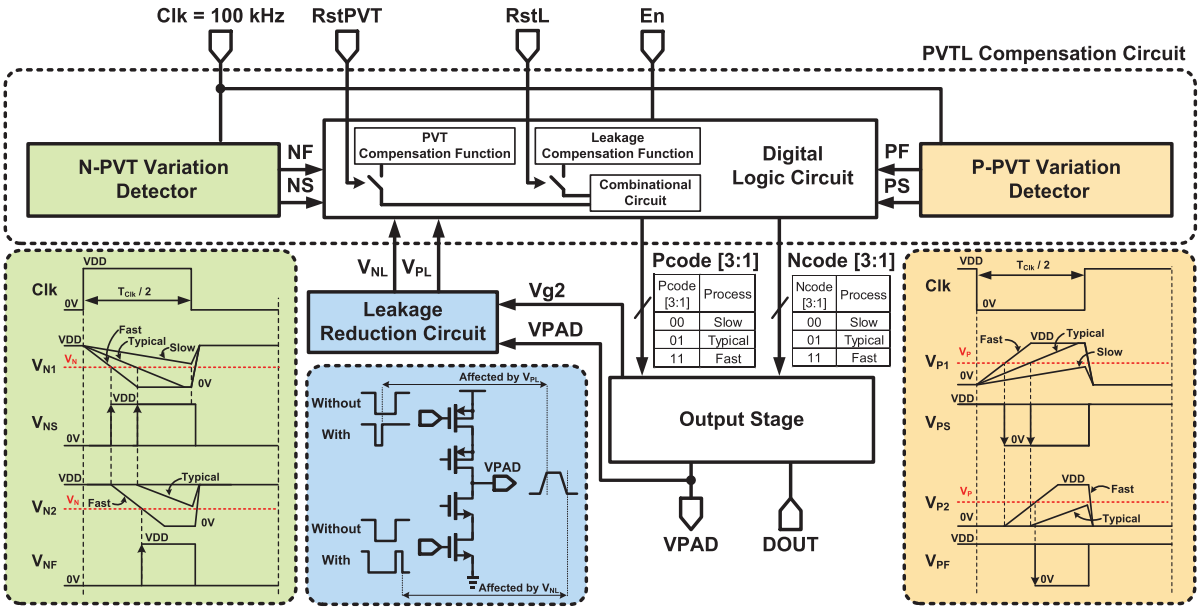

Fig. 1. Block diagram of the proposed 2 × VDD output buffer.

after comparing with the reference voltage, the digital signal, $V_{\rm NS}$, with the signal width dependent on the PVT variation is obtained. Thus, NS could refer to the slow corner of nMOS. In the second step, $V_{\rm NF}$ is generated by comparing the corner signal, V_{N2}, and the reference signal, V_N. By the same approach, NF can then differentiate the typical corner from the fast corner of CMOS. Similarly, the P-PVT variation detector generates PS and PF by using the rising edge of the corner signals, V_{P1} and V_{P2}, and the reference signal, V_P, to distinguish the slow corner and typical corner of pMOS, respectively.

Leakage reduction circuit generates the control signals, $V_{\rm NL}$ and $V_{\rm PL}$, with respect to VPAD. At the slow corner, the auxiliary current paths would be turned ON to compensate the SR. However, it causes additional leakage current during signal transitions. Thus, $V_{\rm PL}$ is used to turn OFF the auxiliary pMOS current paths to suppress leakage currents after the low to high transition at VPAD is done. The mechanism waveform is shown in Fig. 1 (blue region). The symbol "Without" indicates before compensation, and "With" indicates after compensation. By contrast, when high-to-low transition is completed, $V_{\rm NL}$ will turn OFF corresponding nMOS transistors of the output stage to avoid extra power consumption.

A. N-PVT & P-PVT Variation Detector

Fig. 2 shows the block diagrams and waveforms of the dual PVT variation detectors. Each of N-PVT and P-PVT variation detectors consists of two delay cells, two D-type flip flops (DFFs), and a bias circuit.

Bias circuit consists of two diode-connected pMOS transistors, where the bulks of these two transistors are coupled to its own source to make V_N and V_P be equally divided.

In each variation detector, two cascaded delay cells are used to determine fast, typical, and slow corners. N-Delay Cell 1 is aimed at the differentiation of the slow corner, and N-Delay Cell 2 is in charge of the typical corner. V_N is a reference voltage for N-Delay Cells 1 and 2.

N-Delay Cell 1 is composed of a high-skew inverter, an on-chip capacitor, a comparator, and an inverter. Clk signal is a periodic signal with 50% duty cycle from the system. During the high level of Clk, C_{N1} is driven by the high-skew inverter 1, such that V_{N1} would drop at a very slow rate. Thus, the slope of V_{N1} could be used to determine the PVT corners. Referring to the waveforms in the left-hand side of Fig. 1, the SR of high-skew inverter 1 for driving C_{N1} could be expressed as follows:

$$\mathrm{SR}_{\mathrm{NS}(x)} = \frac{\Delta \mathrm{V}}{T_{\mathrm{NS}(x)}} = \frac{I_{\mathrm{NS}(x)}}{C_{N1}} \tag{1}$$

where the subscript, x, is denoted by S, T, and F, referring to the slow, typical, and fast corners, respectively. $I_{\rm NS}$ is the discharging current of the high-skew inverter 1.

In order to detect the slow corner, the discharging time $T_{\mathrm{NS}(S)}$, from VDD to V_N (=(1/2) × VDD), should be longer than one half of the Clk period. On the contrary, the discharging time $T_{\mathrm{NS}(F,T)}$, from VDD to 0 V, must be less than the positive part of Clk at the typical and fast corners. Thus, the following equations could be derived:

$$T_{\mathrm{NS}(S)} = \frac{\mathrm{VDD} \cdot C_{N1}}{2 \cdot I_{\mathrm{NS}(S)}} \geq \frac{T_{\mathrm{Clk}}}{2} \tag{2}$$

$$T_{\mathrm{NS}(T,F)} = \frac{\mathrm{VDD} \cdot C_{N1}}{I_{\mathrm{NS}(T,F)}} < \frac{T_{\mathrm{Clk}}}{2}. \tag{3}$$

The critical condition is determined by the slow corner and the typical corner. Thus, the range of C_{N1} could be found as follows:

$$\frac{I_{\mathrm{NS}(S)} \cdot T_{\mathrm{Clk}}}{\mathrm{VDD}} \leq C_{N1} < \frac{I_{\mathrm{NS}(T)} \cdot T_{\mathrm{Clk}}}{2 \cdot \mathrm{VDD}}. \tag{4}$$

For the N-Delay Cell 2, the discharging process is within the pulse duration of $V_{\rm NS}$, which is the required time from V_N to 0 V for $V_{\rm NS}$. Thus, $D_{\rm NS}$, the pulse duration of $V_{\rm NS}$, could be derived by

$$D_{\mathrm{NS}} = \frac{T_{\mathrm{Clk}}}{2} - \frac{T_{\mathrm{NS}(T,F)}}{2}. \tag{5}$$

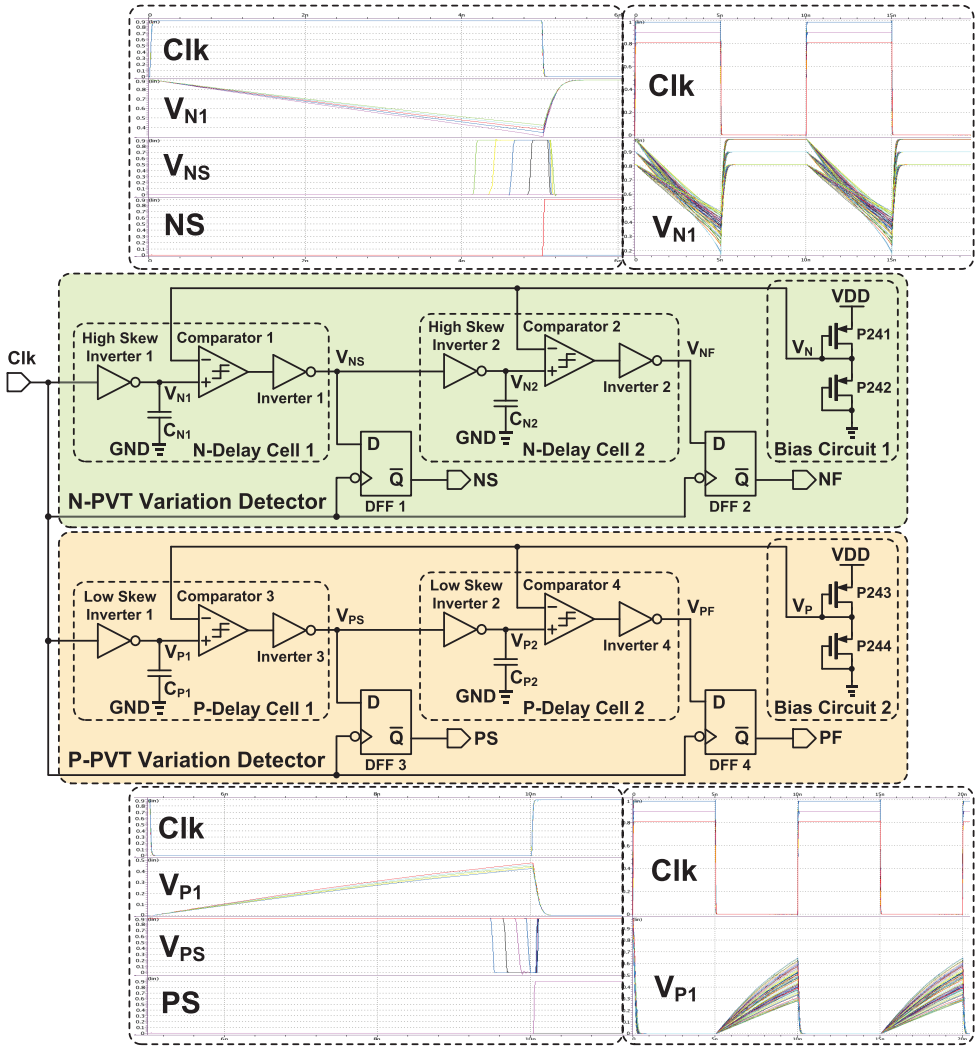

Fig. 2. Block diagrams and waveforms of the dual PVT variation detectors.

Similarly, in order to detect the PVT corner correctly, the discharging time should be larger than D_{NS} for the typical corner. Moreover, the discharging time of the fast corner is less than D_{NS}. Then, the discharging time of the N-Delay Cell 2 could be expressed as the following equations:

$$T_{\mathrm{NF}(T)} = \frac{\mathrm{VDD} \cdot C_{N2}}{2 \cdot I_{\mathrm{NF}(T)}} \geq D_{\mathrm{NS}} \tag{6}$$

$$T_{\mathrm{NF}(F)} = \frac{\mathrm{VDD} \cdot C_{N2}}{I_{\mathrm{NF}(F)}} < D_{\mathrm{NS}}. \tag{7}$$

By combining (2), (3), and (5)–(7), the range of C_{N2} can be decided by

$$I_{\mathrm{NF}(T)} \cdot \left(\frac{T_{\mathrm{Clk}}}{\mathrm{VDD}} - \frac{C_{N1}}{I_{NS(F)}} \right) \leq C_{N2} < \frac{I_{\mathrm{NF}(F)}}{2} \cdot \left(\frac{T_{\mathrm{Clk}}}{\mathrm{VDD}} - \frac{C_{N1}}{I_{NS(T)}} \right). \tag{8}$$

Referring to Fig. 2, the components in the P-Delay Cell are generally the same as those in the N-Delay Cell except that the high-skew inverter is replaced with a low-skew inverter. Thus, the rising edge of V_{PS} and V_{PG} values are used to generate compensation signals when Clk is at low state. For both PVT variation detectors, the judgment of process corners will be completed in the first half cycle of the clock and generate digital codes, NS, NF, PS, and PF, through DFFs in the next half. The truth table is shown in Table I.

TABLE I
TRUTH TABLE OF DUAL PVT VARIATION DETECTORS

PVT corners	$T_{\mathrm{NS}}/T_{\mathrm{PS}}$	$T_{\mathrm{NF}}/T_{\mathrm{PF}}$	NS/PS	NF/PF
Slow	$\geq \frac{T_{\mathrm{Clk}}}{2}$	$\geq \frac{T_{\mathrm{Clk}}}{2}$	1	1
Typical	$< \frac{T_{\mathrm{Clk}}}{2}$	$\geq \frac{T_{\mathrm{Clk}}}{2}$	0	1
Fast	$< \frac{T_{\mathrm{Clk}}}{2}$	$< \frac{T_{\mathrm{Clk}}}{2}$	0	0

B. Leakage Reduction Circuit

Fig. 3 shows the schematic of the leakage reduction circuit and how it performs the compensation technique. Referring to Fig. 1 again, Vg2 is generated from the output stage. Notably, Vg2 is biased at 0 and 0.9 V for VDDIO at $1 \times$ VDD

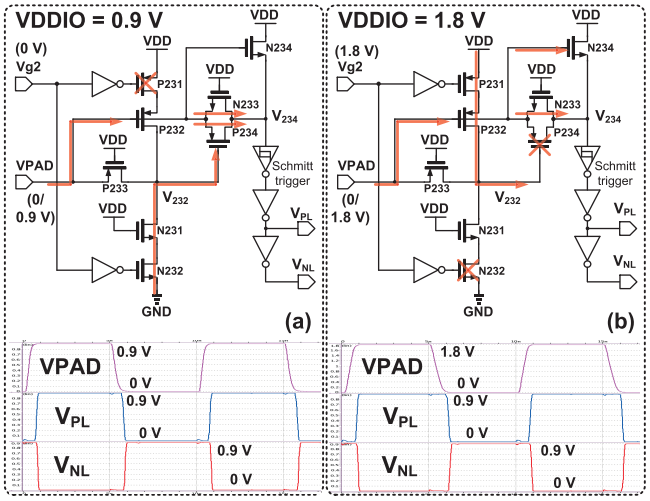

Fig. 3. Schematics and functionality of a leakage reduction circuit when (a) VDDIO = 0.9 V and (b) VDDIO = 1.8 V.

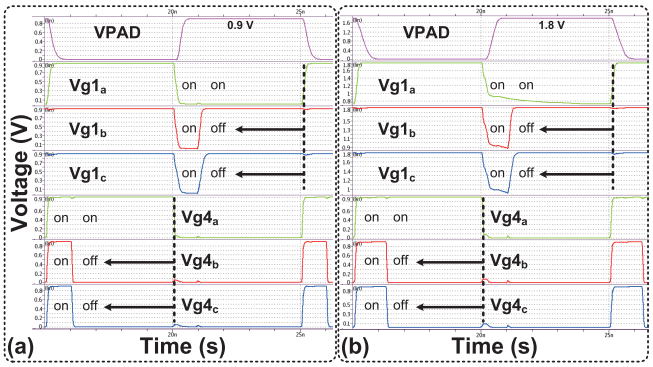

Fig. 4. Leakage reduction mechanism in the SS corner for (a) VDDIO = 0.9 V and (b) VDDIO = 1.8 V.

and 2 × VDD, respectively. When VDDIO = 1 × VDD (0.9 V), P231 is OFF, and N231 and N232 are ON to turn ON P234. Thus, VPAD is transmitted to V_{234} through N233 and P234. The Schmitt trigger and the two inverters, INV_{233} and INV_{234}, would generate delayed signals, V_{PL} and V_{NL}, for the digital logic circuit to turn OFF the auxiliary leakage current paths. When VDDIO = 2 × VDD (1.8 V), N232 is OFF. VPAD of 1.8 V would charge V_{234} to 0.9 V by N234 and the clamping MOS, N233. In this case, V_{232} will be clamped at 0.9 V. Therefore, P231, P232, P233, N231, and N233 are used to avoid overvoltage hazards caused by 1.8 V at VPAD. Again, after the completion of data transferring, the Schmitt trigger will generate delayed signals, V_{PL} and V_{NL}, to adjust compensation codes.

Next, as shown in Fig. 4(a) and (b), it demonstrates how the leakage reduction mechanism works. Notably, the example is the SS corner, which needs to be compensated by turning ON three current paths in both charging and discharging states. Referring to Fig. 4(a), VDDIO = 0.9 V, and $Vg4_a$ stands for the always-turn-ON signal. However, the turn-ON period of the other signals, namely, $Vg4_b$ and $Vg4_c$, will be shortened to turn OFF auxiliary discharging current paths after VPAD becomes logic 0. Thus, the source–drain current is reduced. Similarly, at the rising edge of VPAD, $Vg1_a$ stands for the always-turn-ON signal. $Vg1_b$ and $Vg1_c$ will be shortened accordingly to turn OFF auxiliary charging current after VPAD becomes logic 1. Referring to Fig. 4(b), the similar simulation is carried out, given VDDIO = 1.8 V.

TABLE II
CODES IN DIGITAL LOGIC CIRCUIT

PS	PF	V_{PL}	Pcode[3]	Pcode[2]	Pcode[1]
0	0	0/1	0	0	1
0	1	0/1	0	1/0	1
1	1	0/1	1/0	1/0	1
NS	NF	V_{NL}	Ncode[3]	Ncode[2]	Ncode[1]
0	0	0/1	0	0	1
0	1	0/1	0	1/0	1
1	1	0/1	1/0	1/0	1

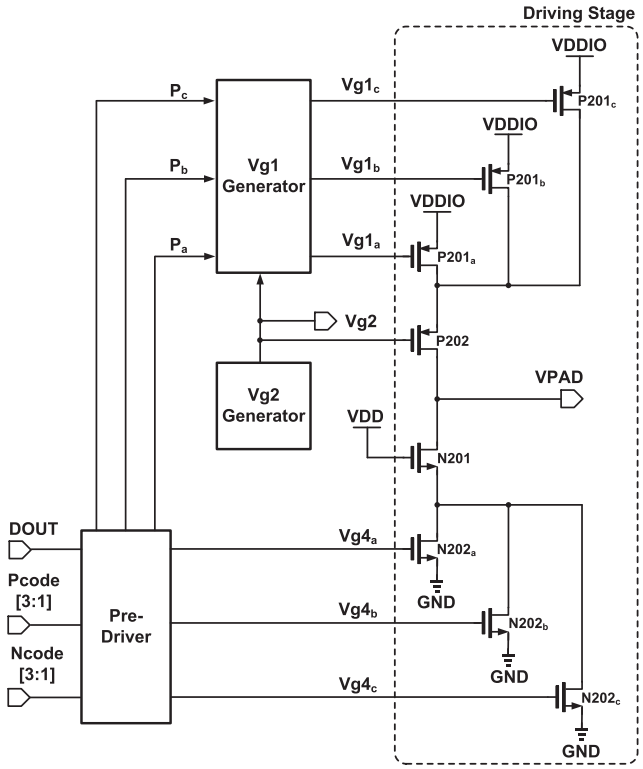

Fig. 5. Block diagram of the output stage.

C. Digital Logic Circuit

Digital logic circuit in Fig. 1 receives six compensation codes, i.e., NF, NS, PF, PS, V_{NL}, and V_{PL}, 3 control signals, including En, RstPVT, and RstL, to fully manage entire 2 × VDD Output Buffer. When RstL is logic high, it will turn OFF the leakage compensation function. When RstPVT is logic high, it will turn OFF the PVT compensation function to keep Ncode[3:1] and Pcode[3:1] equal to 01. When En is logic high, Ncode[3:1] and Pcode[3:1] will be 11 to activate all the current paths. The truth table of functionality is tabulated in Table II.

D. Output Stage

Referring to Fig. 5, the output stage is composed of a predriver, a Vg1 Generator, a Vg2 Generator, and a

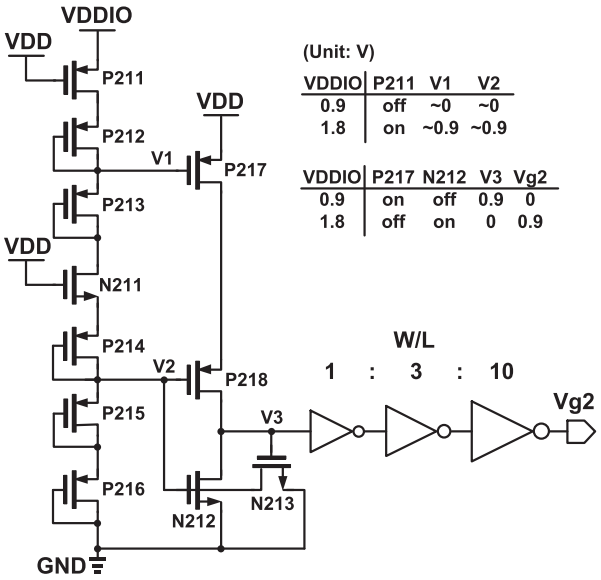

Fig. 6. Schematic of the Vg2 Generator.

driving stage. The predriver receives the compensation codes, i.e., Pcode[3:1], Ncode[3:1], and digital input signal, DOUT, to drive corresponding MOS switches. To prevent the overvoltage hazards from VDDIO, the driving signals, P_a, P_b, and P_c, are shifted high by the Vg1 Generator. Therefore, the Vg2 Generator works as a detector to notify the Vg1 Generator of boosting voltage level or not. Driving stage provides three parallel MOS switches to adjust output SR according to detected PVT corners.

1) Predriver: Predriver is a combinational logic circuit, which generates $P_a \sim P_c$ and $\text{Vg4}_a \sim \text{Vg4}_c$ based on Ncode[3:1], and Pcode[3:1]. DOUT is the signal from digital systems.

2) Vg2 Generator: Vg2 Generator in Fig. 6 works as a VDDIO detector. When VDDIO $= 1\times$VDD (0.9 V), P211 will cut off to make $V1$ and $V2$ close to 0 V. Then, P217 and P218 will be turned ON, such that $V3$ becomes VDD, which will further turn ON N213 to fully cut off N212. Thus, $V3$ is charged to VDD, such that Vg2 is pulled to ground. When VDDIO $= 2 \times$ VDD (1.8 V), $V1$ and $V2$ are pulled high and clamped at 0.9 V (close to 0.9 V) from the G–D-shorted MOS string to cut off P217 and P218. N212 will then be turned ON to pull down $V3$ to zero by N212. Thus, Vg2 of 0.9 V is generated. The operation tables are included in Fig. 6. Moreover, the aspect ratios of MOS transistors in the inverter chain are revealed.

3) Vg1 Generator: Fig. 7 shows the schematic of the Vg1 Generator, which is mainly composed of three-level shift circuits. Each circuit is in charge of its corresponding current switch in the driving stage. For simplicity, the symbol, x, is used to denote a, b, and c, for the three-level shift circuits in the following discussion. When VDDIO $= 1 \times$ VDD (0.9 V), Vg2 $= 0$ V, the output ofNAND gate will turn ON N221 and N222. Thus, Vg1_x would be controlled by Px through the path of N222. Therefore, Vg1_x could be discharged to 0 V by N222 and N226 when P_x is logic 0. If P_x is

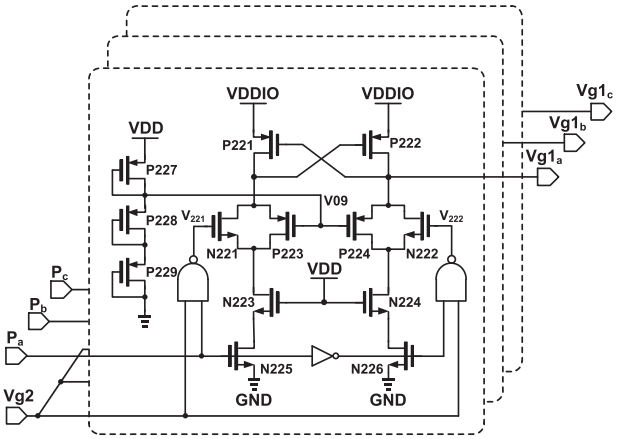

Fig. 7. Schematic of the Vg1 Generator.

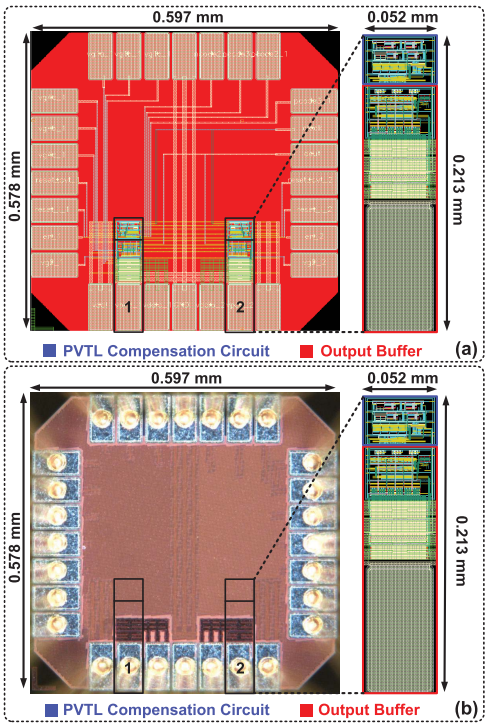

Fig. 8. (a) Layout. (b) Die photograph.

logic 1, N225 will be turned ON to activate P222, such that VDDIO will charge Vg1_x to $1 \times$ VDD. On the other hand, when VDDIO $= 2 \times$ VDD (1.8 V) and Vg2 $= 0.9$ V, the outputs ofNAND gates, V221 and V222, would depend on P_x. Because the bias voltage V09 is clamped at the lower limitation of Vg1_x, i.e., 0.9 V, Vg1_x would be discharged to 0.9 V through P224 when P_x is logic 0. When P_x is logic 1, Vg1_x is pulled to $2 \times$ VDD by P222. In this case, N224 and N226 are protected from HV threat by N222 with V222 at 0.9 V. The function table is also included in Fig. 7.

III. Implementation and Measurement

The proposed $2 \times$ VDD I/O buffer is implemented using the TSMC 40-nm CMOS process. The layout and die photograph are shown in Fig. 8(a) and (b), respectively, where the

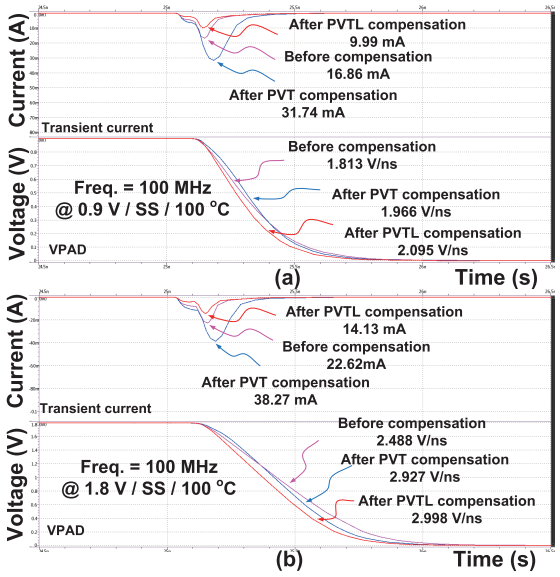

Fig. 9. Simulated dynamic leakage current for (a) VDDIO at 0.9 V and (b) VDDIO at 1.8 V.

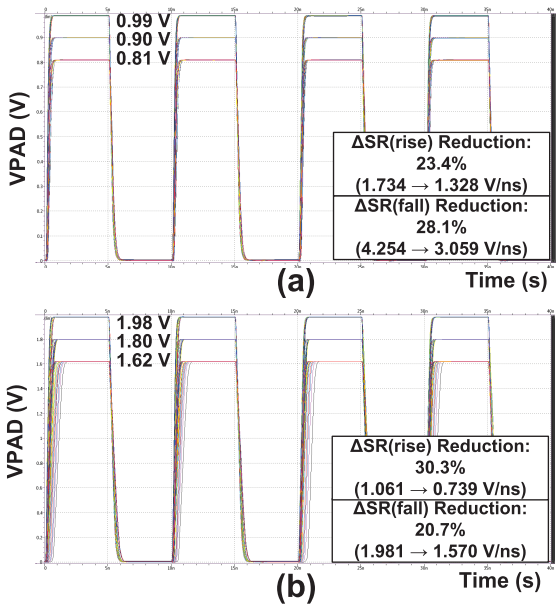

Fig. 10. Simulated waveforms of VPAD at all corners for (a) VDDIO at 0.9 V and (b) VDDIO at 1.8 V.

overall area is 0.578×0.597 mm^2 and the active area is 0.052×0.213 mm^2.

Fig. 9 reveals the waveforms of dynamic leakage current and VPAD. The dynamic leakage current is reduced from 16.86 to 9.99 mA for VDDIO at 0.9 V. Besides, the leakage current reduction is from 22.62 to 14.13 mA for VDDIO at 1.8 V. The SR is improved to 2.095 and 2.998 V/ns for VDDIO at 0.9 and 1.8 V, respectively. Fig. 10 shows the waveforms of VPAD at all corners. The SR variation, i.e., ΔSR, is improved from 20.7% to 30.3% for different cases. The compensation results are revealed in Table III.

Apparently, the process characteristic of each die is unknown. Therefore, to justify the functionality of PVT

TABLE III
WITHOUT/WITH PVTL COMPENSATION RESULTS AT DIFFERENT VDDIOS

VDDIO (V)	0.9	1.8
ΔSR_{rise} Reduction (%)	23.4	30.3
ΔSR_{fall} Reduction (%)	28.1	20.7
Dynamic leakage current reduction (%)	41.0	37.5
Dynamic leakage current (mA)	16.86→9.99	22.62→14.13

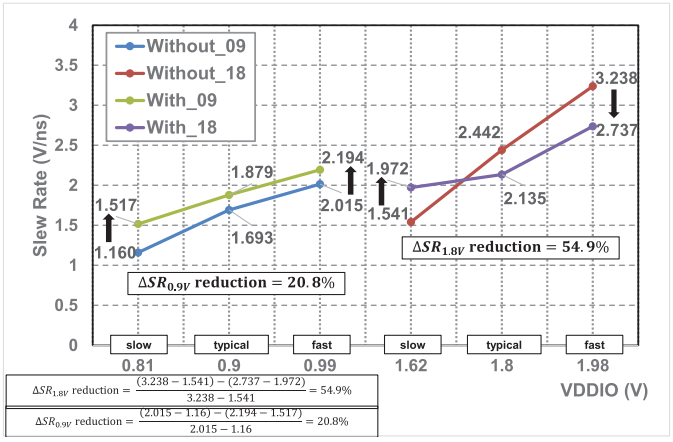

Fig. 11. Measurement of SR, given different VDDIOs.

variation detectors, Fig. 11 shows the measurement result of SR, given different VDDIOs. The negative 10% VDDIO voltage (namely, 0.81 and 1.62 V, slow condition) should have smaller SR than that in nominal voltages before compensation due to the minimal number of turned-ON current paths. The SR increases after the PVT variation detectors turn ON additional current paths. On the other hand, the positive 10% VDDIO voltage (namely, 0.99 and 1.98 V, fast condition) should have smaller SR after the PVT variation detectors turn OFF auxiliary current paths. However, referring to Fig. 11 again, the SR value (2.194) with compensation is higher than that (2.015) without compensation due to the process variations. Finally, the reduction of $\Delta SR_{0.9\,V}$ and $\Delta SR_{1.8\,V}$ is 20.8% and 54.9%, respectively. Fig. 12(a)–(f) shows the measurement waveforms with respect to Fig. 11.

Fig. 13(a) shows the statistic histogram of Monte Carlo based on simulations. The deviation before and after PVTL compensation is 4.79–6.35 and 4.32–5.16 (V/μs), respectively. Two examples of Monte Carlo simulations with 0.9 V/FS and 1.8 V/SS corners are demonstrated in Fig. 13(b) and (c), which clarifies how the SR deviations are achieved.

Power consumption, leakage, and area are key performance indicators to I/O design. The worst case power consumption before and after PVTL compensation is 19.53 and 19.04 mW, respectively, where both simulation results are generated given 725-MHz input signal, 1.98 V, FF corner. Utilizing the PVTL compensation circuit saves 0.8% on average power than that of only an output buffer. Referring to Fig. 9 and Table III, the dynamic leakage current without compensation is 16.86 and 22.62 mA, given VDDIO = 0.9 and 1.8 V, respectively. However, the leakage reduction improves 41% and 37.5% after PVTL compensation. The area overhead

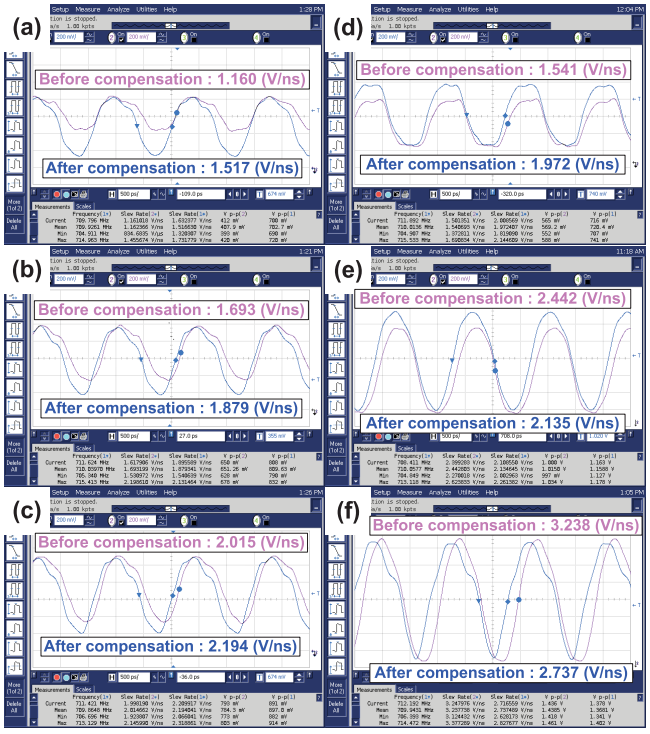

Fig. 12. Measured waveforms on 710-MHz data rate of the output signal, VPAD, for (a) 0.81 V/slow die, (b) 0.9 V/nominal die, (c) 0.99 V/fast die, (d) 1.62 V/slow die, (e) 1.8 V/nominal die, and (f) 1.98 V/fast die.

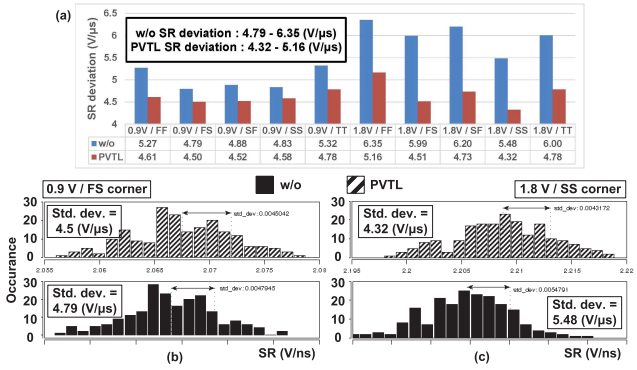

Fig. 13. (a) Monte Carlo simulation results of SR deviation at all corners. (b) Two hundred times simulation at the FS corner at 0.9 V/25 °C. (c) Two hundred times simulation at the SS corner at 1.8 V/25 °C.

of the PVTL compensation circuit (38.47 × 24.08 μm^2) comparing with the overall size of one single 2 × VDD output buffer circuit is 8.36%.

Fig. 14 shows the measurement environment for the proposed design. The measured waveforms of the output signal, VPAD, are revealed in Fig. 15. The maximum data rate of VPAD is 725 and 710 MHz, given VDDIO at 0.9 and 1.8 V, respectively, by measurement. The performance improvement of SR is from 1.15 to 1.45 V/ns and from 2.14 to 2.61 V/ns for VDDIO at 0.9 and 1.8 V, respectively. The improvement of SR is 26.1% and 22% after PVTL compensation is activated. The eye diagrams in different scenarios are shown in Figs. 16 and 17. After compensation,

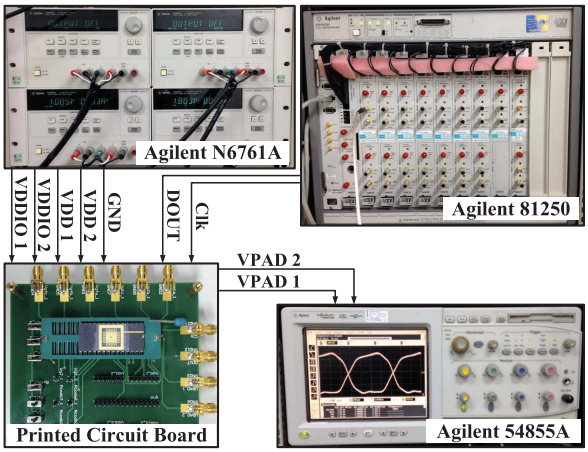

Fig. 14. Measurement environment and PCB for the proposed mixed-voltage output buffer.

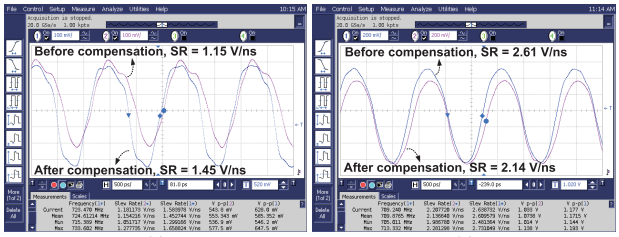

Fig. 15. Measured waveforms at its maximum data rate of the output signal, VPAD, for (a)VDDIO at 0.9 V/25 °C/725 MHz and (b) VDDIO at 1.8 V/25 °C/710 MHz.

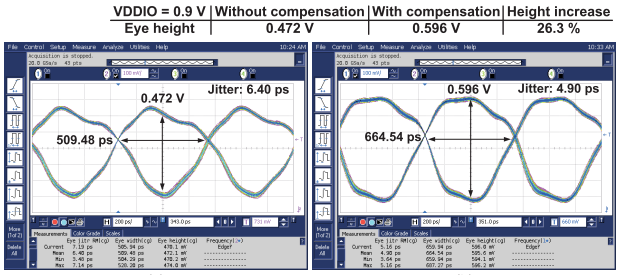

Fig. 16. Eye diagrams (a) without and (b) with PVTL compensations when VDDIO = 0.9 V/25 °C.

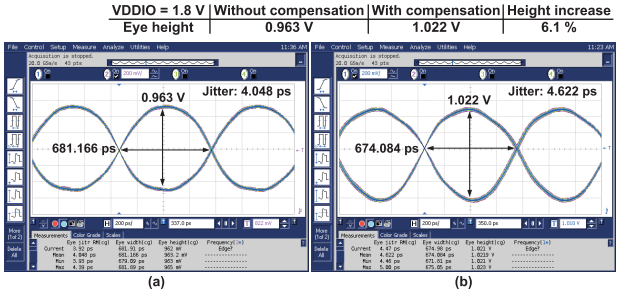

Fig. 17. Eye diagrams (a) without and (b) with PVTL compensations when VDDIO = 1.8 V/25 °C.

the height of eye diagrams is increased to 26.3% (from 0.472 to 0.596 V) and 6.1% (from 0.963 to 1.022 V), given VDDIO at 0.9 and 1.8 V, respectively.

TABLE IV
PERFORMANCE COMPARISON OF OUTPUT BUFFERS

	[17] *TCAS-I*	[16] *TCAS-II*	[18] *TCAS-I*	[7] *JSSC*	[19] *MEJ*	This work
Year	2013	2010	2013	2006	2015	2016
Process (nm)	90	180	180	130	40	40
VDD (V)	1.2	1.8	1.8	1.0	0.9	0.9
VDDIO (V)	2.5	1.8	0.9 / 1.8 / 3.3	2 / 3	0.9 / 1.8	0.9 / 1.8
Detection corners	3 (TT FF SS)	3 (TT FF SS)	5	N/A	5	5 (TT FF SS FS SF)
Detection cycles	1 cycle	1 cycle	Tens of cycles	No PVT	3 cycles	1 cycle
Data rate (MHz)	125	500	75 / 95 / 120	100 / 133	500 / 460	725 / 710
Slew rate (V/ns)	2.2-3.4	2.1-3.58	1.28-2.79	N/A	N/A	1.45-2.14
ΔSR (V/ns)	1.2	1.48	1.51	N/A	N/A	0.69
ΔSR Reduction (%)	37.5	N/A	N/A	N/A	N/A	20.8 / 54.9
Leakage Current Reduction (%)	N/A	N/A	N/A	N/A	N/A	41.0 / 37.5
Power dissipation (mW)	N/A	13.7 @(500 MHz)	0.427 @(120 MHz)	N/A	N/A	19.53 @(725 MHz)(Worst case)
Area (mm^2)	N/A	0.009	0.0104	0.0105	0.0132	0.0111

Table IV shows the comparison with prior works. Ker and Chen [7] demonstrated the HV tolerant technique for 3 $\times$ VDD without any compensation at all. The previous design in [16] improved the ΔSR in only three process corners. Although Wang *et al.* [18], [19] possessed five-corner compensation, the ΔSR and leakage current compensation were not considered. Another previous work [17] compensates the ΔSR with the improvement of 37.5% in only three corners. Our design compensates the ΔSR with 23.4% improvement in five process corners in the worst case, and the ΔSR is only 0.69 V/ns. Besides, the dynamic leakage current is reduced by 41.0% and 37.5%. Moreover, the data rate of our design is 725 and 710 MHz for 0.9 and 1.8 V modes, respectively. Therefore, for any work highlighted in Table IV and the summary mentioned earlier, 0.8% average power saving, 41% and 37.5% leakage reduction, and 20.8% (worst case) ΔSR improvement with only 8.36% area overhead, our design demonstrates comprehensive compensation and outstanding performance.

IV. CONCLUSION

In this proposed design, the 2 $\times$ VDD output buffer with dynamic leakage and SR variation compensation is fabricated and realized with the TSMC 40-nm CMOS process. The dual PVT variation detectors detect the PVT variation for pMOS and nMOS separately, such that it could compensate the ΔSR with at least 23.4% in five corners. The leakage reduction circuit has properly shut down the auxiliary current paths when the digital signal has been transmitted. It reduces the dynamic leakage current by 41.0%. Besides, the maximum data rate of VPAD is up to 725 MHz.

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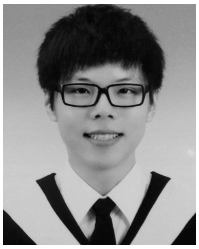

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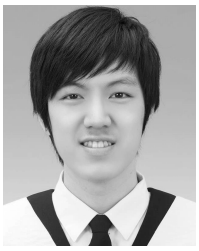

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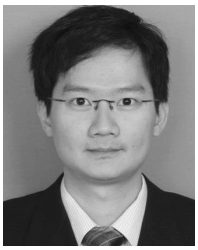

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