2 × VDD 40-nm CMOS Output Buffer With Slew Rate Self-Adjustment Using Leakage Compensation

Chua-Chin Wang, *Senior Member, IEEE*, Zong-You Hou, and Kai-Wei Ruan

***Abstract*—A 2 × VDD output buffer for 40-nm complementary metal–oxide–semiconductor technology nodes is proposed in this investigation featured with a slew rate (SR) auto-adjusted by process, voltage, temperature, and leakage (PVTL) detection and, particularly, the leakage compensation mechanism. The output driving current is boosted by turning on extra charging paths and discharging paths when the SR is detected to be dropping. With the proposed PVTL detection and leakage compensation circuit, the SR is improved with 11.0% and 67.4% by on-silicon measurement results given different VDDIO values (1.8/0.9 V) and temperatures (from 0 °C to 100 °C), respectively. The data rate is 250/500 MHz for VDDIO at 1.8/0.9 V, respectively.**

***Index Terms*—Auto-adjustment, mixed-voltage, output buffer, process, voltage, temperature, and leakage (PVTL) compensation, slew rate (SR).**

I. Introduction

As complementary metal-oxide-semiconductor (CMOS) technology evolves toward deep nanoscale nodes, e.g., 65 nm or even 40 nm, the impact resulting from variations in process (P), supply voltage (V), temperature (T), and, even worse, leakage (L) has become the major problem of digital output buffers of the chips fabricated using these advanced technologies. Another practical issue regarding the system integration comprising chips fabricated by different generations of CMOS technologies is the digital level conversion there between. To reduce the number of level converters as well as the size of the printed circuit board, mixed-voltage buffers become required to translate digital signals from different chips with different supply voltages. Although many researchers have noticed the demand of mixed-voltage output buffers and proposed various solutions to resolve the slew rate (SR) deterioration problems caused by PVT variations, the leakage, in fact, will be the foe to beat in the deep nanoscale CMOS technology nodes [1]. For instance, many prior reports highlight the effect caused by PVT variations upon the output digital signal quality, e.g., [5] and [11]; however, most of them ignored the impact brought about by leakage.

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More specifically, Kwak *et al.* proposed a delay-detection-based approach to assess PVT variation, in which a massive amount of logic gates are needed to realize this approach [5]. Chen *et al.* further proposed a dual-way approach to respectively assess the process corners of PMOS and NMOS transistors such that all five corners (SS, SF, TT, FS, and FF) are fully differentiated [11]. Then, the SR is adjusted correspondingly based on the detected corners. The major problem of this method is that the bias voltages for those comparators are vulnerable to power supply noise and drifting. The consequence is that the accuracy of the corner detection is doubtful in some cases. Most important of all, the leakage issue was never explored. Apart from the above two prior works, the SR was also reported to be self-adjusted using various phase-locked-loop-based [2], delay-locked-loop-based [3], and speed-locked-loop-based [4] schemes and PVT [6] compensation schemes for standard digital output buffers to meet different standards, e.g., LPDDR2 (1.0–2.5 V/ns), PCI-X 133 (1–4 V/ns), and DDR4 (4–9 V/ns). However, these compensation circuits cannot be directly applied to 2 × VDD mixed-voltage output buffers. The PVT compensation for the SR improvement of 2 × VDD output buffers has not drawn too much attention until two recent reports, namely, [7] and [8]. Nevertheless, these works did not consider the leakage issue either. The leakage current, in particular, is a severe problem in the nanoscale CMOS process [10].

Although we have shown process, voltage, temperature, and leakage (PVTL) compensation design for 2 × VDD output buffer in [16], only simulation results were demonstrated therein. By contrast, in this brief, this investigation proposes the leakage current compensation apart from PVT corner detection and compensation circuitry for the SR of the 2 × VDD output buffer to achieve the SR improvement of 11.0%–67.4% in two VDDIO cases and five temperature corners. The maximum data rate is 250/500 MHz for VDDIO at 1.8/0.9 V, respectively.

II. 2 × VDD Output Buffer With Leakage Compensation

Fig. 1 shows the block diagram of the proposed 2 × VDD output buffer, which is composed of the PVT detector, the digital logic circuit, the leakage compensation circuit, and the 2 × VDD output stage.

A. PVT Detector

Since PVT variations have been known to throw significant impact on delay [12], a detector as shown in Fig. 2 is used to tell where the PVT corner is. The PVT detector is composed of

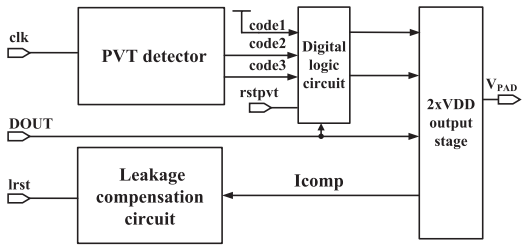

Fig. 1. Proposed 2 × VDD output buffer with leakage compensation.

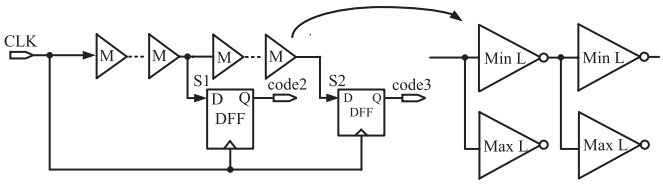

Fig. 2. PVT detector.

a logic gate string, where each delay unit, i.e., M, is composed of two cascaded inverters, as shown on the right side of Fig. 2. Min L stands for the length of the PMOS and NMOS of the inverter that is the minimum allowed by the selected CMOS process. This inverter has the smallest delay and will be affected by PVT variation most seriously. By contrast, the Max L inverter has the largest length for PMOS and NMOS therein such that the delay will be least affected by PVT variation. Node S1 is in the middle of the gate delay string, whereas node S2 is at the end. Two delay flip-flops latch the signal of these two nodes, respectively, to generate code2 and code3.

Referring to the mathematical analysis of Yuan and Bi [17], assume that the input load of the Max L inverter is $C_{\mathrm{Max\,L}}$ at any PVT corner, i.e.,

$$\mathrm{SR} = \frac{I_M}{C_{\mathrm{Max\,L}}} = \frac{0.8 \times \mathrm{VDD}}{T_{\mathrm{SR}}} \tag{1}$$

where SR is the SR of the delay unit, I_M is the current of the delay unit, and T_{SR} is the rise time or fall time. Equation (1) is reorganized as

$$T_{\mathrm{SR}} = \frac{C_{\mathrm{Max\,L}} \times 0.8 \times \mathrm{VDD}}{I_M}. \tag{2}$$

Assuming that α is a variation parameter of the current at different PVT corners, $T_{\mathrm{SR}} \propto 1/\alpha I_M$ is attained from (2). Therefore, an increase of I_M results in the drop of T_{SR}, and *vice versa*. Referring to Fig. 3, a PVT corner can be classified into three categories (fast, typical, and slow) in accordance with T_{SR}. The three categories are denoted by the output of the PVT detector (e.g., 001, 011, and 111 denoted by code3, code2, and code1).

B. Digital Logic Circuit

In fact, the digital logic circuit in Fig. 1 is a control signal generator or encoder. It receives code2 and code3 from the PVT detector, code1 from VDD, rstpvt (reset), DOUT (data to be transmitted) to generate the corresponding control signals, where P_{PATHA}, P_{PATHB}, and P_{PATHC} are coupled to the following level converter (which will be shown in Fig. 6), and V_{g4}, V_{g5}, V_{g6}, directly drive M_{N301}, M_{N302}, M_{N303}, respectively (which will be shown in Fig. 6). The schematic of digital logic signal is given in Fig. 4.

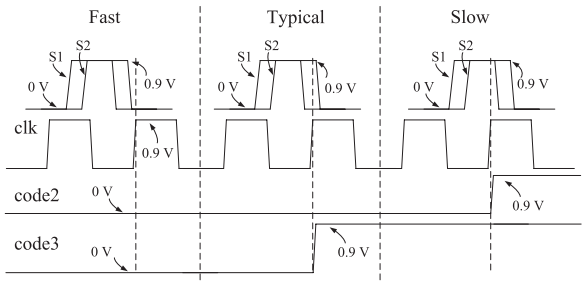

Fig. 3. Output waveform illustration of the PVT detector.

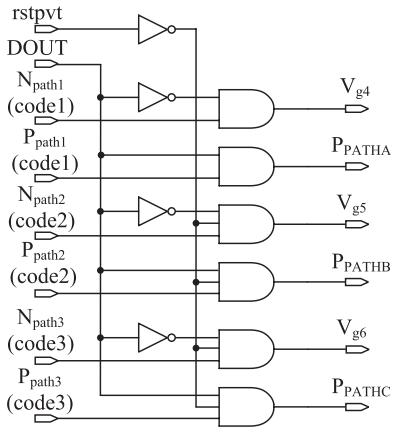

Fig. 4. Digital logic circuit.

C. Leakage Analysis

Referring to Fig. 5, the gate leakage current is given as

$$I_G = I_{\mathrm{GC}} + I_{\mathrm{GB}} + I_{\mathrm{GDO}} + I_{\mathrm{GSO}} \tag{3}$$

where I_{GDO} and I_{GSO} are the parasitic leakage currents through the drain and source overlap regions, respectively. I_{GB} is the leakage current through the gate to the substrate. I_{GC} is the gate-to-channel tunneling current, which is resulted from the electron conduction band and the hole valence band tunneling mechanism for NMOS and PMOS, respectively. I_{GC} is composed of two components: I_{GCD}, which is from the gate to the drain, and I_{GCS}, which flows into the source. I_{GC} is given by

$$I_{\mathrm{GC}} = \frac{J_{G0} W L \left(1 - e^{B^* K L}\right)}{B^* K L} \tag{4}$$

where J_{G0} is the gate tunneling leakage current density. K is a parameter dependent on the terminal voltages and the threshold voltage [10]. B^* is a parameter associated with the process and the oxide voltage. Equation (4) reveals that I_{GC} is proportional to the width of the MOS transistor. Thus, I_{GC} is the dominant leakage current component for the MOSFETs in the output stage because these transistors are very wide to deliver large output currents.

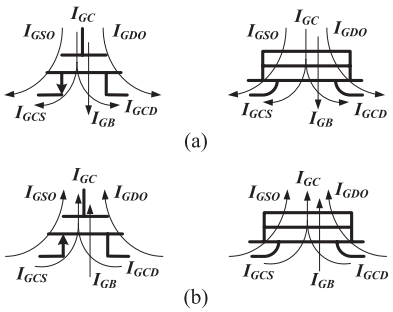

Fig. 5. Gate leakage current components in (a) NMOS and (b) PMOS.

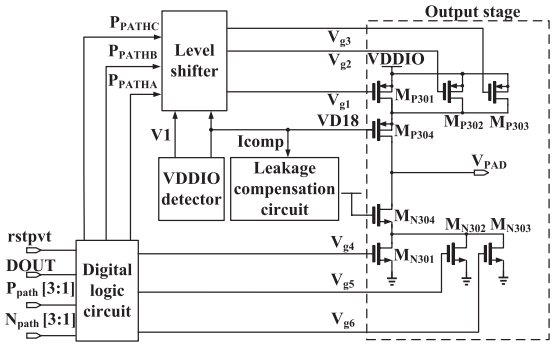

Fig. 6. $2 \times$ VDD output stage.

The leakage current results in the unstable gate bias voltages at the output stage of the $2 \times$ VDD output buffer, which, in turn, results in poor SR. What is even worse is that it causes the reliability problem due to the gate oxide overstress and hot carrier degradation if the voltage differences across the terminals of the transistors are larger than the tolerant voltage required by the foundry.

D. Leakage Analysis Compensation

Notably, the $2 \times$ VDD output stage in Fig. 1 is coupled to a leakage compensation circuit, in which a current signal $I_{\rm comp}$ is the signal to be detected. Meanwhile, the gate drive of M_{P304} in Fig. 6, i.e., VD18, is noise prone and variation prone, because it is generated from the VDDIO generator that is used to estimate the voltage on the pad. Apparently, M_{P304} is more sensitive to external noise relative to the other transistors in the $2 \times$ VDD output stage. That is, every transistor in the $2 \times$ VDD output stage except M_{P304} is driven by a voltage drive internally from the V_{g1} generator, digital logic circuit, or VDD. Therefore, a leakage compensation mechanism is needed to stabilize the gate drive of M_{P304}.

The leakage compensation circuit in Fig. 6 is disclosed in Fig. 7, comprising two subcircuits, a voltage-controlled current source, and a leakage current detector. The individual functionality of these subcircuits is given as follows.

Leakage Current Detector: Assuming that $I_{\rm leak}$ is the gate leakage current of M_{P304}, the voltage variation $(V_{\rm leak})$ of the gate drive of M_{P304} caused by leakage current can be written as

$$V_{\rm leak} = I_{\rm leak} \times R_{\rm in} \tag{5}$$

where $R_{\rm in}$ is the input resistance of M_{P304}.

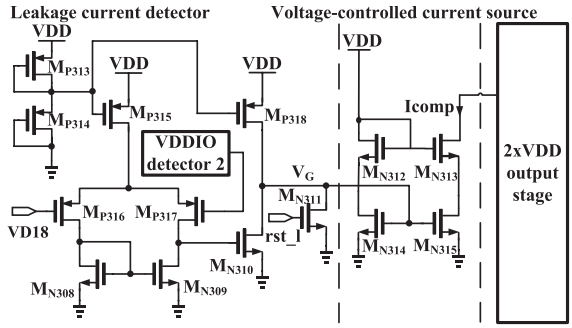

Fig. 7. Leakage compensation circuit.

A replica of the VDDIO detector is used as a reliable bias, which is deemed as the standard VD18, in the leakage current detector. $V_{\rm leak}$ is also the voltage difference between VDD18 and the output of VDDIO detector 2. Thus, we carry out a small-signal analysis of the leakage current detector. The output drain voltage of M_{N310}, i.e., V_G, is derived as

$$V_G = A_{\rm OL} \times V_{\rm leak} \tag{6}$$

where $A_{\rm OL}$ is the open-loop gain of the leakage current detector.

If VD18 is higher than the output of VDDIO detector 2, V_G is pulled up to raise the drain currents in the current mirror, i.e., M_{N312} and M_{N313}. Notably, the drain current of M_{N313} is $I_{\rm comp}$. When VD18 is lower than the output of VDDIO detector 2, the entire operation is opposite.

Voltage-Controlled Current Source: Referring to Fig. 7, $I_{\rm comp}$ is the signal coupled to the gate drive of M_{P304}. It is also the drain current of M_{N313}, which is the mirror of M_{N312}. As addressed in the previous paragraph, the magnitude of the drain current is determined by the drain current through the foot transistors, i.e., M_{N314} and M_{N315}. That is, according to (5) and (6), $I_{\rm comp}$ can be written as

$$I_{\rm comp} = A_{\rm OL} \times I_{\rm leak} R_{\rm in} \times gm_{N313} \tag{7}$$

where $gm_{N313} = \mu_n C_{ox}(W/L)(V_{GS,N313} - V_{th})$.

Therefore, $I_{\rm comp}$ will be able to stabilize VD18 by adjusting W/L and $A_{\rm OL}$ according to (7).

E. $2 \times$ VDD Output Stage

Referring to Fig. 6 again, M_{P304} is driven by the VDDIO detector, and M_{N304} is driven by VDD. M_{P301}, M_{P302}, and M_{P303} are driven by V_{g1}, V_{g2}, and V_{g3}, respectively, where V_{g1}, V_{g2}, and V_{g3} are generated by the level shifter. By contrast, the corresponding discharging current paths M_{N301}, M_{N302}, and M_{N303} are driven by V_{g4}, V_{g5}, and V_{g6}, respectively. As addressed earlier, V_{g4}, V_{g5}, and V_{g6} are generated by the digital logic circuit. The details of the VDDIO detector and the level shifter are given in the following text.

VDDIO Detector: Referring to Fig. 8, the major function of the VDDIO detector is to generate VD18 driving M_{P304} as shown in Fig. 6 such that the overstress problem is prevented when the output stage is transmitting or receiving $2 \times$ VDD pulses. In addition, an extra voltage reference, namely, V1, is generated as well, which is coupled to the level shifter for the purpose of providing appropriate gate drives to M_{P301},

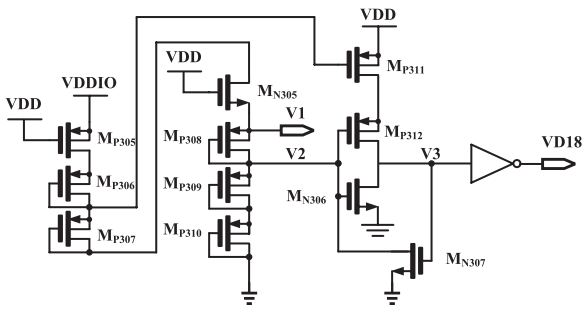

Fig. 8. VDDIO detector.

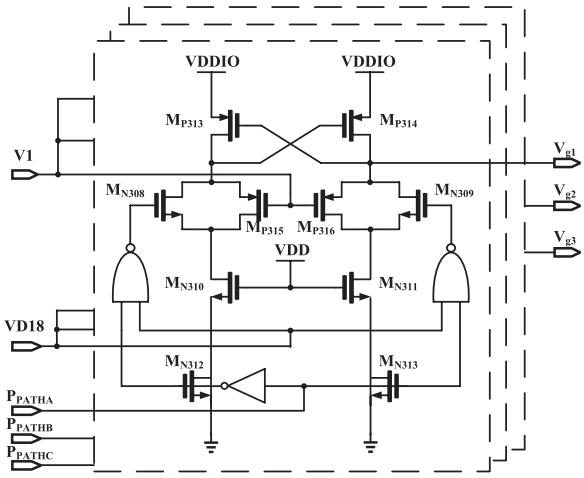

Fig. 9. Level shifter.

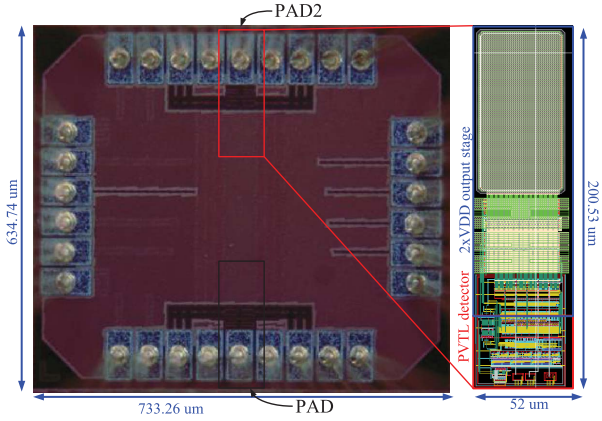

Fig. 10. Die photo and layout of the proposed output buffer.

M_{P302}, and M_{P303}. The scenarios within the VDDIO detector are summarized as follows.

(1) If VDDIO $= 1.8$ V, M_{P305} is on to close M_{P311}. V2 is kept around twice of V_{thp}, and M_{P306} is on such that V3 is pulled down to ground so as to pull up VD18 $= 0.9$ V.

(2) When VDDIO becomes 0.9 V, M_{P305} is off to turn on M_{P311} and M_{P312}. Then, V2 is kept around 2.0 V to charge V3 up to 0.9 V such that M_{N307} is on to ensure V2 is grounded. Since V3 is 0.9 V, VD18 will be pulled down to 0 V.

Level Shifter: Apparently, the signals generated by the digital logic circuit, i.e., P_{PATHA}, P_{PATHB}, and P_{PATHC}, cannot be

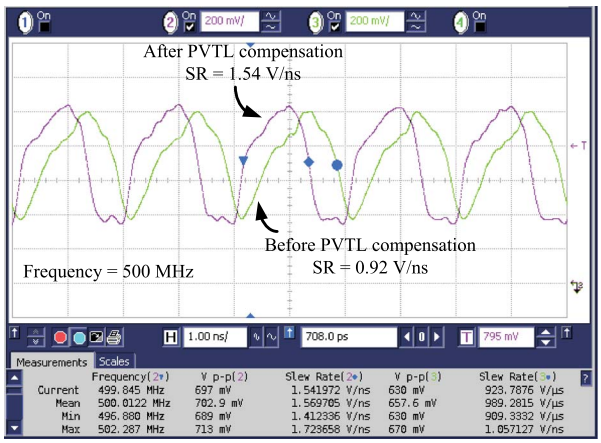

Fig. 11. 500-MHz output waveform at V_{PAD} given VDDIO $= 0.9$ V.

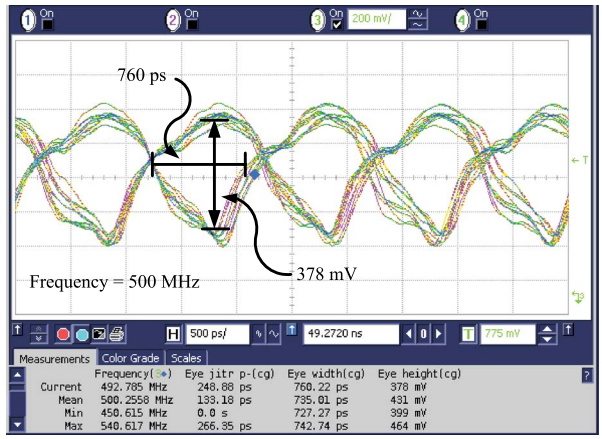

Fig. 12. 500-MHz eye diagram at V_{PAD} given VDDIO $= 0.9$ V (with compensation).

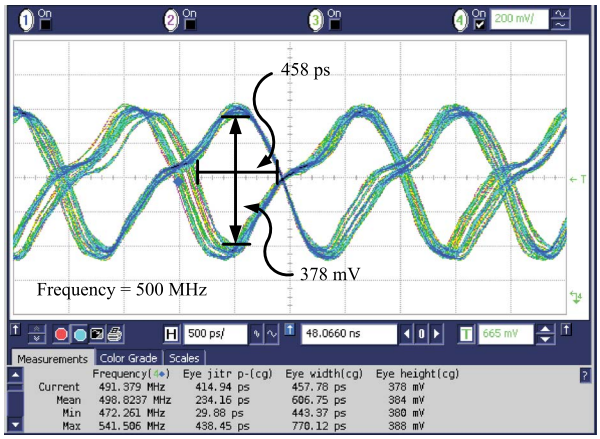

Fig. 13. 500-MHz eye diagram at V_{PAD} given VDDIO $= 0.9$ V (without compensation).

the correct gate drives of M_{P301}, M_{P302}, and M_{P303}, respectively, if the voltage level is not properly converted. The function of the level shifter is meant to provide such voltage level conversion. Referring to Fig. 9, it consists of three identical subcircuits that convert the voltage level of P_{PATHA}, P_{PATHB},

TABLE I
COMPARISON WITH SEVERAL RECENT WORKS

	This work	[9]	[7]	[13]	[5]	[14]	[15]
Year	2015	2013	2013	2014	2007	2011	2012
Publication		MEJ	TCAS-I	EDSSC	ISSCC	ISVLSI	ISOCC
Process	40 nm	40 nm	90 nm	90 nm	0.18 μm	90 nm	65 nm
Result	Measured	Measured	Measured	Simulation	Measured	Simulation	Simulation
VDD (V)	0.9	0.9	1.2	1.0	1.8	1.2	1
VDDIO (V)	1.8/0.9	1.8/0.9	2.5/1.2	1.8/1.0	3.3/1.8	1.2	1
Data rate (MHz)	250/500	460/500	125	300/500	120	83.3	10 Gbps
SR improvement	67.4%	8%	36%	27%	5%	-61.3%	21.2%
Power (mW)	27 mW@ 500 MHz	2.2 mW@ 330 MHz	N/A	21 mW@ 500 MHz	13.7 mW@ 500 MHz	10.92 mW@ 83.3 MHz	6.05 mW@ 10Gbps
Compensation	PVTL	PVT	PVT	PVTL	PVT	overshoot	PVT
Area (mm^2)	0.01	0.026	N/A	0.025	0.009	N/A	N/A
FOM‡	0.13	0.56	N/A	0.1	0.21	0.026	0.57

Note: ‡: FOM = Averasge SR/Power

and P_{PATHC}, respectively. Take P_{PATHA} as an example, the scenarios are summarized as follows.

- VDDIO $= 0.9$ V: If P_{PATHA} is 0.9 V, V_{g1} is the same as VDDIO, i.e., 0.9 V. By contrast, if P_{PATHA} is 0 V, then V_{g1} becomes 1.8 V.
- VDDIO $= 1.8$ V: Similarly, if P_{PATHA} is 0.9 V, V_{g1} is the same as VDDIO, i.e., 0.9 V. However, if P_{PATHA} is 0 V, then V_{g1} becomes 0.9 V.

III. IMPLEMENTATION AND MEASUREMENT

The proposed $2 \times$ VDD output buffer is implemented using a Taiwan Semiconductor Manufacturing Company 45-nm CMOS LOGIC General Purpose Superb (40 G) ELK Cu 1P 10 M 0.9/2.5-V process. Fig. 10 shows the die photo of the proposed output buffer, in which the layout of one signal output buffer is also disclosed. The area of the entire chip is $733.26 \times 637.74\ \mu\mathrm{m}^2$, and the active area of one single buffer is $200.53 \times 52.00\ \mu\mathrm{m}^2$. Notably, a total of two output buffers is fabricated on the same die, in which PAD is the buffer with enabled PVTL compensation, whereas PAD2 is that without compensation. Thus, the effect of the proposed PVTL compensation design will be faithfully demonstrated.

Referring to Fig. 11, the SR is raised from 0.92 V/ns (without compensation) to 1.54 V/ns (with compensation), which is a 67.4% improvement. Moreover, comparing Fig. 12 with Fig. 13, the eye is widened from 458 ps $\times$ 378 mV (without compensation) to 760 ps $\times$ 378 mV (with compensation), which is a 66% enhancement.

Table I tabulates the performance comparison between this work and several recent mixed-voltage I/O designs. Apparently, the proposed $2 \times$ VDD output buffer attains the best SR improvement at the maximum date rate (500 MHz). Moreover, the proposed buffer is also the first 40-nm buffer with PVTL compensation.

IV. CONCLUSION

This investigation has demonstrated the PVTL detection and SR compensation on silicon. Particularly, it is applied to the advanced 40-nm CMOS process, which has been bothered by severe leakage problems. The physical measurement of two buffers, one with PVTL compensation and the other without, justifies the functionality and outstanding performance of the proposed design. The proposed design will be easily migrated to deeper nanoscale CMOS processes, e.g., 28 nm.

ACKNOWLEDGMENT

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