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A 19.38 dBm OIP3 gm-boosted up-conversion CMOS mixer for 5–6 GHz application

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ABSTRACT

A highly linear up-conversion mixer for 5–6 GHz wireless local area network (WLAN) applications implemented using TSMC 0.18-μm standard complementary metal oxide semiconductor (CMOS) technology is presented. The feature of the proposed mixer is based on the double-balanced Gilbert cell with current-reused technique to enhance the third-order input intercept point (IIP3). Moreover, local oscillator (LO) body grounded and gm-boosting techniques are also integrated to boost the power conversion gain (CG). The proposed up-conversion mixer demonstrates a maximum CG of 7.21 dB, a maximum IIP3 of 13.17 dBm, an output third-order input intercept point (OIP3) of 19.38 dBm, and a DC power consumption of 4 mW on silicon given a 1.1 V supply voltage. The overall chip area including radio frequency (RF) pads is 1×0.85 mm^2, where the active area is merely 0.7×0.37 mm^2.

1. Introduction

The wireless multimedia services have become part of our daily lives, and in this respect, IEEE 802.11a/b/g/n wireless local area network (WLAN) standards are indispensable [1,2]. However, to keep pace with the rapid development of the information technology (IT), new communication systems/devices, such as smart phones, pads, cameras and even TVs, demand more reliable wireless links as well as higher data rate. Consequently, there is a requirement of coping capability for devices and standards with next-generation wireless communication systems [3]. Federal Communications Commission (FCC) announced a new protocol of IEEE 802.11ac WLAN standard for higher data rate of wireless communication systems. That is, if the data rate higher than 1000 Mbps, 160 MHz channel bandwidth from 5 GHz to 6 GHz is the one to be utilized [4].

To meet such high data rates, a highly linear mixer should be included in next-generation wireless communication systems, since the linearity has significant impact on the total linearity of a radio frequency (RF) front-end. Therefore, it is worthwhile investigating superior techniques for highly linear mixers. In general, third-order input intercept point (IIP3) and output intercept point (OIP3) are two important features to demonstrate the linearity of the CMOS RF front-end. Several techniques have been reported to enhance the IIP3 of RF mixer [5–12], which are all very sensitive to gate bias variations. Multiple gated transistors (MGTR) technique had been implemented by adopting two MOSFETs, where the overdrive voltage of each transistor is chosen to compensate for the nonlinear characteristics of the main transistor [5,6]. Derivative superposition (DS) using a negative gm in saturated pseudo-differential transistor (PDT) is compensated by the positive value of PDT in subthreshold region [7,8]. Passive mixers without consuming power consumption can achieve high linearity, since the level of undesired intermodulation products of these mixers is weaker than their active counterparts. However, they are suffered from conversion loss, poor isolation, and may require more amplifiers in upstream stages [9,10]. The third-order intermodulation distortion (IMD3) cancellation method realized that a common-source amplifier generates IMD3 signals with 180 phase difference against the IMD3 of the cascode main amplifier IMD canceller [11], and utilized negative impedances to simultaneously cancel flicker noise and IM3 in Gilbert-type mixers [12]. To eliminate the derivative nonlinearity, the previous studies utilized auxiliary transistors or circuits to drive the derivative coefficient close to zero. Although linearity could be improved through these approaches, extra transistors or circuit pay the price of high design complexity and more power dissipation. Furthermore, not only the linearity, but power conversion gain (CG) should also be taken into account with CMOS active mixers to alleviate the design margin of the following stages.

In this work, a wideband up-conversion mixer with high linearity and moderate power CG has been proposed, where gm-boosting, current-reused features are integrated. A prototype implemented using 0.18-μm CMOS process is demonstrated to meet the requirements of IEEE 802.11ac WLAN standard.

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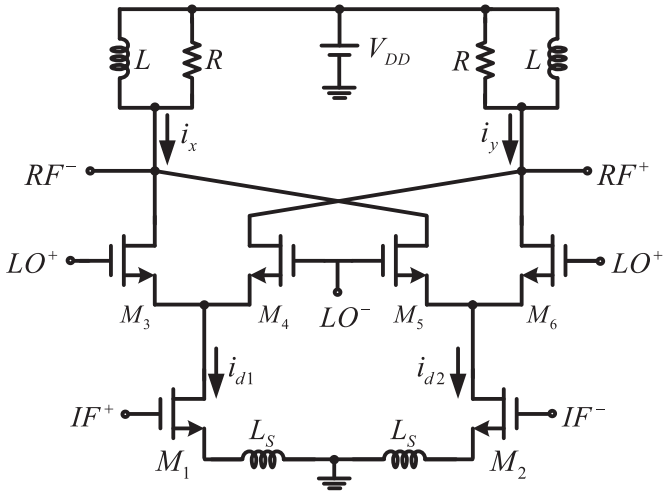

Fig. 1. Schematic diagram of the conventional up-conversion mixer [13].

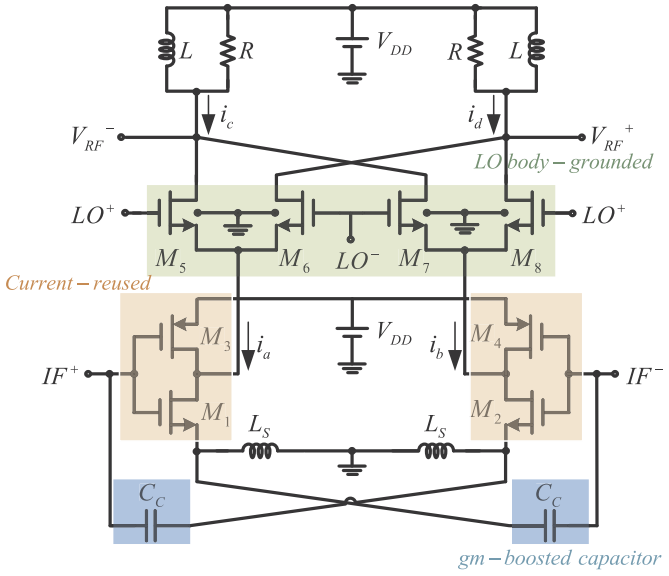

Fig. 2. Schematic diagram of the proposed up-conversion mixer.

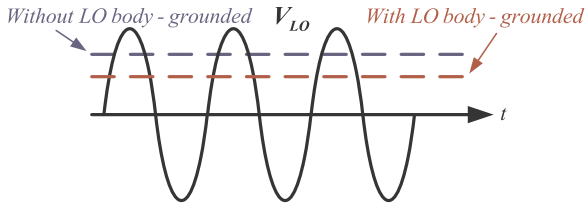

Fig. 3. Signal waveform diagram of the conventional CMOS switch.

2. Up-conversion mixer with high linearity

Many recent up-conversion mixers use the conventional double-balanced Gilbert-cell up-conversion mixer architecture [13] as shown in Fig. 1. The differential pair M_1–M_2 with degenerative inductance acts an IF transconductance stage. M_3–M_6 consist of the LO switching pair. Two modified output loads for high frequency are used to flatten the CG. The differential IF currents shown in Fig. 1, namely i_{d1} and i_{d2} in the S-domain, are expressed as follows:

$$i_{d1}(S) = -i_{d2}(S) = \frac{V_{IF}(S)}{2} \frac{g_{m1,2}}{1 + g_{m1,2} S L_S} \tag{1}$$

where g_{m1} and g_{m2} are the transconductance of NMOS transistor pair M_1 and M_2, respectively, S is equal to $j\omega$, and $V_{IF}(S)$ is the input signal, namely $V_{IF}\cos(j\omega_{IF}t)$. The differential output current of the conventional up-conversion mixer in time-domain can be attained by the following equation:

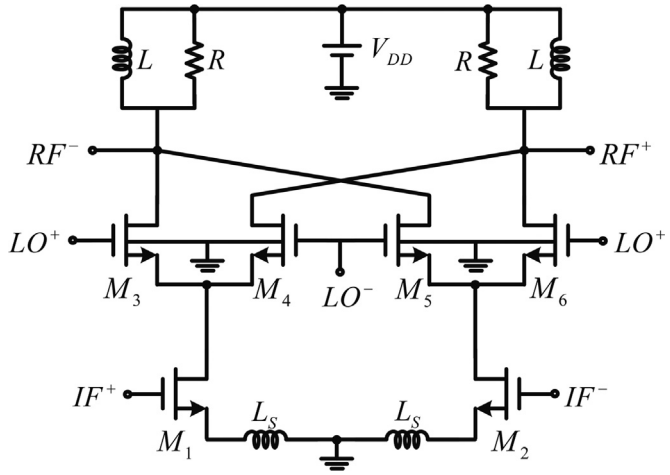

Fig. 4. Schematic of the conventional up-conversion mixer with LO body-grounded structure.

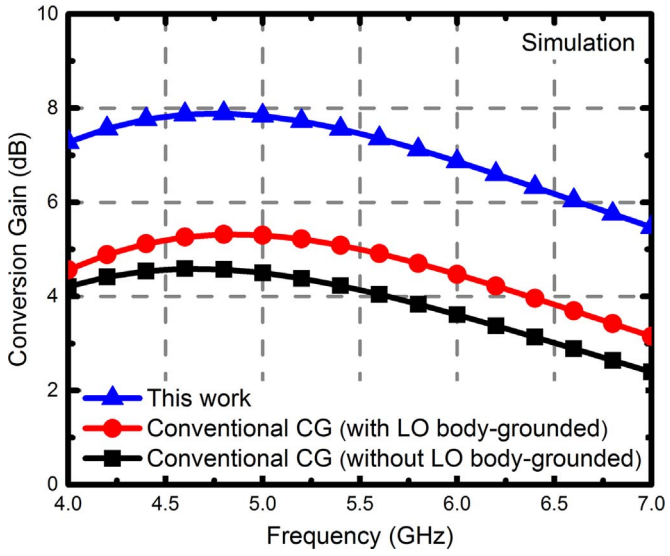

Fig. 5. Simulated CG comparison with conventional up-conversion mixer.

Table 1
Main parameters for conventional up-conversion mixer.

Mixer types	W/L (μm) (M_1/M_2)	W/L (μm) (M_3–M_6)	R (Ω)	L (nH)	L_S (nH)	V_{DD} (V)
Conventional Conventional (with LO body-grounded)	90/0.18	20/0.18	500	10	0.57	1.2

Table 2
Main parameters for the proposed up-conversion mixer.

Mixer types	W/L (μm) (M_1/M_2)	W/L (μm) (M_3–M_4)	W/L (μm) (M_5–M_8)	R (Ω)	L (nH)	L_S (nH)	V_{DD} (V)
This work	90/0.18	120/0.18	20/0.18	500	10	0.57	1.2

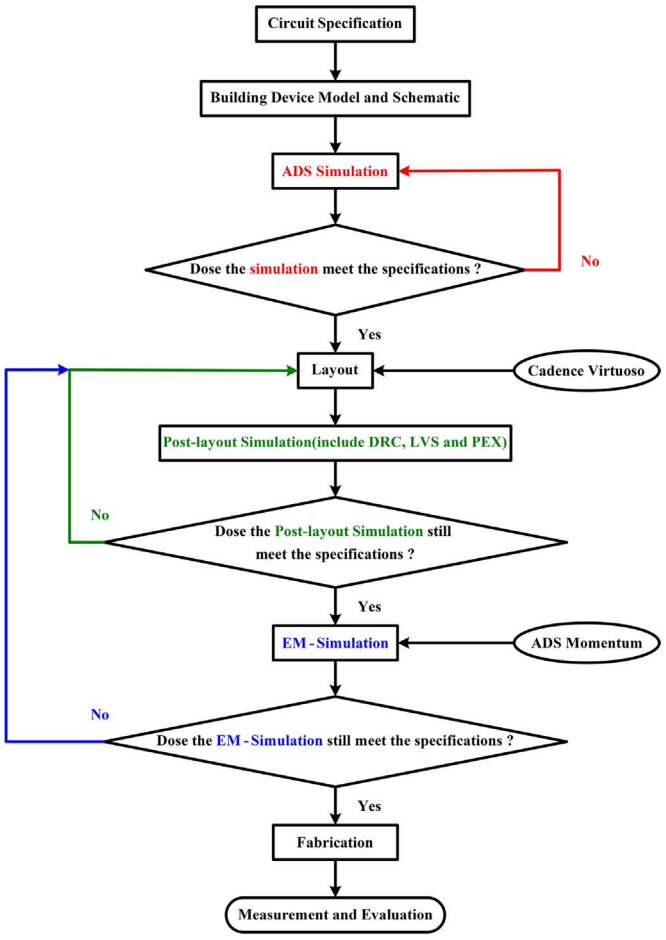

Fig. 6. Design flow of the proposed up-conversion mixer.

$$i_{out}(t) = i_x(t) - i_y(t) = \frac{g_{m1,2}}{\sqrt{1 + (g_{m1,2}\omega L_S)^2}} V_{IF}\cos(\omega_{IF}t - \theta)\cdot sq[\cos(\omega_{LO}t)] \tag{2}$$

where $\theta = \tan^{-1} g_{m1,2}\omega L_S$ and $sq[\cos(\omega_{LO}t)]$ is a square waveform denoting the LO signal of which expansion is given as follows:

$$sq[\cos(\omega_{LO}t)] = \frac{4}{\pi}\cos(\omega_{LO}t) - \frac{4}{3\pi}\cos 3(\omega_{LO}t) + \cdots \tag{3}$$

By substituting Eq. (3) into Eq. (2) and neglecting high order terms, the RF output current at $\omega_{IF} + \omega_{LO}$ can be attained as follows:

$$i_{out}(t) \approx \frac{2}{\pi}\frac{g_{m1,2}}{\sqrt{1 + (g_{m1,2}\omega L_S)^2}} V_{IF}\cos[(\omega_{IF} + \omega_{LO})t - \theta] \tag{4}$$

Thus, the up-conversion mixer output signal is simplified as follows:

$$V_{RF}(t) = \frac{2}{\pi}\frac{g_{m1,2}}{\sqrt{1 + (g_{m1,2}\omega L_S)^2}}\cdot\frac{\omega L}{\sqrt{1 + (\omega L/R)^2}} V_{IF}\cos[(\omega_{RF})t + \phi - \theta] \tag{5}$$

where $\phi = 90° - \tan^{-1}(\omega L/R)$, ω_{RF} is the sum of ω_{IF} and ω_{LO}, and the conversion gain is derived:

$$CG = \frac{2}{\pi}\frac{g_{m1,2}}{\sqrt{1 + (g_{m1,2}\omega L_S)^2}}\cdot\frac{\omega L}{\sqrt{1 + (\omega L/R)^2}} \tag{6}$$

By contrast, the schematic of the proposed high-linearity up-conversion mixer is shown in Fig. 2. To relax the design of the demodulation circuit, the intermediate frequency (IF) is set to 10 MHz. Besides, the frequency of local oscillator (LO) and RF are selected between 4.99–5.99 GHz and 5–6 GHz, respectively. To enhance the linearity, power CG and bandwidth, an IF transconductance stage (M_1–M_4) with gm-boosting and current-reused designs, a LO switch stage (M_5–M_8) with LO body-grounded structure and an output stage with parallel RL load are adopted in this research.

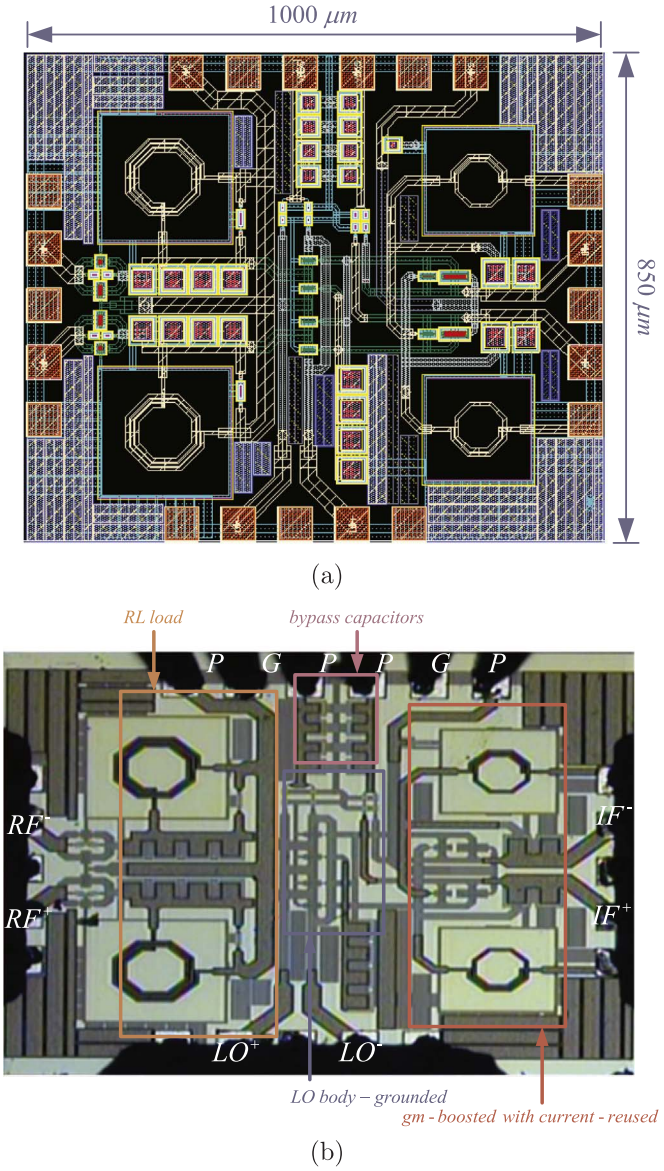

Fig. 7. (a) Layout and (b) die photo of the proposed up-conversion mixer.

The IF transconductance stage converts the input signal into a current signal, which will be further mixed with the LO signal in the switching stage. In this research, the gm-boosted technique is firstly adopted for effectively improving the transconductance, linearity and power CG of RF up-conversion mixer. Two cross-coupled capacitors (C_C) and NMOS transistor pair (M_1–M_2) consist of this gm-boosted circuit, where the source terminal of one transistor is coupled to the gate terminal of the other transistor through one cross-coupled capacitor. In addition, a current-reused technique (M_1/M_3 and M_2/M_4 pairs) is also employed for further enhancing the linearity. The two inductors (L_S) are used to avoid the signal coupled through the ground while adopting gm-boosted technique.

In the LO switch stage, an LO body-grounded technique (M_5–M_8) is included to raise the power CG. A signal waveform diagram of the conventional CMOS switch (with and without LO body-grounded) is shown in Fig. 3 [14]. The switch is turned on as the bias voltage is higher than the overdrive voltage (V_{OV}) such that CMOS is operated in

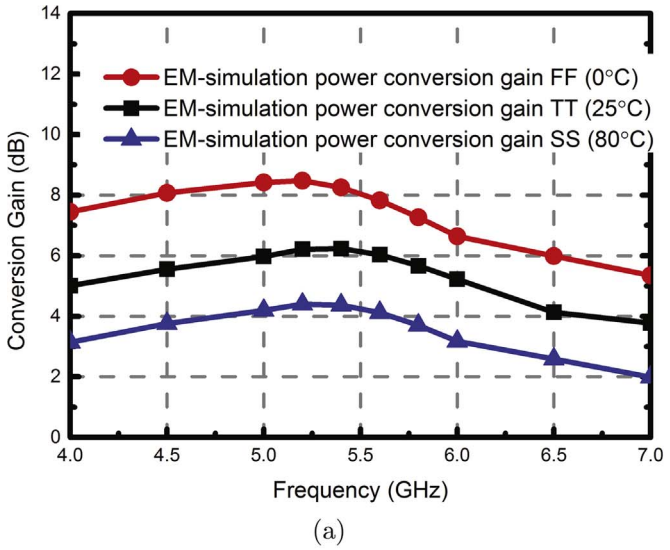

Fig. 8. EM simulated (a) CG and (b) IIP3 of the proposed mixer at different PVT corners.

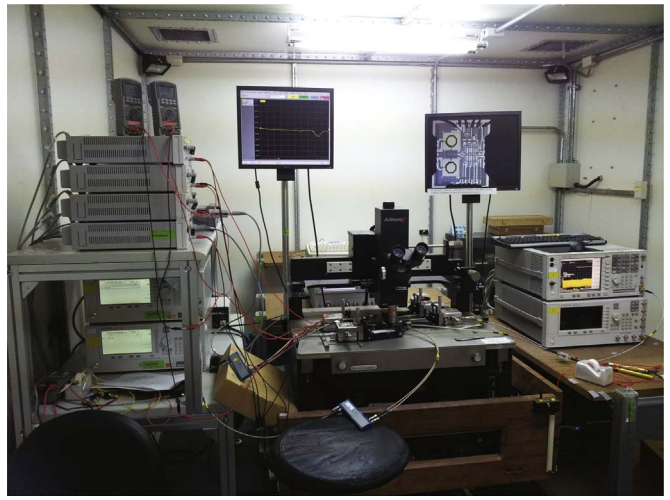

Fig. 9. RF characteristics measurement environment.

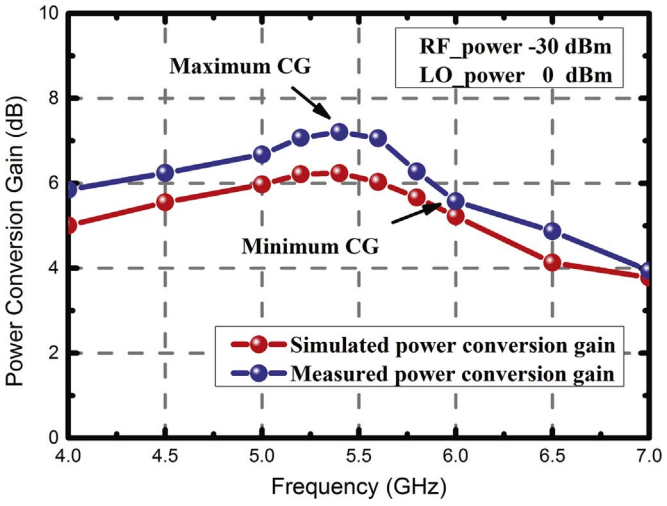

Fig. 10. Simulated and measured conversion gain ranging from 4 to 7 GHz.

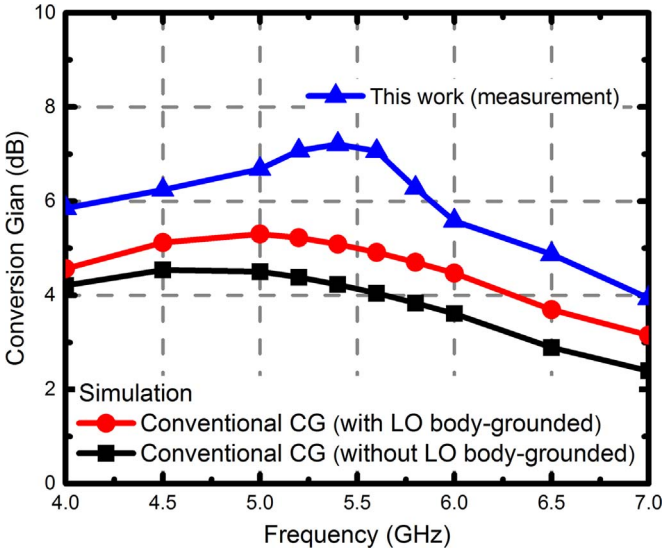

Fig. 11. Measured CG comparison with conventional up-conversion mixer.

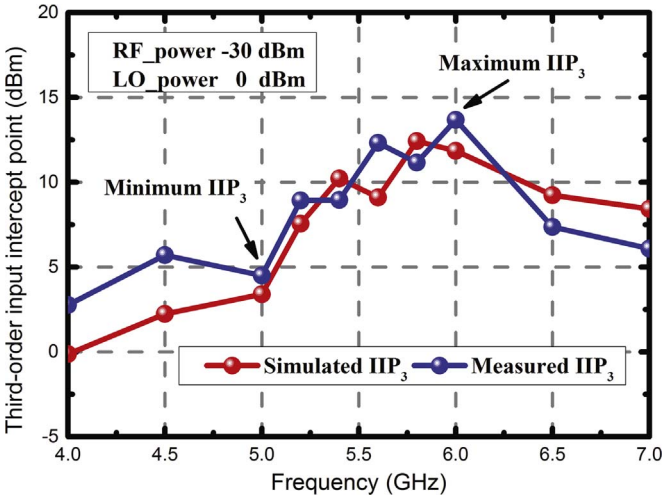

Fig. 12. Simulated and measured IIP3 versus frequency.

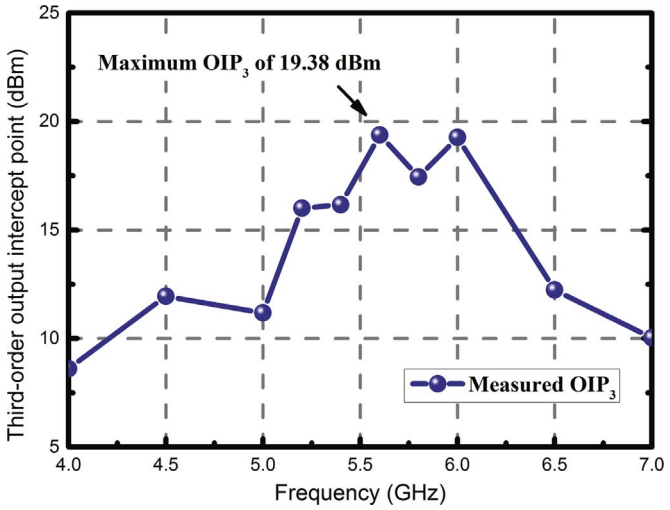

Fig. 13. Measured OIP3 versus frequency.

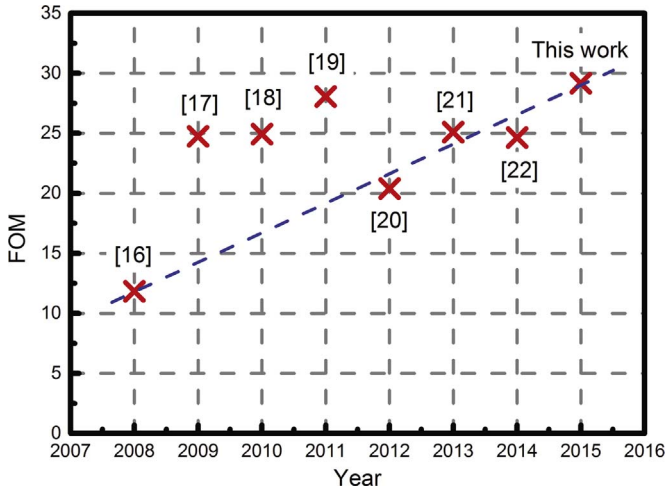

Fig. 14. FOM comparison.

the triode region, and the counterpart is operated in the off region as the switch stays off. The switch must be monitored such that it will not be suffered from imperfect switching function caused by the large but vain saturation region as the on/off state switches. Based on the theory of microelectronic circuits [15], the threshold voltage of a conventional MOS transistor is given as

$$V_{th} = V_{th0} + \gamma\left[\sqrt{2\varphi_f + V_{SB}} - \sqrt{2\varphi_f}\right] \tag{7}$$

where V_{th0} is the threshold voltage as the source-bulk potential difference (V_{SB}) equals to zero, γ denotes the body effect coefficient, and φ_f is the surface potential. The LO body-grounded technique of the proposed mixer generates a non-zero (V_{SB}) such that the threshold voltage (V_{th}) is increased. Besides, if the power consumptions of traditional and proposed mixer are the same, then i_a in Fig. 2 is smaller than i_{d1} in Fig. 1 owing to $i_a = i_{M1} + i_{M3} = K|V_{OV}|^2$. The overdrive voltage can be efficiently reduced by employing LO body-grounded and current-reused techniques.

Thanks to the gm-boosting technique, the differential IF currents shown in Fig. 2, namely i_a and i_b in the *S*-domain, are expressed as follows:

$$i_a(S) = -i_b(S) = \frac{V_{IF}(S)}{2}(2g_{m1,2} + g_{m3,4}) \tag{8}$$

where $g_{m1,2}$ and $g_{m3,4}$ are the transconductance of $M_{1,2}$ and $M_{3,4}$, respectively. If $V_{IF}(S)$ is $V_{IF}\cos(j\omega_{IF}t)$, the output current of the proposed up-conversion mixer can be derived as follows:

$$i_{out}(t) = i_c(t) - i_d(t) = (2g_{m1,2} + g_{m3,4})\cdot V_{IF}\cos(\omega_{IF}t)\cdot sq[\cos(\omega_{LO}t)] \tag{9}$$

Neglecting high order terms of the square waveform function, the LO signal is rewritten as $sq[\cos(\omega_{LO}t)] = 4/\pi\cdot\cos(\omega_{LO}t)$, based upon Eq. (9). The output current at $\omega_{IF} + \omega_{LO}$ can be attained as follows:

$$i_{out}(t) = \frac{2}{\pi}(2g_{m1,2} + g_{m3,4})V_{IF}\cos(\omega_{IF}t + \omega_{LO}t) \tag{10}$$

Hence, the CG of the up-conversion mixer is derived:

$$CG = \frac{V_{RF,rms}}{V_{IF,rms}} = \frac{2}{\pi}(2g_{m1,2} + g_{m3,4})\cdot\frac{\omega L}{\sqrt{1 + (\omega L/R)^2}} \tag{11}$$

where the total transconductance G_m can be expressed as follows:

$$\begin{aligned} Gm &= 2gm_{1,2} + gm_{3,4} = 4k_n V_{OVn} + 2K_P V_{OVp} \\ &= 4k_n(V_{GSn} - V_{thn}) + 2K_P(V_{SGp} - V_{thp}) \end{aligned} \tag{12}$$

If $4k_n = 2K_P = K_{eq}$, Eq. (11) is rewritten as follows:

$$Gm = K_{eq}(V_{DD} - V_{thn} + V_{thp}) \tag{13}$$

Compared with Eq. (6), the CG is obviously increased by gm-boosting and current-reused techniques given that power consumption in both cases are the same. However, the mixer consumes larger chip area if inductors L_s are used to avoid the signal loss through the ground. Notably, since the transconductance derivation of Eq. (10) is irrelevant to square root, the proposed up-conversion mixer achieves relatively linear transconductance. Moreover, according to Eq. (13), the deriva-

Table 3
Performance comparison.

References	[17][a]	[18][b]	[19][b]	[20][b]	[21][a]	[22][b]	[23][b]	This work
Year	2008	2009	2010	2011	2012	2013	2014	2015
Process (μm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Supply voltage (V)	1.8	1	1.2	1.8	1.5	1.2	1.2	1.1
IF frequency (MHz)	10	N/A	N/A	100	100	100	100	10
RF frequency (GHz)	5.26	3–5	3.4–3.7	5.2	5.2	1.8	1.8	5–6
CG (dB)	6.3	6.5	11.5	6	6.5	5	8.1	5.6–7.2
OIP3 (dBm)	−2.6[c]	18.1	5.5	10	6.7	19.68	23.9	19.38
Power (mW)	15.3	11	2.38	2.48	6.25	9.45	14.28	4
FOM	11.89	24.74	24.92	28.06	20.4	25.09	24.64	29.17
Chip area (mm^2)	0.69	0.688	0.855	N/A	1.265	0.85	0.995	0.85

[a] Measurement.
[b] Simulation.
[c] Estimation.

tion is unrelated to input signal. That is, as properly choosing the aspect ratio of the current-reused CMOS inverters, a high linearity of the up-conversion mixer can be achieved.

Apparently, the transconductance can be further enhanced by adopting gm-boosted and current-used techniques. Take the conventional up-conversion mixer with LO body-grounded in Fig. 4 as an illustrative example to be compared with ours. Fig. 5 presents the CG simulation of our design vs. the conventional up-conversion mixer with and without LO body-grounded technique. Notably, all of the simulations are based on the same semiconductor process, power consumption, LO and RF power, output load and source inductors (L_S). The design parameters of the conventional (with and without LO body-grounded) and the proposed up-conversion mixer are listed in Tables 1 and 2, respectively. Referring to Fig. 5, our design attains averagely 3.22 dB over the conventional mixers.

3. Simulation and measurement

Fig. 6 illustrates the design flow of the proposed up-conversion mixer. The proposed high linearity up-conversion mixer is implemented using TSMC 0.18-μm standard CMOS technology. Agilent ADS and Cadence Virtuoso commercial softwares are the tools to carry out our design. Lastly, Agilent Momentum software is used to analyze the electromagnetic (EM) effect. Fig. 7(a) and (b) shows the layout and die photo of the proposed design, respectively, including RF pads and dummy metal, where the area is $1 \times 0.85\ mm^2$. The simulated CG and IIP3 at different PVT corners are shown in Fig. 8.

The implemented mixer is characterized on wafer using a measurement system comprising Agilent E4440A spectrum analyzer, E8247C signal generator, E4413 power meter and DC power supply as shown in Fig. 9. Both IF and LO input ports are coupled to an external 180° hybrid balun through G–S–G–S–G probes for single-to-differential conversion. The RF port is connected to the spectrum analyzer through dc-blocking capacitors to measure the output characteristics.

Fig. 10 shows the simulated and measured power conversion gain ranging from 4 to 7 GHz, while the IF and LO signal power are set to −30 and 0 dBm, respectively. The gm-boosted up-conversion mixer demonstrates a moderate power conversion gain with a flatness variation of ± 1.63 dB. The maximum conversion gain of 7.21 dB is found at 5.4 GHz, whereas the minimum conversion gain of 5.58 dB is located at 6 GHz. Notably, the simulated and the measured curves of the conversion gain are matched very well. Referring to Fig. 11, the measured CG of our design is compared with those of conventional up-conversion mixers with and without LO body-grounded. Apparently, our CG outperforms either mixer.

Fig. 12 exhibits the simulated and the measured IIP3 of the implemented mixer in the range 4–7 GHz. The frequencies of the two-tone IF baseband signals are selected as 9 and 11 MHz with a difference of 2 MHz. The gm-boosted up-conversion mixer shows the maximum IIP3 of 13.17 dBm at 6 GHz, and the minimum IIP3 of 4.5 dBm is attained at 5 GHz given that the IF and LO power are chosen to be −30 and 0 dBm, respectively. Both the simulated and the measured curves are also matched well.

In addition to the IIP3, another linear characteristic is OIP3, which is also widely recognized for up-conversion mixer designs, since it can be used as one RF function block in the front-end. The OIP3 is defined as follows [13]:

$$OIP3 = IIP3 + CG \tag{14}$$

Fig. 13 depicts the variation of the OIP3 of the proposed mixer using gm-boosted technique. The maximum OIP3 of 19.38 dBm is located at 5.6 GHz. In summary, the proposed mixer demonstrates an excellent linear feature.

Moreover, the entire measurement is carried out by a supply voltage of 1.1 V, and the power consumption of the proposed gm-boosted up-conversion mixer is 4 mW measured by the power meter. Besides, the performance of the proposed 5–6 GHz up-conversion mixer can be appraised using a well-known figure of merit (FOM), as shown below [16]:

$$FOM = 10\log\left(\frac{10^{CG_{\max}/20} \times 10^{(IIP3_{\max}-10)/20}}{Pd}\right) \tag{15}$$

where CG_{max} is the maximum conversion gain in dB, $IIP3_{max}$ is the maximum input third-order intercept point in dBm, and Pd is the power dissipation in Watts. Table 3 tabulates a performance comparison between the proposed wideband up-conversion mixer and prior state-of-the-art mixers [17–23]. The up-conversion mixer reported in this study with lower IF frequency of 10 MHz and highest RF frequency of 6 GHz than the other literatures. Our design also attains OIP3 of 19.38 dBm and CG of 7.2 dB. Although the prior mixers in [22,23] exhibit a higher OIP3, they consume larger power. It is obvious that the proposed mixer has the highest FOM of 29.17 with a power consumption of 4 mW, which is also shown in Fig. 14.

4. Conclusion

In this work, a highly linear up-conversion mixer for 5–6 GHz applications has been developed using TSMC 0.18-μm 1P6M CMOS technology. A prototype of this mixer was measured at an LO power of 0 dBm and an IF power of −30 dBm with 4 mW of DC power dissipation given a 1.1 V supply. By employing gm-boosting, current-reused, and LO-body grounded techniques, the proposed up-conversion mixer shows the maximum CG of 7.2 dB, the maximum IIP3 of 13.17 dBm, and an excellent OIP3 of 19.38 dBm. Finally, the implemented mixer is well suited for WLNA applications.

Acknowledgments

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