2 × VDD output buffer with 36.4% slew rate improvement using leakage current compensation

C.-C. Wang✉, T.-Y. Tsai, T.-J. Lee and K.-W. Ruan

A 2 × VDD output buffer using leakage current compensation is demonstrated. With the proposed leakage current compensation circuit, the SR (slew rate) is improved 36.4–101.89% based on on-silicon measurement results given different VDDIO (1.0/1.2/1.8 V) and temperatures (from 0 to 100°C). The data rate is 510/630/400 MHz for VDDIO at 1.8/1.2/1.0 V, respectively. Moreover, the reliability problem, the gate oxide overstress and the hot carrier degradation is avoided. The proposed design is implemented using a typical 90 nm CMOS process. The active area is 0.425 × 0.0563 mm. The SR is measured in the range from 0.766 to 2.585 V/ns.

Introduction: Mixed-voltage output buffers are often required to operate given different supply voltages. To attain transmission quality in extreme environments, the slew rate (SR) was reported to be self-adjusted using phase-locked loop, delay-locked loop, speed-locked loop based and PVT (process, voltage, and temperature) [1, 2] compensation for the output buffers to meet different standards, e.g. low-power double-data-rate two (LPDDR2) (1.0–2.5 V/ns), and peripheral components interconnect X (PCI-X) 133 (1–4 V/ns). However, these compensation circuits cannot be directly applied to 2 × VDD output buffers owing to the stringent SR requirement in these standards. Therefore, the PVT compensation for the SR improvement of 2 × VDD output buffers was presented recently [3, 4]. Nevertheless, these prior works did not consider the leakage current. The leakage current, particularly, is a severe problem in the nano-scale CMOS process [5–8]. The leakage current results in the unstable gate bias voltages at the output stage of the 2 × VDD output buffer, which in turn results in the poor SR. Moreover, what's even worse is that it causes the reliability problem due to the gate oxide overstress and hot carrier degradation if the voltage differences across the terminals of the transistors are larger than the tolerant voltage required by the foundry. Thus, this Letter proposes the leakage current compensation for SR of 2 × VDD output buffer to achieve the SR improvement in three VDDIO cases and five temperature corners. The maximum data rate is 630 MHz for VDDIO at 1.2 V.

2 × VDD output buffer using leakage current compensation: Fig. 1*a* shows the block diagram of the proposed 2 × VDD output buffer composed of the PVT sensor, the PVT decider, the leakage current compensation circuit, and the 2 × VDD output stage. The PVT sensor and PVT decider employed in the PVT compensation are based on the prior work [9]. Fig. 1*b* shows the schematic of 2 × VDD output stage in Fig. 1*a*.

Fig. 1*c* shows the schematic of leakage current compensation circuit, comprising leakage current detector and voltage-controlled current source. MP803–MP805 and MN801–MN802 are a single-stage comparator with the positive input biased at V_{REF18} and the negative input coupled to VD18. V_{REF18} is generated by VDDIO detector 2, which is the replica of VDDIO detector. Notably, VDDIO detector 2 has no loading effect and VD18 indicates the leakage effect caused by the large PMOS transistor, MP_2. When VD18 < V_{REF18}, V_x is biased at VDD. It turns on MN803 such that V_{comp} is pulled down to 0 V. Thus, MN805 and MN806 are turned off. The compensation current I_{comp} is close to zero. When VD18 > V_{REF18}, V_x is biased at 0 V. MN803 is then turned off such that V_{comp} is pulled high to VDD. MN805 and MN806 are turned on. The compensation current, I_{comp}, is then determined by the transistors of MP807, MN805 and MN806. By tuning the aspects of MP807, MN805 and MN806, the leakage current, $I_{leakage}$, at MP_2 will be compensated.

Fig. 1*d* reveals the terminal voltages of MP_2 in the output stage when V_{PAD} is charged from 0 V to VDDIO. When V_{PAD} is at 0 V and VDDIO is biased at 1.8 V, V_{g2} is 0.6 V and V_{s2} is clamped at $V_{g2} + |V_{tp}|$ initially. When the state of the output is flipped, MP_{1a}–MP_{1c} are turned on to charge V_{s2} to VDDIO. At the same time, V_{PAD} is charged to VDDIO. The *IV* curve of the MP_2 is illustrated in Fig. 1*e*. During the charging process, MP_2 operates in the saturation region initially and then moves to the triode region. By using the reciprocal slope of the grey line through point A and point B as the effective resistance of MP_2, the analysis can be carried out easily. The SR is expressed as the slope of the saturation current charging the total equivalent capacitor at PAD

$$\begin{aligned} SR &= \frac{\Delta V_{SD}}{\Delta t} = \frac{I_{D2,sat}}{C_{tot}} = \frac{I_{D2,sat}}{C_{gd} + C_L} \\ &= \frac{(1/2)\mu_p C_{ox}(W/L)(\text{VDDIO} - 0.6 - |V_{tp}|)^2}{(1/2)WLC_{ox} + C_L} \end{aligned} \tag{1}$$

When the leakage current, $I_{leakage}$, is injected to the gate of MP_2, V_{g2} is charged to 0.6 V + $\Delta V_{leakage}$. SR becomes as follows:

$$SR = \frac{(1/2)\mu_p C_{ox}(W/L)(\text{VDDIO} - 0.6 - \Delta V_{leakage} - |V_{tp}|)^2}{(1/2)WLC_{ox} + C_L} \tag{2}$$

where $\Delta V_{leakage}$ is the voltage rise caused by the leakage current injection. As shown in Fig. 1*b*, the compensation current means to drain the leakage current, $I_{leakage}$. Theoretically, the voltage rise, $\Delta V_{leakage}$, will be eliminated when

$$I_{comp} = I_{leakage} \tag{3}$$

However, the real leakage current is almost impossible to detect or measure accurately. Through the simulations, the leakage of MP_2 is estimated to be 500 µA for VDDIO = 1.8 V and the aspects of MP805–MP808 can be derived accordingly. Thus, the leakage current compensation circuit generates the compensation current with the same magnitude to drain the leakage current when it detect the voltage rise at the gate of MP_2.

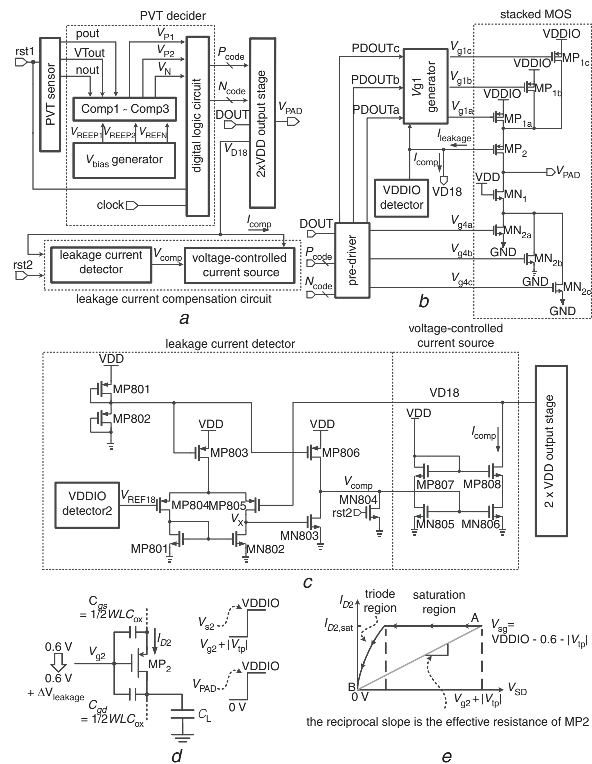

Fig. 1 *Block diagrams, schematics, and illustrations of proposed design*

a Block diagram of the proposed 2 × VDD output buffer
b Schematic of 2 × VDD output stage
c Schematic of leakage current compensation circuit
d Illustration of the terminal voltages
e Illustration of the *IV* curve of MP2 in the output stage when V_{PAD} is charged from 0 V to VDDIO

Implementation and measurement: The proposed 2 × VDD output buffer is implemented using a typical 90 nm CMOS process. The active area of one buffer is 0.425 × 0.0563 mm, as shown in Fig. 2*a*. The die is covered with the dummy metals of the upper layers requested by the foundry. Thus, the circuit is invisible in the microphotograph and the dashed line just shows where the IO1 and IO2 are. Notably, the left of Fig. 2*a* is the layout of the proposed design.

Figs. 2*b*–*d* show the measured eye diagrams at 25°C given different VDDIOs. The maximum data rate is measured to be 400, 630, and 510 MHz for VDDIO at 1.0, 1.2, and 1.8 V, respectively. Figs. 2*e*–*g*

reveal the measured waveforms of V_{PAD} for various VDDIO at 25°C with the data rate of 400 MHz. The improvement of the SR is 38.52% (from 0.553 to 0.766 V/ns), 66.9% (from 0.84 to 1.402 V/ns), and 73.84% (from 1.487 to 2.585 V/ns) for VDDIO at 1.0, 1.2, and 1.8 V, respectively.

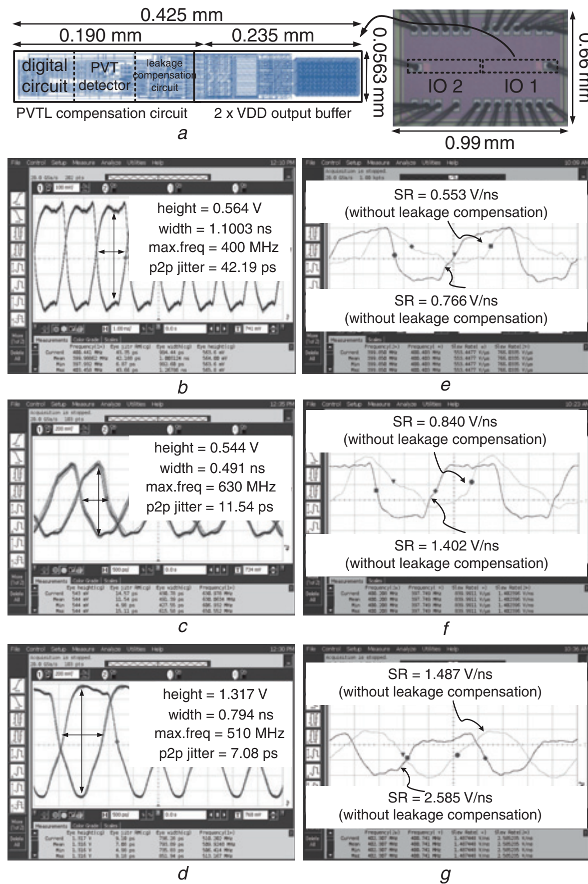

Fig. 2 *Diephoto and measurement results*

a Diephoto of the proposed 2 × VDD output buffer
b, *c* and *d* Eye diagrams of maximum data rate when VDDIO = 1.0/1.2/1.8 V
e, *f* and *g* Output SR on 400 MHz data rate for VDDIO = 1.0/1.2/1.8 V

Table 1 summarises performance comparison with several prior works using only PVT compensation. Ker and Chiu and Shin *et al.* in [3, 10] utilised the process compensation for three corners to reduce the variation of the SR in different PVT corners, respectively. They, however, did not demonstrate the improvement of the SR. Besides, the data rate is only 125 MHz in [3]. The SR of Shin's report is only 0.23–0.28 V/ns even though the load compensation is considered. The SR of Wang's study is improved by 117% and the frequency is improved from 85 to 120 MHz for VDDIO at 3.3 V [4]. However, it does not provide the leakage current compensation and the data rate is still slow.

Table 1: Comparison with several prior works

	This work	[4]	[3]	[1]	[10]
Year	2015	2013	2013	2010	2007
Production		TCAS-I	TCAS-I	TCAS-II	TCAS-II
Process	90 nm	0.18 μm	90 nm	0.18 μm	0.13 μm
VDD (V)	1.0	1.8	1.2	1.8	3.3
VDDIO (V)	1.8/1.2/1.0	3.3/1.8	2.5/1.2	1.8	3.3
Data rate (MHz)	510/630/400	120	125	2000	N/A
SR (V/ns)	0.766–2.585	1.28–2.79	2.1–3.4	2.1–3.58	0.23–0.28[a]
SR improvement (%)	36.4–101.89	117	N/A	28 (post-sim)	N/A
Compensation	PVT and leakage	PT	PVT	PVT	PVT and load

[a]SR is estimated from the voltage differences over the rising time in their report.

Kwak *et al.* [1] reported 2000 MHz data rate and 2.1–3.58 V/ns SR. However, it provides only one output voltage mode. Besides, the SR improvement is only based on the simulation results. Our work shows the SR improvement from 36.4 to 101.89% in 15 corners of VDDIO (1.0, 1.2, and 1.8 V) and temperatures (0, 25, 50, 75, and 100°C). Moreover, this work possesses the maximum data rate of 630 MHz for VDDIO at 1.2 V and temperature of 25°C. It outperforms all of these prior works.

Conclusion: This Letter proposes the 2 × VDD output buffer with process, voltage, temperature, leakage (PVTL) compensation. By using the proposed leakage current compensation, the gate oxide overstress is avoided. Moreover, the SR is improved 36.4–101.89% in 15 cases of VDDIO (1.0/1.2/1.8 V) and temperatures (0/25/50/75/100°C). The maximum frequency is measured to be 510/630/400 MHz for VDDIO at 1.8/1.2/1.0 V, respectively.

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One or more of the Figures in this Letter are available in colour online.

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