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High-voltage on-chip current sensor design and analysis for battery modules

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Abstract: Large current sensing in a high-voltage (HV) battery module or string is hard to be realised on-chip. Thus, it is a disadvantage for the system to be miniaturised. A current sensor with a HV sense stage on silicon for HV battery modules is designed and analysed in this investigation. The proposed HV current sensor takes advantage of HV CMOS processes and resolves the problems caused by the voltage drop limitation thereof. The design methodology and analysis, including aspect sizes, are also presented. The physical on-chip and system measurement of the proposed HV current sensor demonstrates maximum error ≤ ±0.7% provided that the sensing voltage is 36–55 V, and the sensing current is 0.5–2.2 A.

1 Introduction

In a foreseeable future, efficient energy utilisation has become a driving force for almost every country to floorplan their economic strategy. Besides, reducing pollution and saving energy are also future goals of industrial development in response to global warming and environmental issues. Energy storage based on batteries is considered as one of the critical devices to propel efficient energy utilisation [1]. For instance, electric vehicles (EV), e.g., hybrid electric vehicle (HEV), plug-in HEV [2, 3] and E-scooter [4] heavily rely on power of battery systems and the associated battery management systems (BMS).

The core technology of the mentioned battery-operated vehicles, e.g., EV, includes battery modules and the BMS [5, 6]. A battery module is composed of series or parallel battery cells, and battery modules can also be connected in series or in parallel to constitute a larger battery pack. Notably, the cells in EV power systems are all reusable batteries, which are charged and discharged frequently. Therefore, SOH (state of health) and SOC (state of charge) of battery cells must be monitored to find out which cells are aged or malfunctioned caused by overcharge and overdischarge. Namely, BMS is in charge of battery storage safety. In addition, BMS also needs to attain real-time battery information for diagnosis and analysis, which helps to achieve energy efficiency [4].

The most popular approach of current sensing is the Hall effect current sensor [7, 8]. Hall effect is generated by the Lorentz force [9]. When a magnetic field is not parallel to the direction of the current in a conductor, the charge in the conductor is affected by a force, namely the Lorentz force. Therefore, the Hall voltage will be generated in the conductor to resist the Lorentz force. Likewise, the Hall voltage is also generated when a magnetic field is not parallel to the direction of a semiconductor. Because the sensing current flows through Hall coil, the Hall voltage varies in response to the sensing current. Thus, the Hall voltage is deemed as the sensed voltage to estimate the current. The advantage of the Hall effect current sensor is low cost and good reliability. However, the accuracy by the Hall effect current sensing is lower than that of other current sensors. Thus, a compensator is usually required to enhance the accuracy.

When it comes to current sensing in HV systems, insulated-gate bipolar transistor (IGBT)-based approaches were quite popular as well due to the feature that IGBT can carry a large current. Motto and Donlon proposed an IGBT-based current sensor, where a small portion of the main emitter current is duplicated by a current mirror structure to sense the large emitter current [10]. A lateral insulated-gate bipolar transistor (LIGBT) structure then was also proposed in smart power ICs [11]. However, IGBT or LIGBT is not a good option to be carried out with other control circuit on the same die, since they are mainly power devices good for drivers or discretes. By contrast, because high-voltage (HV) designs cannot be realised by low-voltage (LV) technologies [12–16], most of the existing current sensors fabricated by LV technologies were not applied in HV systems. For instance, Shalmany *et al.* proposed a micro-power current-sensing system including a calibrated shunt resistor to sense current of the battery [12]. Wang *et al.* proposed a current measurement method dedicated for electromigration management [13]. Another design was the dynamically biased shunt feedback technique current sensor, which pushes non-dominant poles to higher frequencies to improve stability and speed of the current sensor to cover a wide range of load currents [14]. Many other reported current sensors have been implemented on chip [10–17]. Nevertheless, only one of above-mentioned design physically comprises a HV current sensing resistor on the same die [12].

Thanks to the presence of bipolar-CMOS–DMOS (BCD) process featured with a HV spectrum running from 12 to 60 V to support the application specific standard power IC [18], a current sensor with a HV sense stage carried out by the BCD process is proposed in this work. Although HV BCD processes are available, prior or existing current sensor designs cannot be directly migrated to this process because of strict voltage drop limitations of the MOS devices of these HV processes. We have analysed the HV current sensor, which design is based on the required voltage drop limitations such that even the HV large current can be estimated, the safety of those HV devices are also firmly ensured.

2 HV current sensor

Fig. 1 shows the proposed HV current sensor in this work, including R_{sense}, $K \times R_{sense}$, and HV sense stage. R_{sense} is a very small resistor. The ratio, K, is selected to be 10^6 such that the resistances of R_{sense} and $K \times R_{sense}$ are set to be feasible 0.01 Ω and 10^4 Ω, respectively. They are both too small to affect the load of BMS [12, 13]. Consequently, the current flowing through the load would not be interfered with that in the HV current sensor.

2.1 Features of HV MOS

The HV BCD process not only offers HV devices but also provides LV PMOS and LV NMOS, as shown in Fig. 2. The voltage

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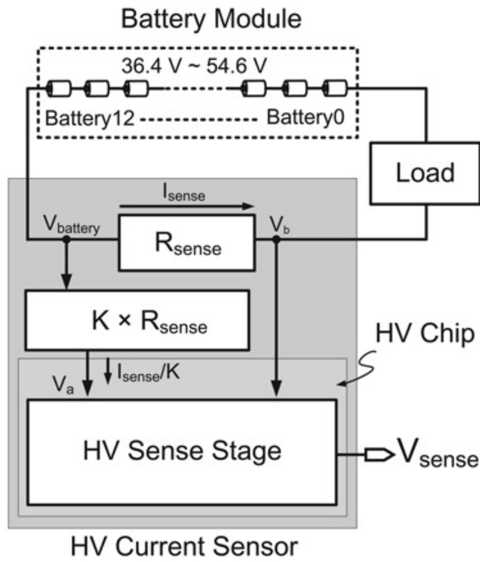

Fig. 1 *Block diagram of the proposed HV current sensor*

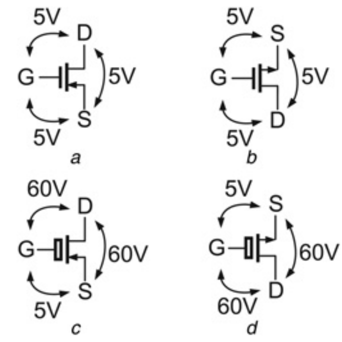

Fig. 2 *Voltage limitations of*

a LV PMOS
b LV NMOS
c HV PMOS
d HV NMOS

limitation of those LV devices is 5 V between any two terminals. By contrast, the most critical limitation is that the gate-to-source voltage of HV PMOS and HV NMOS must be kept under 5 V to prevent breakdown hazards. By contrast, the drain-to-source voltage of HV PMOS and HV NMOS can sustain up to 60 V drop, as shown in Figs. 2*c* and *d*, respectively.

2.2 HV sense stage

The HV sense stage in Fig. 1 is realised by four HV PMOSs (HP1–HP4), and four HV NMOSs (HN1–HN4) as shown in Fig. 3. The current mirror composed of HP2 and HP3 equalises I_2 and I_3 such that V_a equals to V_b.

Assume $I_{sat,HP2}$, $I_{sat,HP3}$, $I_{sat,HN2}$, and $I_{sat,HN3}$ are the saturation currents in HP2, HP3, HN2, and HN3, respectively, as shown in (1)–(4).

$$I_{sat,HP2} = \frac{1}{2}\mu_p C_{ox,p}\frac{W_{HP2}}{L_{HP2}}(V_{GS,HP2} - V_{th,HP2})^2 \times (1 + \lambda_{HP2}V_{DS,HP2}) \quad (1)$$

$$I_{sat,HP3} = \frac{1}{2}\mu_p C_{ox,p}\frac{W_{HP3}}{L_{HP3}}(V_{GS,HP3} - V_{th,HP3})^2 \times (1 + \lambda_{HP3}V_{DS,HP3}) \quad (2)$$

$$I_{sat,HN2} = \frac{1}{2}\mu_n C_{ox,n}\frac{W_{HN2}}{L_{HN2}}(V_{GS,HN2} - V_{th,HN2})^2 \times (1 + \lambda_{HN2}V_{DS,HN2}) \quad (3)$$

$$I_{sat,HN3} = \frac{1}{2}\mu_n C_{ox,n}\frac{W_{HN3}}{L_{HN3}}(V_{GS,HN3} - V_{th,HN3})^2 \times (1 + \lambda_{HN3}V_{DS,HN3}) \quad (4)$$

where μ_p is the carrier mobility of PMOS, μ_n is that of NMOS, $C_{ox,p}$ is the capacitance of gate oxide of PMOS, $C_{ox,n}$ is that of NMOS, W is the channel width of MOS, L is the channel length, V_{GS} is the gate-to-source voltage of the MOS, V_{th} is the threshold voltage, V_{DS} is the drain-to-source voltage of the MOS, and λ is the channel-length modulation parameter.

$I_2 = I_3$ will be attained when the W/L ratio of HP2 and HN2 equal to those of HP3 and HN3, respectively, which results in that $V_{GS,HN2}$, $V_{GS,HN3}$, $V_{GS,HN1}$, and $V_{DS,HN1}$ are identical. $V_{DS,HN2}$ and $V_{DS,HN3}$ can be written as (5)

$$V_{DS,HN2} = V_{DS,HN3} \quad (5)$$

In addition, the gate-to-source voltage of HP2 and HP3 are also identical when they are both saturated. $V_{DS,HP2}$ and $V_{DS,HP3}$ then is written as (6)

$$V_{DS,HP2} = V_{DS,HP3} = V_{GS,HP2} \quad (6)$$

By (5) and (6), $V_a = V_b$ is concluded.

The current mirror consisting of HN1 and HN2 duplicates m times of I_2 to I_1, preventing MOSs from overvoltage. Because the length of HV NMOS is limited to 700 nm according to specification of HV BCD process, the channel-length modulation factor of HV NMOS should be considered. By contrast, when the length of PMOS is large enough, the channel-length modulation factor in (1), (2) can be neglected.

Not only are the width, V_{GS}, and V_{th} of HP1 and HP2 the same, the W/L ratio, V_{GS}, and V_{th} of HN1 and HN2 are also the same. As mentioned earlier, $I_{sat,HP1}$, $I_{sat,HP2}$, and $I_{sat,HN1}$ are assumed as the saturation currents in HP1, HP2, and HN1, respectively, as shown in (7)–(9).

$$I_{sat,HP1} = \frac{1}{2}\mu_p C_{ox,p}\frac{W_{HP1}}{L_{HP1}}(V_{GS,HP1} - V_{th,HP1})^2 \quad (7)$$

$$I_{sat,HP2} = \frac{1}{2}\mu_p C_{ox,p}\frac{W_{HP2}}{L_{HP2}}(V_{GS,HP2} - V_{th,HP2})^2 \quad (8)$$

$$I_{sat,HN1} = \frac{1}{2}\mu_n C_{ox,n}\frac{W_{HN1}}{L_{HN1}}(V_{GS,HN1} - V_{th,HN1})^2 \times (1 + \lambda_{HN1}V_{DS,HN1}) \quad (9)$$

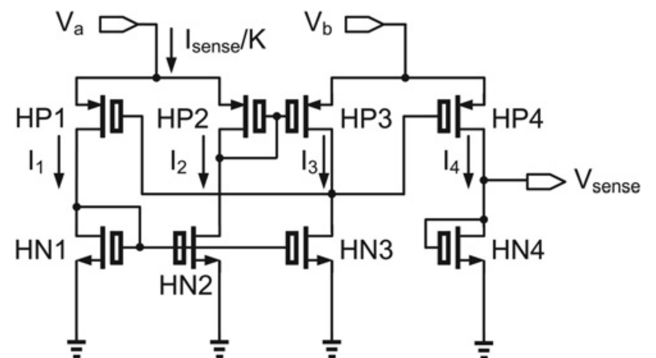

Fig. 3 *Schematic representation of the proposed HV sense stage*

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Based upon (4), (7)–(9), $I_{sat,HP1}$, $I_{sat,HP2}$, $I_{sat,HN1}$, and $I_{sat,HN2}$ are re-organised as

$$\frac{I_{sat,HP1}}{I_{sat,HP2}} = \frac{L_{HP2}}{L_{HP1}} = m \tag{10}$$

$$\frac{I_{sat,HN1}}{I_{sat,HN2}} = \frac{1 + \lambda_{HN1} V_{DS,HN1}}{1 + \lambda_{HN2} V_{DS,HN2}} = m \tag{11}$$

where m is the ratio of I_1 against I_2.

Apparently, if $I_2 < I_{sense}/K$ is substituted into (8), $V_{GS,HP2}$ can be kept < 5 V by tuning size of HP2. Meanwhile, because V_b equals to $V_{DS,HP3} + V_{DS,HN3}$ in Fig. 3, $V_{GS,HP2}$ can be written as follows

$$\begin{aligned} V_{GS,HP2} &= V_b - V_{DS,HN2} < 5 \\ &\Rightarrow V_{DS,HN2} > V_b - 5 \end{aligned} \tag{12}$$

Assume the voltage difference between V_b and that of the battery module ($V_{battery}$) is <1 V, and the minimum voltage of the $V_{battery}$ is 36 V. Consequently, the minimum voltage of V_b is 35 V (= 36–1 V). Equation (12) is re-derived as

$$V_{DS,HN2} > V_b - 5 = 35 - 5 = 30 \tag{13}$$

λ_{HN1} is assumed to the same as λ_{HN2}, if the lengths of HN1 and HN2 as the same [19]. According to (13) and $V_{DS,HN1} = V_{GS,HN1}$, (11) is re-organised as follows

$$V_{GS,HN1} = V_{DS,HN1} > V_{DS,HN2} > 30, \quad \text{when } m > 1 \tag{14}$$

$$V_{GS,HN1} = V_{DS,HN1} = V_{DS,HN2} > 30, \quad \text{when } m = 1 \tag{15}$$

$$\left.\begin{array}{c} V_{GS,HN1} = V_{DS,HN1} < 30 \\ V_{DS,HN1} < V_{DS,HN2} \end{array}\right\}, \quad \text{when } m < 1 \tag{16}$$

Therefore, all MOSs will not run into overvoltage problems in the scenario of (16) as long as the range of $V_{GS,HP2}$ and $V_{GS,HN1}$ is kept between 0 and 5 V. In short, the drain-to-source voltage and the gate-to-source voltage of the MOSs to prevent break down and overcharge are summarised in Table 1.

The current mirror composed of HP1 and HP4 in Fig. 3 duplicates I_1 to I_4, which is derived as follows.

$$I_4 = \frac{m}{1+m} \times \frac{I_{sense}}{K} \tag{17}$$

Assume $I_{sat,HN4}$ is the saturation current in HN4.

$$\begin{aligned} I_{sat,HN4} &= \frac{1}{2}\mu_n C_{ox,n} \frac{W_{HN4}}{L_{HN4}} (V_{GS,HN4} - V_{th,HN4})^2 \\ &\quad \times (1 + \lambda_{HN4} V_{DS,HN4}) = I_4 \end{aligned} \tag{18}$$

Since $I_4 = I_{sat,HN4}$, the relationship between V_{sense} and V_{sense} can be derived.

$$\begin{aligned} V_{sense} &= \sqrt{\frac{2m \times L_{HN4} \times I_{sense}}{1 + m \times W_{HN4} \times \mu_n C_{ox,n}(1 + \lambda_{HN4} V_{DS,HN4})}} \\ &\quad + V_{th,HN4} = \kappa \sqrt{\frac{I_{sense}}{(1 + \lambda_{HN4} V_{DS,HN4})}} + V_{th,HN4} \end{aligned} \tag{19}$$

where

$$\kappa = \sqrt{\frac{2m \times L_{HN4}}{1 + m \times W_{HN4} \times \mu_n C_{ox,n}}}$$

Table 1 HP1–HP3 and HN1–HN3 safe operation voltage range

Voltage limit	V_{GS} 5 V	V_{DS} 60 V
HP1	0–5 V	V_a–$V_{DS,HN1}$ < 60 V
HP2, HP3	0–5 V	0–5 V
HN1	0–5 V	0–5 V
HN2, HN3	0–5 V	V_b–$V_{DS,HP2}$ < 60 V

In summary, I_{sense} can be indirectly estimated by V_{sense} with appropriate aspect ratio of HN4 and m selection.

3 Implementation and measurement

The proposed design is implemented using TSMC 0.25 µm CMOS HV mixed signal general purpose IIA-based BCD 60 V to justify the functionality as well as the circuit theory. Fig. 4 shows the die photograph of the proposed HV sense stage. The core area is $0.926 \times 0.584\,\text{mm}^2$. The entire HV current sensor is used to sense the current of battery module, as shown in Fig. 5. The power supply (Chroma 62012P-600-8 DC Power Supply) generates the equivalent battery voltage, where the magnitude of current is adjusted by an electronic load (PRODIGT 3302C Electronic Load). The oscilloscope (Teledyne LeCroy – WaveRunner 610Zi) is used to demonstrate V_{sense}.

Take a battery string consisting of 13 cascaded IHR18650BN cells of which specification is summarised in Table 2 [20] as an example. The capacity of each battery cell is 2200 mAh. The charge and discharge of the battery module are usually 0.5 C-rate (0.5 C-rate is 1 A). The voltage range of the 13-cell string is from 36.4 to 54.6 V as shown in Fig. 1.

The measurement results are shown in Fig. 6. When the input voltage is 48 V and the sensing current range is from 0.44 to 2.2 A (0.2–1 C-rate), the output range of the HV current sensor, V_{sense}, is from 1.701 to 2.001 V. The maximum error with respect to a linear asymptotic line is as low as 1.13%.

The next experiment is to enlarge input voltage to 36–55 V. In order to make sure that the proposed chip is functional by working in the

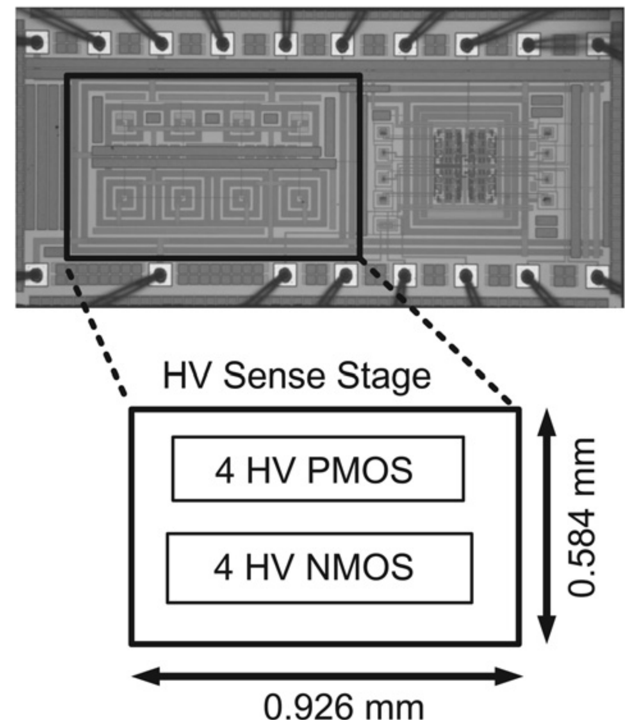

Fig. 4 *Die photograph of the proposed HV sense stage*

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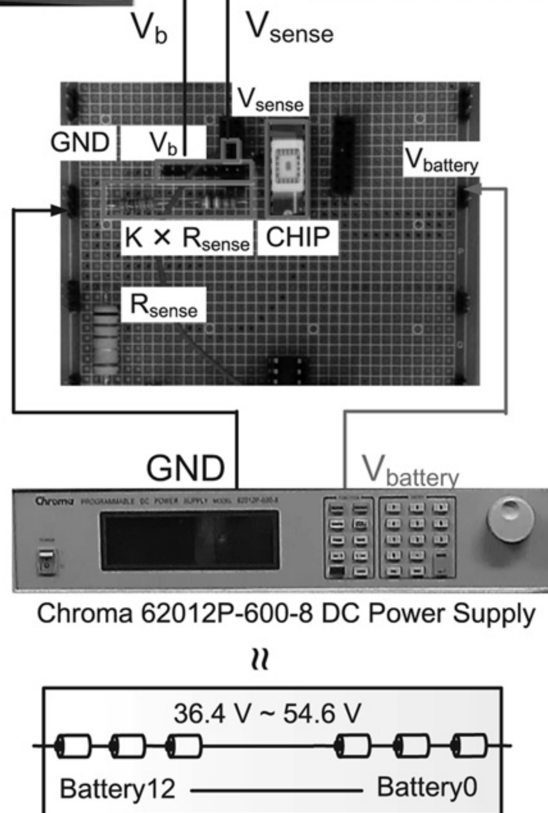

Fig. 5 *Measurement setup of the proposed HV current sensor*

range of 36–55 V, the power supply is applied to provide 20 V cases, i.e., 36, 37, 38, …, 55 V. Besides, the electronic load provides nine testing cases given different currents in the range of 0.44–2.2 A. Fig. 7 shows the error distribution of 20 different sensing voltages given the same current. The error distribution is measured to be <0.7% ($\leq \pm 3\sigma$). The performance comparison of the proposed design and several recent works is tabulated in Table 3. Notably, our design is the only one to work in the range of 36–55 V, 0.44–2.2 A, with maximum error about ±0.7% ($\leq \pm 3\sigma$).

Table 2 Cell specification of lithium-ion rechargeable battery (MODEL : IHR18650BN) [20]

	IHR18650BN
nominal voltage	3.6 V
charge voltage	4.2 V
discharge cut-off voltage	2.8 V
nominal charge current	1 A
maximum charge current	1 A
minimum discharge current	10 A
typical capacity	2200 mAh
minimum capacity	2100 mAh

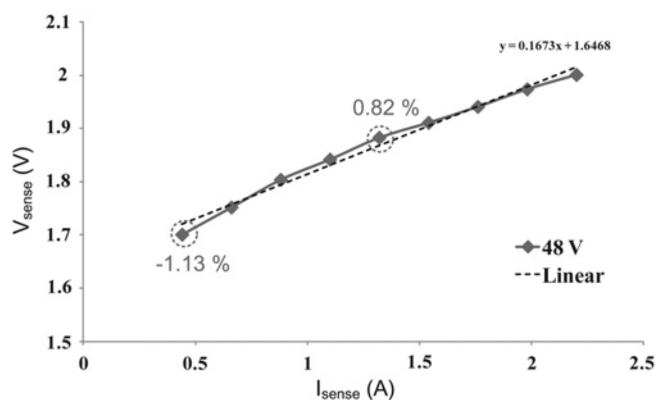

Fig. 6 *Measurement results of the proposed HV current sensor given $V_{battery} = 48$ V*

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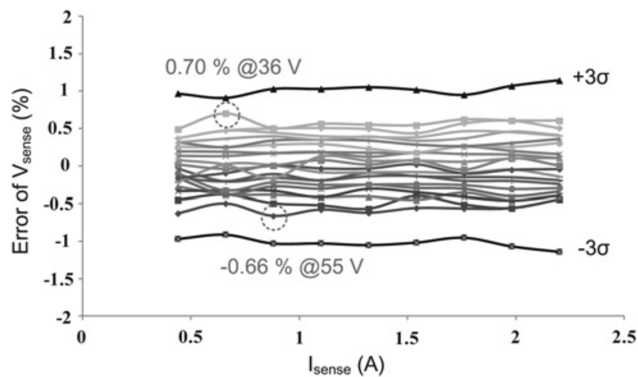

Fig. 7 V_{sense} *error measurement of the proposed HV current sensor*

Table 3 Performance comparison of current sensors

	[14] TCAS-I	[12] ISSCC	[21] TPE	This work
year	2010	2013	2014	2015
process, μm	0.35	0.13	0.5	0.25
supply voltage, V	3.3	1.5	5	5
sensing voltage range, V	2.7–4.2	0–1.5	2.7–4.5	36–55
sensing current range, A	0.025–0.5	0–1	0.05–0.6	0.44–2.2
max. error, %	5	±0.03(≤ ±3σ)	4.7	±0.7(≤ ±3σ)
core area, mm^2	1.1	1.1	2.25	0.541
normalised area, mm$^{2\xi}$	8.98	65.09	9	8.656

$^{\xi}$Normalised Area = Area/Process^2 and σ, Standard deviation

4 Conclusion

This investigation is the first to propose a HV current sensor with a HV sense stage IC using HV CMOS process. Not only is the feasibility of on-silicon HV current sensing is justified, the problems caused by HV process voltage drop limitation is resolved. The proposed design is physically implemented using TSMC 0.25 μm CMOS HV mixed signal general purpose IIA-based BCD 60 V. This work prevents MOSs from overvoltage problem by adjusting the ratio of I_1 and I_2. Thus, our design does not require extra HV circuits or expensive processes. In summary, the physical on-chip measurement of the proposed HV current sensor demonstrates maximum error ≤±0.7% provided that the sensing voltage is 36–55 V, and the sensing current range is 0.5–2.2 A.

5 Acknowledgments

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