A Leakage Compensation Design for Low Supply Voltage SRAM

Chua-Chin Wang, *Senior Member, IEEE*, Deng-Shain Wang, Chiang-Hsiang Liao, and Sih-Yu Chen

***Abstract*— A leakage current compensation design for nanoscale SRAMs is proposed in this paper. The proposed compensation design is composed of a leakage current sensor, which generates a warning signal if the leakage is over a predefined threshold, and a compensation circuit following the sensor, which will be activated to speed up the read operation. At 0.6 V system voltage, the proposed compensation design reduces 27.86% of the average power dissipation, and 54.88% of the read delay at the expense of 3.64% area overhead. The proposed Static Random-Access Memory is implemented using the TSMC 40-nm CMOS logic technology. The energy per access is measured to be 0.9411 pJ given a 600-mV power supply and a 54-MHz system clock rate.**

***Index Terms*— Compensation circuit, disturbfree, leakage sensor, single-ended Static Random-Access Memory cell, SRAM.**

I. Introduction

SRAM HAS been an important role in many products, e.g., the cache of CPU. To extend the operation time and reduce power dissipation, Static Random-Access Memory (SRAM) is usually fabricated using advanced processes. However, as the technology evolving toward the nanometer scale, the leakage becomes a threat. The operation frequency and the power consumption of SRAMs will be deteriorated, because the leakage current increases exponentially with the drop of threshold voltage (V_{th}) and gate oxides [1]–[3]. Although the high V_{th} CMOS has been deemed as a solution to the mentioned issues, it will slow down the operation speed of SRAMs. Therefore, to reduce the leakage and increase the operation speed, three major design approaches were proposed as follows.

1) *Current Mode Sense Amplification [4], [5]:* Since the CMOS technology has been scaled down very fast, the bitline capacitances may be too large for an SRAM cell to drive. During a read operation, the sense amplifier predetermines the output result by sensing the differential current on two bitlines (BL_1 and BLb_1), as shown in Fig. 1, such that the low power and high speed would be feasible [4]. Notably, the output delay is irrelevant of the bitline capacitances in such a scenario.

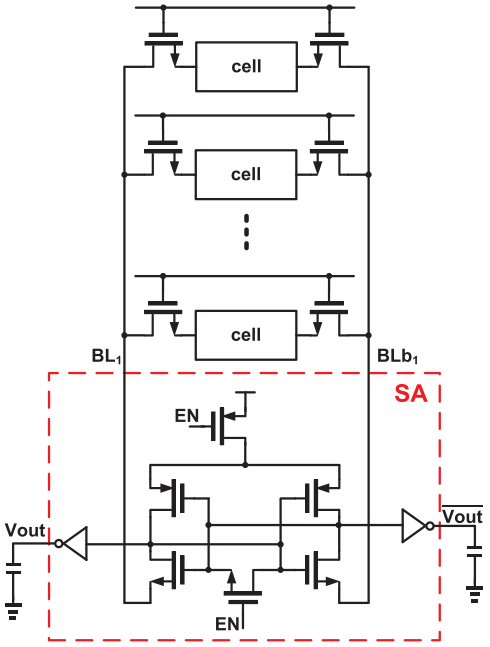

Fig. 1. SRAM with sense amplification [4].

2) *Current Compensation Circuit [6], [7]:* One of the classic current compensation circuits is shown in Fig. 2 [6]. When the SRAM begins to work, the current compensation circuit detects the leakage current of each bitline, and then injects a proper current into the corresponding bitline. For an example, an SRAM array has N cells, where n of the N cell is stored with logic 1, and the rest are stored with logic 0, as shown in Fig. 2. If the bitline leakage is detected, the current compensation circuit injects $n \times I_{\text{OFF}}$ into BLb_2, and $(N - n) \times I_{\text{OFF}}$ into BL_2, where I_{OFF} is the cutoff leakage current. Then, when one of the SRAM cells is activated to read mode, the speed will be enhanced, since the cell does not need to be affected by the leakage current caused by the other cells. Although this way cannot reduce the leakage current, the access speed of the SRAM will be improved.
3) *Secondary Supply [8]:* By using another higher supply voltage, the access of the SRAM cell will be fastened. For example, by boosting the bitline voltage, the write

Manuscript received April 1, 2015; revised June 22, 2015 and August 24, 2015; accepted September 25, 2015. Date of publication November 19, 2015; date of current version April 19, 2016. This work was supported in part by the Ministry of Science and Technology under Grant NSC 102-3113-P-110-101, Grant NSC 102-2221-E-110-081-MY3, and Grant NSC 102-2221-E-110-083-MY3 and in part by the Southern Taiwan Science Park Administration, Taiwan, under Contract BY-09-04-14-102. *(Corresponding author: Chua-Chin Wang.)*

C.-C. Wang, D.-S. Wang, and C.-H. Liao are with the Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung 80424, Taiwan (e-mail: ccwang@ee.nsysu.edu.tw; tonyhenry2@vlsi.ee.nsysu.edu.tw; liao@vlsi.ee.nsysu.edu.tw).

S.-Y. Chen is with National Applied Research Laboratories, Chip Implementation Center, 7F, Chimei Building, Tzu-Chiang, No. 1, Ta-Hsuch Rd., Tainan City 701, Taiwan (e-mail: sihyuuchen@vlsi.ee.nsysu.edu.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2015.2484386

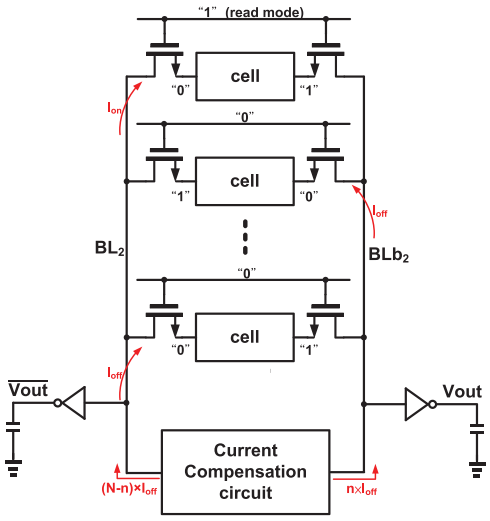

Fig. 2. SRAM with current compensation circuit [6].

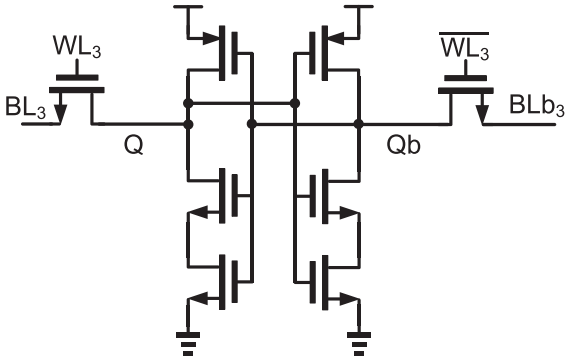

Fig. 3. 8T SRAM cell with stack forcing in pull-down nMOS [9].

speed can be improved due to the current of the access transistor is increased. By contrast, by boosting the supply voltage and reversing body bias voltage in the 6T SRAM cell, the leakage reduction is better than the 8T SRAM cell with stack forcing in pull-down nMOS, as shown in Fig. 3 [9].

In this paper, we propose a new compensation design. The proposed circuit is composed of a leakage current sensor and a compensation circuit. A leakage current sensor is utilized to sense the voltage drop caused by the leakage current. A compensation circuit will speed up the read operation of SRAM if the leakage is detected and confirmed. The proposed SRAM fabricated using the TSMC 40-nm CMOS logic process is proved on silicon to operate at 54 MHz with a 600-mV power supply, and the energy per access is measured to be 0.9411 pJ. At 0.6 V system voltage, the proposed compensation design reduces 54.88% of the read delay at the expense of 3.64% area overhead.

II. 5T SRAM With Leakage Sensor and Read Delay Compensation

The structure of the proposed SRAM using the leakage current sensor and the compensation circuit is shown in Fig. 4.

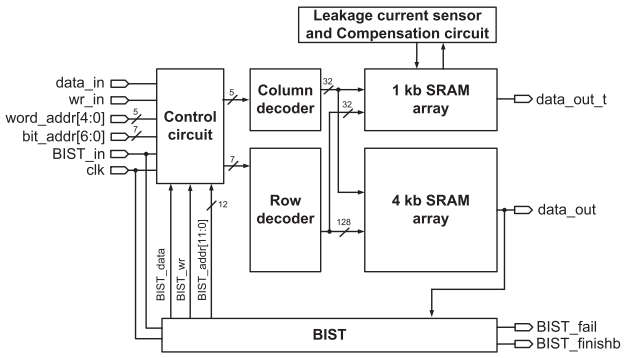

Fig. 4. Block diagram of the proposed SRAM.

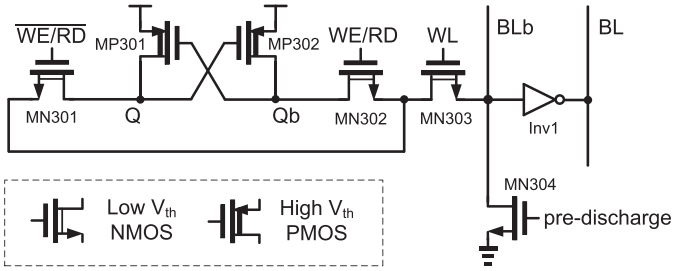

Fig. 5. Schematic of a 5T SRAM cell.

To demonstrate the effect of the proposed compensation circuitry, two SRAM arrays are carried on the same die sharing common row decoder and column decoder. Notably, the 1-kb SRAM array with compensation only needs bit_addr[4:0], while the 4-kb SRAM array without compensation needs bit_addr[6:0]. A control circuit includes several MUXs, which allow BIST_in to select either the normal operation mode or the build-in-self-test (BIST) mode. wr_in determines the entire SRAM is the read mode (wr_in = logic 1) or the write mode (wr_in = logic 0), respectively. word_addr and bit_addr drive column and row decoders to select the corresponding cell, respectively. Data will be stored in the SRAM array via data_in. clk represents the system clock. Notably, the output of the compensated design is data_out_t, while the output of the uncompensated design is data_out. The details of each circuit, as shown in Fig. 4, will be introduced in the following context.

A. Single-Ended Disturbfree 5T Loadless SRAM Cell

Fig. 5 shows a 5T SRAM cell coupled with an inverter. To reduce the cutoff leakage current, high V_{th} pMOS transistors, MP301 and MP302, consist of a latchlike storage. Low V_{th} nMOS transistors, MN301 and MN302, are used as access switches to supply large current for driving the bitline. The single-ended 5T structure is featured by an additional MOS, MN303, which is controlled by word line (WL) to access Qb such that the internal data state stored in Q will not be interfered by the other cells coupled to BLb. Several advantages of the single-ended disturbfree 5T loadless SRAM cell have been reported, including low power, better read static noise margin (SNM), and disturbfree write access.

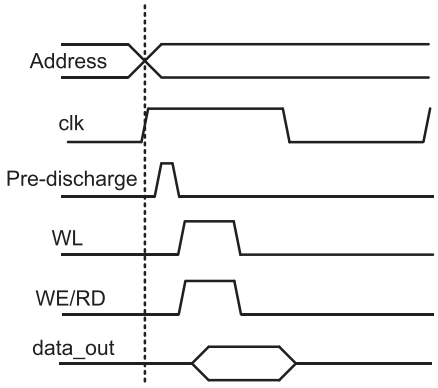

Fig. 6. Read timing diagram of the proposed SRAM cell.

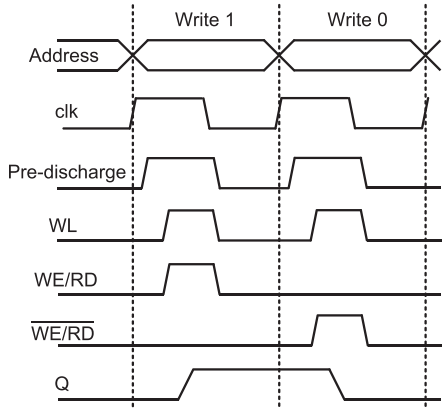

Fig. 7. Write timing diagram of the proposed SRAM cell.

Since the proposed single-ended SRAM cell has no path to ground on nodes Q and Qb, a hidden self-refreshing path is used to neutralize the leakage [10]. With the proven best power delay product (PDP), eight SRAM cells are coupled with a shared inverter in [10].

Figs. 6 and 7 show the read and write timing diagrams, respectively. The steps of each access are described as follows.

1) *Read Access:*
   a) *Step 1:* Referring to Fig. 6, after clk rises high, the predischarge is then pulled high to discharge BLB to ensure that the parasitic capacitance on BLB would not be charged back to the SRAM cell.
   b) *Step 2:* After discharging BLB, WL and WE/RD are pulled high to turn ON MN303 and MN302, respectively. Meanwhile, the state of Qb will be coupled to BLB.
2) *Write Access:*
   a) *Step 1:* Referring to Fig. 7, after clk rises high, the predischarge is pulled high to discharge BLB.
   b) *Step 2:* If data_in is logic 1 (or 0), WL and WE/RD (or $\overline{\text{WE/RD}}$) are high to turn ON MN303 and MN302 (or MN301), respectively. Meanwhile, the state of Qb (or Q) will be coupled to BLB, so that it will be overwritten.

However, once the leakage current starts to increase because of temperature or process variations, the voltage of the node stored with 0 state would rise to cause a longer read delay and more power dissipation.

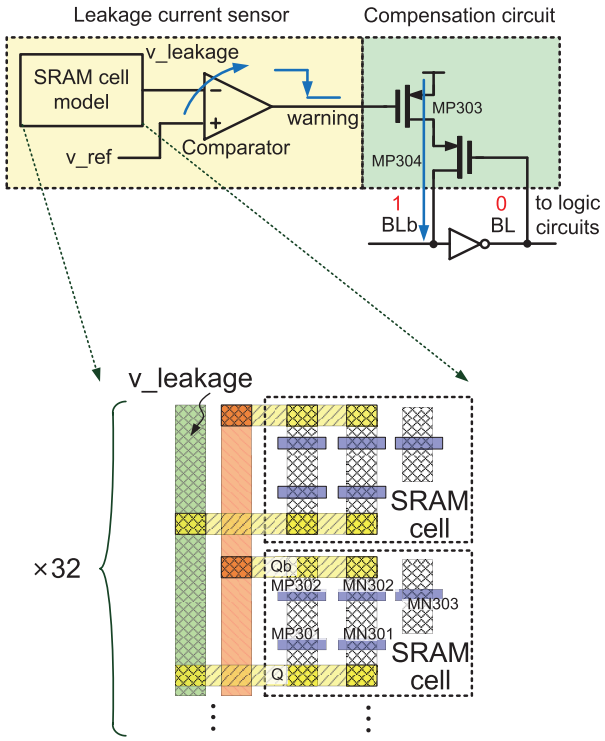

Fig. 8. Schematics of leakage current sensor and compensation circuit.

B. Leakage Current Sensor

The proposed compensation design is composed of the leakage current sensor and compensation circuit, as shown in Fig. 8. A leakage current sensor consists of an SRAM cell model and a comparator. Since a large leakage will result in low operating frequency, high power consumption, and even status flip in the SRAM cell, an SRAM cell model is used as a leakage monitor generating a voltage proportional to the leakage current, v_leakage, for comparator. If v_leakage is higher than v_ref, comparator will notify a warning signal to activate the following compensation circuit.

In this paper, we couple the node Q of 32 SRAM cells together and turn OFF all transistors to serve as the SRAM cell model. The reason is when the nodes Q of many SRAM cell are coupled together, the corresponding leakages of these cells are steered to the same node such that the common Q node voltage, v_leakage, will be pulled high almost proportionally. Fig. 9 shows the voltage of v_leakage provided that different number SRAM cells are coupled. Apparently, the voltage difference between the TT corner and the other process corners is significantly enlarged. Referring to Fig. 8 again, v_leakage stands for the common node Q in the SRAM cell model.

Fig. 10 shows the schematic of comparator, which is basically a differential comparator to compare v_leakage with a predefined reference voltage, v_ref. Notably, v_ref plays a critical role in the proposed design such that v_ref must be determined by thorough simulations. Fig. 11 shows the voltage of v_leakage in an SRAM cell model with all process, temperature (PT) corner simulations. The proposed 5T SRAM cell is proved to keep the stored bit by the hidden self-refreshing path [10]. However, during the read 0 operation,

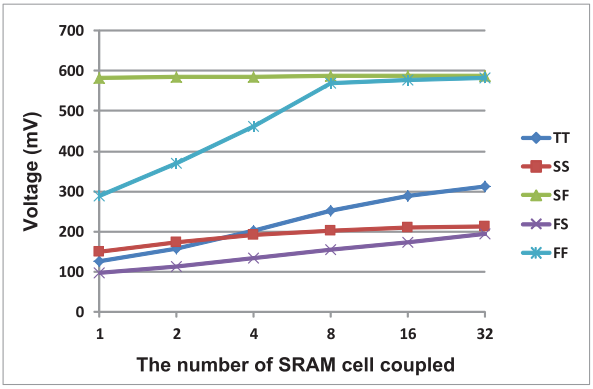

Fig. 9. v_leakage in the SRAM cell model versus different numbers of SRAM cells coupled together.

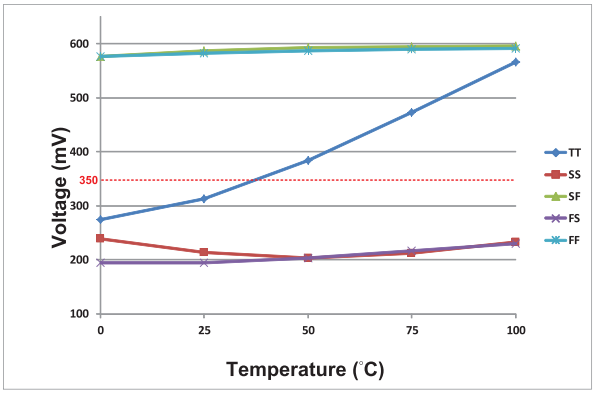

Fig. 11. v_leakage in the SRAM cell model with all PT corners by simulations.

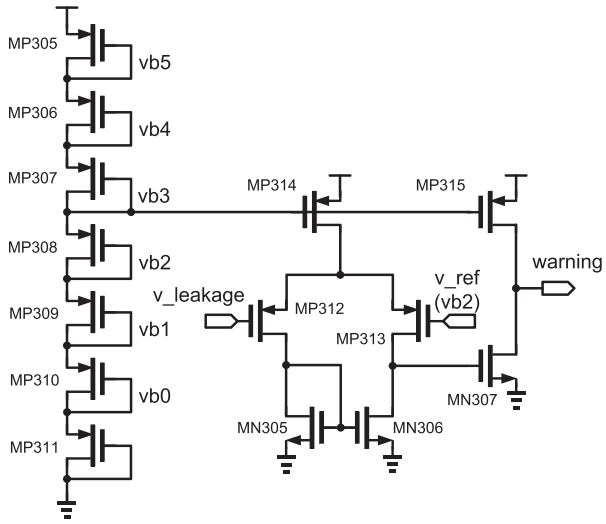

Fig. 10. Schematics of comparator.

BLb will be pulled up due to few leakage flowing from BLb to nodes Q and Qb. It may interfere the stored bit in the unaccessed SRAM cells if the time of the read 0 operation is too long. This syndrome becomes very serious when the entire circuit is operated at fast pMOS corner, since the leakage current of the pMOS (MP301 and MP302 in Fig. 5) is higher than that of nMOS (MN301 and MN302 in Fig. 5). Therefore, we have to ensure that the proposed SRAM cell will be operated correctly preferably like the scenario at TT 25 °C corner by thorough postlayout simulations. Once the output voltage of the SRAM cell model is higher than the voltage at TT 25 °C corner, as the red dashed line (350 mV) shown in Fig. 11, Compensation circuit must be activated. Then, vb2, about 350 mV, in the MOS string of comparator in Fig. 10 is selected and coupled to v_ref. Notably, v_leakage also depends on the SRAM cell size, which means we can appropriately select v_ref to be one of the six biases, vb0∼vb5, according to the size of the SRAM cell model.

C. Read Delay Compensation

Referring to Fig. 8 again, the details of the leakage compensation are as follows.

1) *Step 1:* v_leakage rises to indicate that the SRAM cell model is suffered from leakage currents.
2) *Step 2:* Once if v_leakage is higher than v_ref, comparator pulls low the warning signal.
3) *Step 3:* As soon as the warning drops, MP303 in compensation circuit is turned ON to pull-up BLb such that BL drops fast. In other words, a positive feedback is used to speed up the read access.

The leakage will slow down the entire read access, especially in the scenario of state 0 is to be read. Therefore, a compensation circuit consisting of two pMOS keepers, MP303 and MP304, speeds up the read operation such that the inverter and the following logic circuits can quickly pass the triode region to reduce power dissipation. Notably, since the BLb will be predischarged at the beginning of each read operation, this compensate operation only operates, while data bit 0 is accessed. When reading data bit 1, it stays the same. Besides, the charging speed of the proposed compensation circuit is determined by the size of MP303 and MP304. According to the current–voltage relation of the capacitor, the charging time of the proposed compensation circuit is as follows:

$$t_{\text{ch}} = \frac{C_{\text{BLb}} \times V_{\text{DD}}}{i_{\text{MP}}} \tag{1}$$

where t_{ch} is the charging time of the proposed compensation circuit, C_{BLb} is the equivalent capacitance on BLb, i_{MP} is the charging current generated by MP303 and MP304, and V_{DD} is the system voltage. Fig. 12 shows the equivalent circuit model of BLb, where MN303 is deemed as the read current source, I_{read}, when the cell is selected to be accessed. Since eight SRAM cells coupled with a share inverter, C_{BLb} is formulated as follows:

$$C_{\text{BLb}} = 7 \cdot C_{\text{load}} + C_{\text{pre}} + C_{\text{inv}}. \tag{2}$$

To ensure that the proposed compensation circuit will not interfere the normal R/W operation, the charging time is designed to be ten times smaller than the system clock period. Therefore, (1) is rewritten to be the following equation:

$$i_{\text{MP}} = C_{\text{BLb}} \times V_{\text{DD}} \times \frac{1}{10 \cdot f} \tag{3}$$

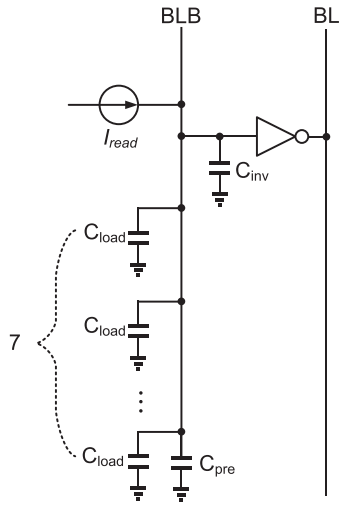

Fig. 12. Equivalent circuit model of the bitlines.

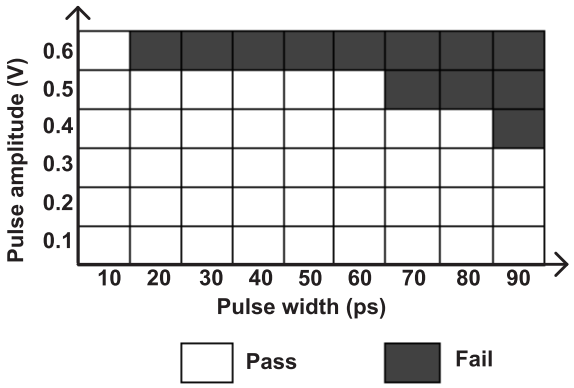

Fig. 13. DNM.

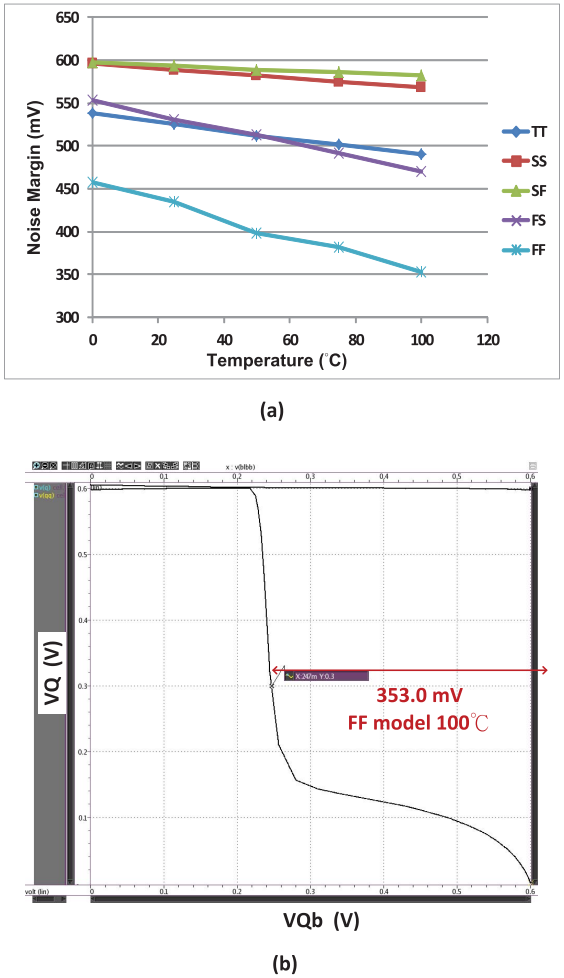

Fig. 14. SNM. (a) All-PT-corner simulation results. (b) Worst case corner simulation result (FF and 100 °C).

where f is the frequency of the system clock. Finally, the size of MP303 and MP304 can be calculated by the CMOS saturation current equation.

In this paper, since eight SRAM cells are coupled with a shared inverter, which means $2^{10}/8 = 128$ groups of compensation circuit are needed in this design.

D. Row/Column Decoder

Row and column decoders are necessary to access the selected cell. The simplest decoder is composed of NAND and NOR gates. A tree of two-input and three-input NAND gates and inverters using static CMOS logic possessing the lowest logical effort is used to build high fan-in gates in the decoders. In addition, those gates in row decoder in this design have two more inputs than those of the column decoder.

E. Build-In Self-Test

A robust testing methodology is required for memory designs to strengthen the reliability. A well-known basic memory testing methodology is the BIST circuit. The BIST circuit in this design is implemented based on March C-algorithm [11]. March C-algorithm is a popular testing algorithm, which has medium fault coverage and complexity. It can detect stuck-at fault, transition fault, address-decoder fault, and coupling fault. The complexity of March C-algorithm is $10N$, where N stands for the size of the memory. The algorithm is outlined as follows:

$$\{\Updownarrow (w0); \Uparrow (r0, w1); \Uparrow (r1, w0); \Downarrow (r0, w1); \Downarrow (r1, w0); \Updownarrow (r0)\} \quad (4)$$

where $\Uparrow$ represents up count, $\Downarrow$ represents down count, $\Updownarrow$ represents up or down count, r means read, and w means write.

III. Implementation and Measurement

A. Simulation Result

To ensure the functionality and performance of the proposed SRAM cell, Figs. 13 and 14 show the dynamic noise margin (DNM) and SNM of the proposed SRAM cell, respectively, by simulations. The DNM is ~0.3 V, which means that the state of the stored bit will not be interfered as long as the amplitude of the noise is lower than 0.3 V. Fig. 14(a) shows the all-PT-corner simulation results of

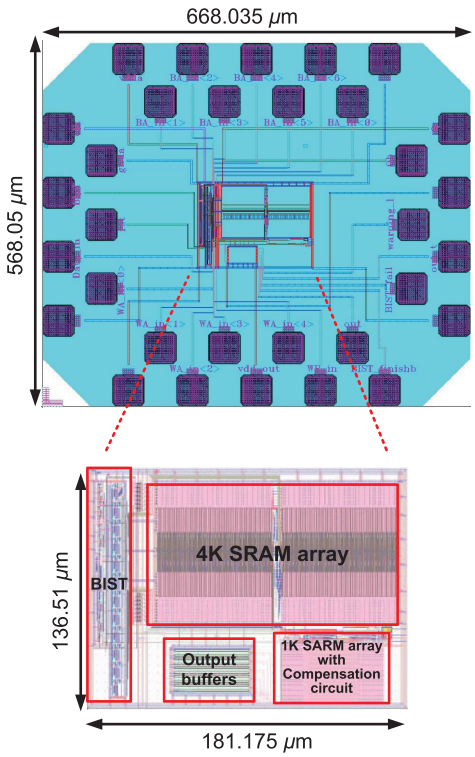

Fig. 15. Layout of the proposed design.

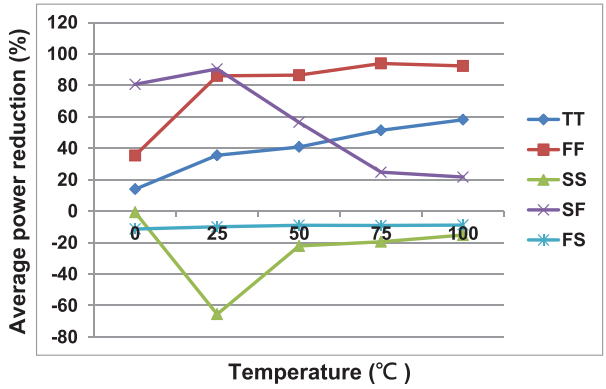

Fig. 16. Improvement of power dissipation after compensation.

the SNM. Since the proposed SRAM cell is a single-ended cell, Fig. 14(b) is not a traditional butterfly diagram, where VQ and VQb are the voltages of nodes Q and Qb, respectively. Besides, Fig. 14(b) shows the worst case of SNM, where the minimal SNM is 353 mV at FF and 100 °C corner.

Fig. 15 shows the layout of the proposed SRAM. Fig. 16 shows the average power dissipation reduction in different temperature and process corners. Notably, the power dissipation becomes bad at SS and FS corners, because the two pMOS keepers in a compensation circuit are in slow corner (S), which is turn slows down the read access. In summary, the mean average power dissipation is reduced by 27.86%. Notably, the overhead of the core area is only 3.64%.

B. Chip Measurement

Fig. 17 shows the die photo of the proposed SRAM. The chip size is 568.05 × 668.035 μm^2. Since the whole chip

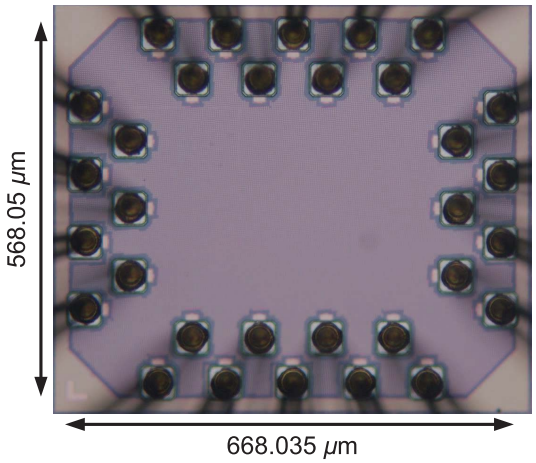

Fig. 17. Die photo of the proposed SRAM.

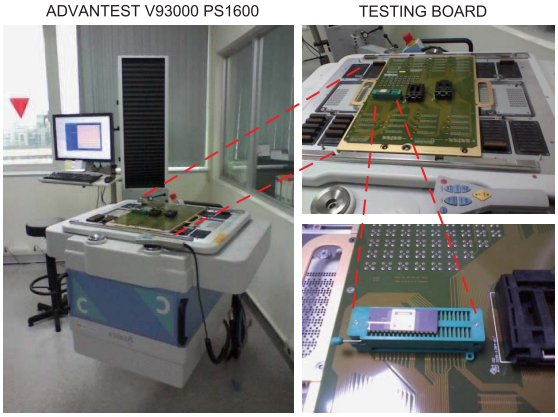

Fig. 18. Measurement environment and facility.

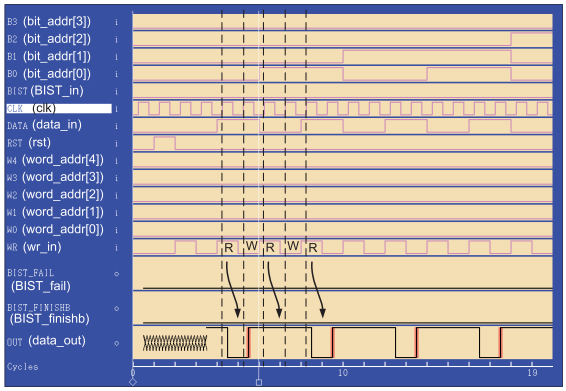

Fig. 19. Measurement result of write/read operations.

is covered by dummy metals, the core is not visible in this photo.

Fig. 18 shows the measurement environment of the proposed SRAM in the chip implementation Center, Taiwan. The instrument we used to measure the chips is a system-on-a-chip (SoC) testing machine—ADVANTEST V93000 PS1600 Automatic Test System, which supports digital, analog, and mixed-signal SoC testing. ACSII vector files, which are binary testing patterns, have to be uploaded to the server before

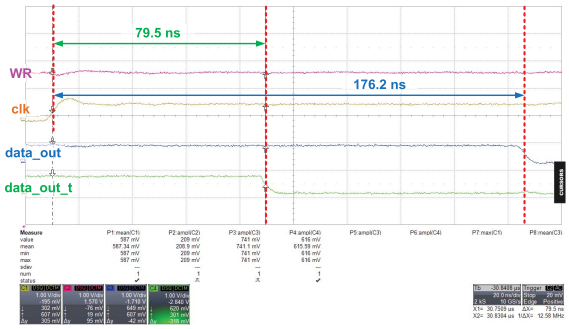

Fig. 20. Demonstration of the measured read delay compensation at 0.6 V system voltage.

TABLE I
READ DELAY MEASUREMENT RESULTS

system voltage (V)	delay_d_t (ns)	delay_d (ns)	reduction (%)
0.55	83.1	224.4	62.97
0.6	79.5	176.2	54.88
0.65	74.3	81.6	8.95
0.7	72.1	75.1	3.99
0.75	71.3	74.1	3.78
0.8	69.4	71.9	3.48
0.85	67.3	69.5	3.17

the testing. In this experiment, test files for the BIST test and address counting write/read are used for the functional test. After the file uploading, V93000 will start bonding test, short-cut test, and then SoC function test.

Fig. 19 shows the write/read function test. The shown testing process of the write/read function test is $(w0, r0)$ then $(w1, r1)$. The starting address is 12'b000000000000 and up counts every four clock cycles. Notably, the voltage level of the output pin data_out is kept logic 1 during the write access.

When our SRAM cells are suffered from leakages, the compensation circuit will be activated to compensate the delay during read 0 access. Fig. 20 shows the compensation measurement result, where data_out is the output of the uncompensated SRAM array, and data_out_t is compensated by the compensation circuit. Notably, data_out_t is 96.7 ns faster than data_out given a 0.5-MHz operating frequency and 0.6 V system voltage. Table I shows the delay measurement results given 0.55–0.8 V system voltage, where delay_d and delay_d_t denote the delays of data_out and data_out_t, respectively. The delay reduction is 62.97% at 0.55 V and 3.48% at 0.8 V. The read delay will be improved by the current injected from the system voltage when the system voltage is getting higher. Therefore, the advantage of delay reduction by our compensation circuit becomes less dominant. Notably, based on the following two reasons, the comparison between the output of the 4- and 1-kb SRAM array is considered fair.

1) Referring to Fig. 4, since the control circuit and the decoder are shared, the delay from input signals to the SRAM cells in each array is equal.
2) Fig. 21 shows the schematic of the proposed SRAM array. Regarding the load of each node, the only one difference between 4- and 1-kb SRAM array is the output load of the transmission gate (TG). The amount of the TGs in a 4-kb array is four times more than that in a 1-kb array. However, the output load of the SRAM arrays (about 20 pF, composed of pad, bonding wire, and probe) is much larger than the total parasitic capacitance of the transmission gates (about $2^9 \times 0.5$ fF in 4 kb and $2^7 \times 0.5$ fF in 1 kb) such that the total parasitic loads are negligible compared with the output load. Therefore, the output load of the transmission gate in 1- or 4-kb arrays is almost equal.

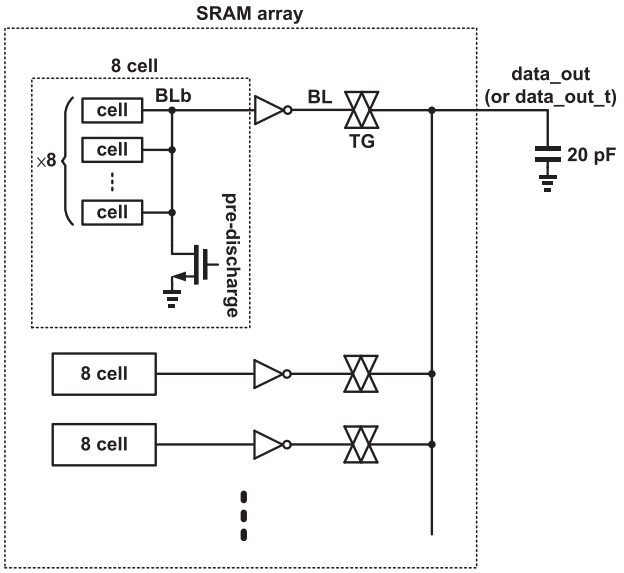

Fig. 21. Schematic of the proposed SRAM array.

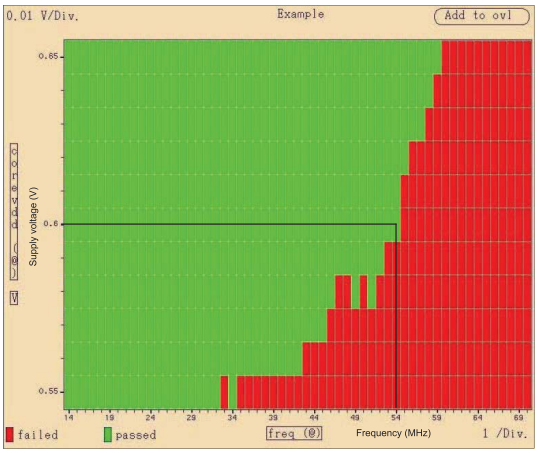

Fig. 22. Shmoo plot of the proposed SRAM.

Fig. 22 shows the shmoo plot of the proposed SRAM, where the x-axis is the operation frequency, which is between 14 and 74 MHz, and the y-axis is the supply voltage, which is 550–650 mV. Therefore, the maximum operation frequency of this design is 54 MHz provided that the system voltage is 600 mV.

To compare the proposed SRAM with prior works, a figure-of-merit (FOM) used in Table II is given

TABLE II
PERFORMANCE COMPARISON

	VLSIC'11 [12]	ISQED'12 [13]	TCAS-II'12 [14]	TCAS-I'14 [15]	TCAS-I'14 [16]	This work
Technology	40 nm CMOS	40 nm CMOS	65 nm CMOS	40 nm CMOS	40 nm CMOS	40 nm CMOS
Cell Architecture	8T	8T	9T	12T	8T	5T
Capability (kb)	1024	256	1	4	512	4+1
Word Length (bit)	16	16	16	16	64	5
Frequency (MHz)	N/A	10	0.909	11.5	200	54
Energy/access (pJ)	8.8	11.8	3.86	16	N/A	0.9411
Energy/bit (fJ/bit)	550	698.78	241.25	120	208	188.22
Core Area (μm^2)	$89\times252\times64$	900×1420	182.25×45.46	134×132	947×2810	136.51×181.16
Area/Cap. (μm^2/bit)	1.37	4.875	4.98	4.32	5.08	4.83
FOM ($\times10^3$)	0.754	3.406	1.201	0.518	1.057	0.909

as follows:

$$\text{FOM} = \frac{\text{Energy}}{\text{bit}} \times \frac{\text{Core Area}}{\text{Capability}} \tag{5}$$

which means FOM smaller, the better. Our design has the best energy/access, and the second best operating frequency.

IV. CONCLUSION

A novel read delay compensation design for 5T low supply voltage SRAM is presented in this paper. To demonstrate the effect of the proposed compensation design, two SRAM arrays, 1 and 4 kb, are realized in one single chip. The two SRAM arrays are composed of a single-ended disturbfree 5T loadless SRAM cell optimized based on PDP. The proposed compensation design is composed of a leakage current sensor and a compensation circuit. The leakage current sensor can sense the voltage drop caused by the leakage current. As soon as a warning signal issued by the leakage current sensor is over a predefined threshold, the compensation circuit speeds up the read operation. By the measurement results, given 0.6 V system voltage, the read delay is reduced 54.88% at the expense of 3.64% area overhead. The energy per access is measured to be 0.9411 pJ with a 600-mV power supply and a 54-MHz clock rate, which is the best up to date.

ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center, National Applied Research Laboratories, Taiwan, for their thoughtful chip fabrication service and EDA tool support.

REFERENCES

[1] F. Moradi, D. T. Wisland, S. Aunet, H. Mahmoodi, and T. V. Cao, "65 nm sub-threshold 11T-SRAM for ultra low voltage applications," in *Proc. IEEE Int. Syst.-Chip Conf.*, Sep. 2008, pp. 113–118.

[2] J. Chen, L. T. Clark, and Y. Cao, "Maximum—Ultra-low voltage circuit design in the presence of variations," *IEEE Circuits Devices Mag.*, vol. 21, no. 6, pp. 12–20, Jan./Feb. 2006.

[3] M. Goudarzi and T. Ishihara, "SRAM leakage reduction by row/column redundancy under random within-die delay variation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 12, pp. 1660–1671, Dec. 2010.

[4] A.-T. Do, Z.-H. Kong, K.-S. Yeo, and J. Y. S. Low, "Design and sensitivity analysis of a new current-mode sense amplifier for low-power SRAM," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 2, pp. 196–204, Feb. 2011.

[5] H. Xu, S. Jia, Y. Chen, and G. Du, "A current mode sense amplifier with self-compensation circuit for SRAM application," in *Proc. IEEE 10th Int. Conf. ASIC*, Oct. 2013, pp. 1–4.

[6] K. Agawa, H. Hara, T. Takayanagi, and T. Kuroda, "A bitline leakage compensation scheme for low-voltage SRAMs," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 726–734, May 2001.

[7] L. Ruixing, B. Na, L. Baitao, Z. Jiafeng, and W. Xiulong, "Bit-line leakage current compensation circuit for high-performance SRAM design," in *Proc. IEEE 7th Int. Conf. Netw., Archit. Storage*, Jun. 2012, pp. 109–113.

[8] D. Kim, G. Chen, M. Fojtik, M. Seok, D. Blaauw, and D. Sylvester, "A 1.85 fW/bit ultra low leakage 10T SRAM with speed compensation scheme," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2011, pp. 69–72.

[9] F. Frustaci, P. Corsonello, S. Perri, and G. Cocorullo, "Techniques for leakage energy reduction in deep submicrometer cache memories," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 11, pp. 1238–1249, Nov. 2006.

[10] S.-Y. Chen and C.-C. Wang, "Single-ended disturb-free 5T loadless SRAM cell using 90 nm CMOS process," in *Proc. IEEE Int. Conf. IC Design Technol.*, May/Jun. 2012, pp. 1–4.

[11] S. M. Al-Harbi and S. K. Gupta, "An efficient methodology for generating optimal and uniform march tests," in *Proc. 19th IEEE VLSI Test Symp.*, Apr. 2001, pp. 231–237.

[12] S. Yoshimoto *et al.*, "A 40-nm 0.5-V 20.1-μW/MHz 8T SRAM with low-energy disturb mitigation scheme," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2011, pp. 72–73.

[13] M. Terada *et al.*, "A 40-nm 256-Kb 0.6-V operation half-select resilient 8T SRAM with sequential writing technique enabling 367-mV VDD_{min} reduction," in *Proc. IEEE 13th Int. Symp. Quality Electron. Design*, Mar. 2012, pp. 489–492.

[14] M.-H. Chang, Y.-T. Chiu, and W. Hwang, "Design and iso-area V_{min} analysis of 9T subthreshold SRAM with bit-interleaving scheme in 65-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 7, pp. 429–433, Jul. 2012.

[15] Y.-W. Chiu *et al.*, "40 nm bit-interleaving 12T subthreshold SRAM with data-aware write-assist," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 9, pp. 2578–2585, Sep. 2014.

[16] N.-C. Lien *et al.*, "A 40 nm 512 kb cross-point 8 T pipeline SRAM with binary word-line boosting control, ripple bit-line and adaptive data-aware write-assist," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 12, pp. 3416–3425, Dec. 2014.

Chua-Chin Wang (SM'04) received the Ph.D. degree in electrical engineering from the State University of New York at Stony Brook, Stony Brook, NY, USA, in 1992.

He joined the Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan, where he has been a Full Professor since 1998. In 2000, he co-founded Asuka Semiconductor Inc., Hsinchu, Taiwan, which is an IC design house, and became an Executive Secretary in 2005. He was the Chairman of the Department of Electrical Engineering with National Sun Yat-sen University from 2009 to 2012. He was elevated to be a Distinguished Professor with National Sun Yat-sen University in 2010. He was nominated as the ASE Chair Professor in 2013, and elected to be the Dean of Engineering Collage in 2014. He has also been the Dean of Engineering with National Sun Yat-sen University since 2014. His current research interests include memory and logic circuit design, communication circuit design, and interfacing I/O circuits. In particular, he applies most of his research results on biomedical, memories, consumer electronics, and wireless communication applications, such as implantable ASIC/SoC, Digital Video Broadcasting–Terrestrial/Handheld and National Television System Committee TV circuits, low power memory, and high-speed digital logic.

Prof. Wang became a fellow of the Institution of Engineering and Technology in 2012. He has received the Outstanding Youth Engineer Award of the Chinese Engineer Association in 1999, and the NSC Research Award from 1994 to 1999. In 2005, he received the Best Inventor Award from National Sun Yat-sen University. In 2006, he won the Distinguished Engineering Professor Award of the Chinese Institute of Engineers and the Distinguished Engineer Award of the Chinese Institute of Electrical Engineering. He also won the Distinguished Electrical Engineering Professor Award of the Chinese Institute of Electrical Engineers in 2007, the Outstanding Paper Award of the IEEE International Conference on Consumer Electronics in 2008, and the Best Inventor Award in 2009. He has served as a Program Committee Member in many international conferences. He was the Chair of the IEEE Circuits and Systems Society (CASS) of the Tainan Chapter from 2007 to 2008. He was the Founding Chair of the IEEE Solid-State Circuits Society of the Tainan Chapter from 2007 to 2008, and the Founding Consultant of the IEEE National Sun Yat-sen University Student Branch. He is currently a member of the IEEE CASS Multimedia Systems and Applications, VLSI Systems and Applications, Nanoelectronics and Giga-Scale Systems (NG), and Biomedical Circuits and Systems Technical Committees. He was the Chair of the IEEE CASS NG Technical Committee from 2008 to 2009. Since 2010, he has been invited to be an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II. He serves as an Associate Editor of *IEICE Transactions on Electronics* and the *Journal of Signal Processing*. He was the General Chair of the 2007 VLSI/CAD Symposium. He was the General Co-Chair of the 2010 IEEE International Symposium on Next-Generation Electronics. He was the General Chair of the 2011 IEEE International Conference on IC Design and Technology, the 2012 IEEE Asia-Pacific Conference on Circuits and Systems, and the 2015 Symposium on Engineering Medicine and Biology Application.

Deng-Shain Wang was born in Taiwan in 1988. He received the B.S. and M.S. degrees in electronics engineering from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2011 and 2013, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering.

His current research interests include analog design and power IC design.

Chiang-Hsiang Liao was born in Taiwan in 1989. He received the B.S. and M.S. degrees in electrical engineering from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2012 and 2014, respectively.

His current research interests include SRAM and peripheral circuits.

Sih-Yu Chen was born in Taiwan in 1989. She received the M.S. degree in electrical engineering from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2013.

Her current research interests include analog design.