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A 30 V rail-to-rail operational amplifier

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ABSTRACT

This work presents a high-voltage (HV) operational amplifier (OPA). OPAs are widely used in signal conditioning circuits for industrial applications and integrated circuits (ICs). Particularly, in HV applications like BMS (battery management system), the signal conditioning circuits are always used to transfer voltage signal between HV domain and low voltage (LV) domain. Notably, the voltage from the HV domain could be as high as tens of volts, which might cause damages to regular silicon-based transistors. Nevertheless, since the resolution of the signal conditioning circuits depends on the output range and the operation range is determined by the input range, the input and output ranges of the signal conditioning circuits have been a key issue in the HV applications. We propose a rail-to-rail HV OPA to resolve these issues. The proposed design is implemented using 0.25 μm 1-poly 3-metal 60 V BCD process. The core area is 0.809 × 0.303 mm^2. DC gain and unit-gain bandwidth of the proposed rail-to-rail HV OPA are measured to be 41 dB and 0.3 MHz, respectively. Finally, the proposed rail-to-rail HV OPA is proven on silicon to receive any signals between 0 and 30 V and transmit a signal in the range of [0.4, 29.6] V.

1. Introduction

Electric vehicle (EV) has been recognized as a key role in the energy-shortage future. EV battery modules provide electrical energy to drive everything, including motors [1]. The battery modules of EVs have to generate outputs with tens of volts. Traditional EV BMS usually uses a monitoring integrated circuit (IC) to carry out battery module monitoring, battery module protection, and charge equalization [1–3]. Thus, the battery signal transfer devices must attain wide input and output ranges to meet such a demand. The input and output ranges of the battery signal transfer devices are determined by operational amplifiers (OPAs) of these ICs. Wide input and output ranges up to tens of volts result in difficulties of OPA design in these kinds of applications.

OPAs are widely used in signal transfer devices such as the adder, subtractor, and analog-to-digital converter (ADC) [1–8]. Many prior OPAs relied on high gain to reduce the gain error [4–6]. In [6], a high gain OPA was proposed. However, the performance of the OPA is affected by process variation [7,8]. Thus, the constant-gm designs were also proposed to reduce process variation [7,8]. Since the input and output ranges of OPA directly determine the operating range of the HV signal transfer performance, rail-to-rail OPAs are widely used to resolve these problems [9–19]. Many low-voltage (LV) rail-to-rail OPAs were proposed [9–19]. An LV operational transconductance amplifier (OTA) was proposed [10], where the output current versus the input voltage is linearized for a differential input voltage range extended from rail-to-rail. Three compact CMOS voltage-to-current converters based on OTA/common-source configurations were also reported [11], which attain rail-to-rail input and output ranges. A laser-trimmed rail-to-rail OPA with integrated laser-trimmable polysilicon resistors was disclosed to reduce the input offset voltage mismatch [15]. However, these LV designs cannot be used in HV devices, e.g., 30 V range, [4–19]. Thus, HV OPAs were proposed using HV devices [20–24]. A 36-V JFET-input bipolar OPA was implemented using SOI SiGe bipolar process [20]. The cost of the SOI process is much more expensive than standard high voltage CMOS process [20,21]. Lemkin et al. proposed a 200-V HV amplifier, which is implemented using 10-V trench-isolated CMOS process, but the input range is only 8 V [22]. The input range of the many prior HV OPAs is limited in low voltage range, which means the HV OPAs cannot be used in wide range HV applications [20–24].

In this study, we propose a rail-to-rail HV OPA, which is implemented using a 0.25 μm 1-poly 3-metal 60 V BCD process. The voltage limitation of the LV PMOS and LV NMOS is 5 V between any two terminals, as shown in Fig. 1(a) and (b), respectively. By contrast, the voltage constraints of HV PMOS and

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HV NMOS are different, as shown in Fig. 1(c) and (d), respectively. Notably, V_{GS} of the HV PMOS and HV NMOS must be lower than 5 V to prevent hazards. The proposed rail-to-rail HV OPA attains wide input and output ranges, namely attain 0–30 V and 0.4–29.6 V, respectively, given that the supply voltage is 30 V.

2. Architecture of the proposed HV OPA design

Fig. 2 shows the block diagram of the proposed rail-to-rail HV OPA consisting of 5 major blocks, i.e., a current source, a p-type input stage, an n-type input stage, a voltage limit stage, and an output stage. The proposed rail-to-rail HV OPA uses a p-type input stage and an n-type input stage to achieve a rail-to-rail input range. The output stage also provides a wide voltage range. However, wide input and output ranges must take over-voltage problems into consideration. Zener diodes and voltage limit stages are used to provide protection against the over-voltage problems in our design. The details of these function blocks are given in the following text.

2.1. n-Type input stage

As addressed earlier, V_{GS} of the HV MOSs must be limited lower than 5 V, but the VDD and input voltage might be 30 V and 0–30 V, respectively. Conventional LV OPA, therefore, cannot be directly migrated to be HV OPA. Thus, the zener diodes are used to clamp V_{GS} of the HV MOSs under 5 V. Notably, the n-well resistor is used to reduce channel length modulation effect of the HV MOSs.

- Referring to Fig. 3(a), an n-type input stage directly migrated by an LV OPA is shown, where the voltage ranges of the Vp and Vn are 0–30 V. Thus, the V_{GS}'s of HV MN4 and HV NM5 easily exceed 5 V to destroy the devices.

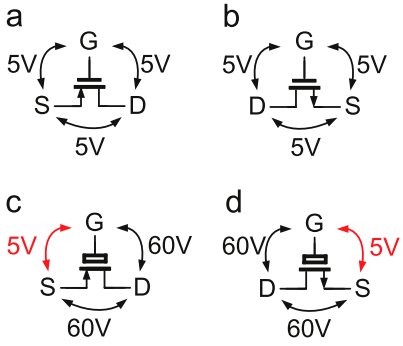

Fig. 1. Schematic of the (a) LV PMOS, (b) LV NMOS, (c) HV PMOS, and (d) HV NMOS.

- If four zener diodes are used to clamp the D–G voltage drop of HV MN4 and HV NM5, as shown in Fig. 3(b), Vn3 and Vp3 become $Vn-2\times Vz$ and $Vn-2\times Vz$, respectively, where Vz is the forward bias voltage of the zener diodes. Thus, V_{GS}'s of HV MN4 and HV NM5 are clamped to be $2\times Vz$ and $2\times Vz$, respectively. Though the problem of V_{GS} constraint is resolved, V_{DS}'s of HV MN6 and HV MN7 always drift with different input voltages. The major reason is that the channel length modulation effect becomes very serious based on Eq. (1), when the V_{DS} is not a constant.

$$I_{sat}=\frac{1}{2}uC_{ox}\frac{W}{L}(V_{GS}-\mathrm{Vth})^2(1+\lambda V_{DS}) \quad (1)$$

  where I_{sat} is the saturation current, W is the channel width, L is the channel length, C_{ox} is the oxide capacitance, u is the mobility, V_{DS} is the voltage difference between drain and source of MOS, λ is the channel length modulation coefficient, and Vth is the threshold voltage.
- To resolve the channel modulation problem, two n-well resistors are added at the source of HV MN4 and HV MN5, respectively, as shown in Fig. 3(c), to reduce V_{DS} drop.
- Vp3 and Vn3 then become as $I3\times R3+(Vn-2\times Vz)$ and $I4\times R4+(Vn-2\times Vz)$, respectively, which make V_{GS} of HV MN4 and HV MN5 vary with the input voltage.
- Thus, the currents of HV MN4, HV NM5, HV MN6, and HV NM7 will be kept constant regardless of different input voltages.

In summary, by the insertion of the zener diodes and n-well resistors, the proposed n-type stage not only attains HV input range, it also avoids the over-voltage problem and reduce the channel length modulation effect.

2.2. p-Type input stage

By a similar thought, the p-type input stage is considered as the dual design of the n-type counter part. The proposed p-type input stage is shown in Fig. 4.

2.3. HV voltage limiter

The HV voltage limiter composed of 4 PMOSs, 5 NMOSs, and 4 zener diodes is shown in Fig. 5. HVout is constrained in a high voltage range, which is written as

$$\mathrm{HVlow}\le \mathrm{HVout}\le \mathrm{HVhigh} \quad (2)$$

where HVlow is $V_{DS-MN6}+V_{DS-MN4}+4\times Vz'$, HVhigh is $VDD-V_{SD-MP5}$, Vz' is reverse bias voltage of the zener diodes. Notably, HVout is the gate drive of HV MP8 in Fig. 2. Besides, the gate drive of the MP1 is mirrored from the current source block, as

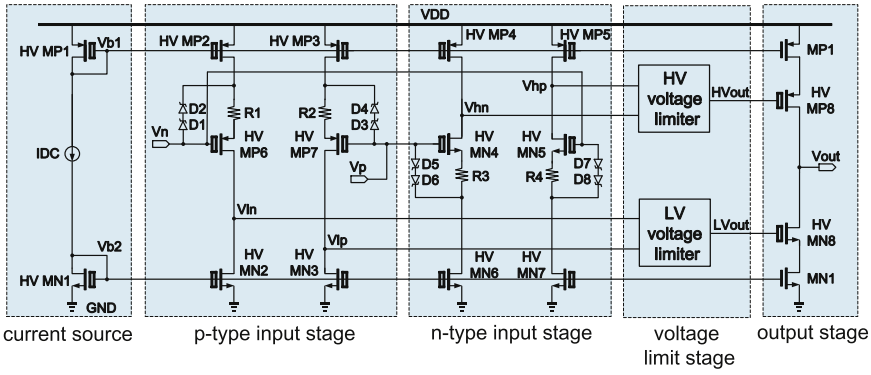

Fig. 2. Schematic of the proposed rail-to-rail HV OPA.

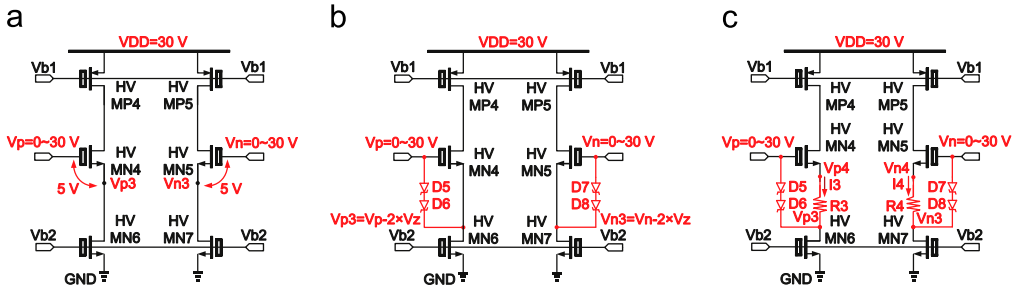

Fig. 3. Schematics of different n-type input stages (a) without 2 n-well resistors and 4 zener diodes, (b) without 2 n-well resistors, and (c) the proposed design.

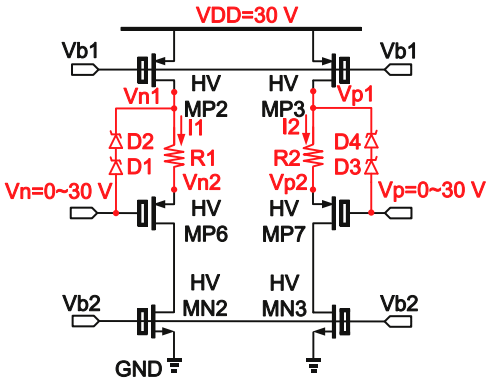

Fig. 4. Schematic of the proposed p-type input stage.

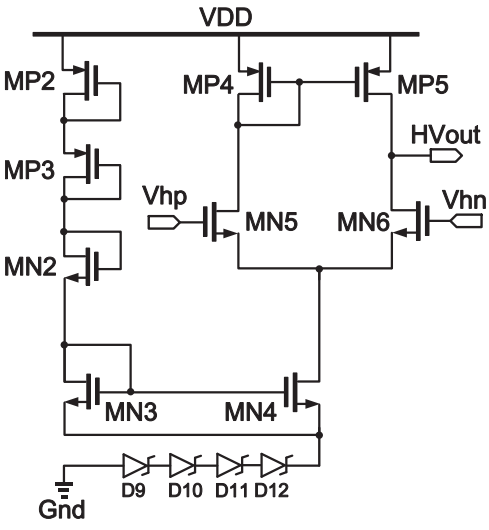

Fig. 5. Schematic of the HV voltage limiter.

shown in Fig. 2. Since the gate drive of HV MP8 is clamped, the output stage will not run into the over-voltage problem.

2.4. LV voltage limiter

The counter part of the HV limiter is the LV voltage limiter composed of 4 PMOSs, 5 NMOSs, and 4 zener diodes, as shown in Fig. 6:

$$\text{LVlow} \le \text{LVout} \le \text{LVhigh} \tag{3}$$

where LVhigh is $\text{VDD} - 4 \times \text{Vz}' - V_{\text{SD-MP8}} - V_{\text{SD-MP10}}$, LVlow is $V_{\text{DS-MN10}}$. Similarly, because the gate drive of HV MN8 in Fig. 2 is clamped as shown in Eq. (3) and the gate drive of MN1 is also mirrored from the current source block, they will not encounter any over-voltage hazard, either.

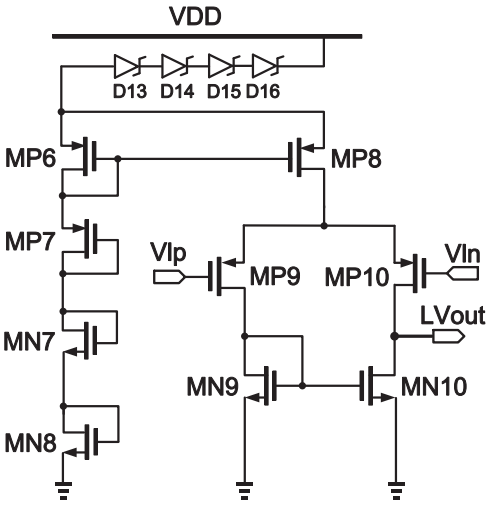

Fig. 6. Schematic of the LV voltage limiter.

2.5. Transfer function analysis

The small signal analysis of the rail-to-rail HV OPA is defined in Eqs. (4) and (5), when the p-type input stage is solely activated. Notably, the analysis of the n-type input stage operation is similar.

$$\text{Av}(s), p \approx \frac{A_{\text{DC}}, p \times (1 + w_{\text{z1}} \times s)}{(1 + w_{\text{p1}} \times s) \times (1 + w_{\text{p2}} \times s) \times (1 + w_{\text{p3}} \times s)} \tag{4}$$

$$A_{\text{DC}}, p \approx g_{\text{m,HV MP6}} \times \left(g_{\text{m,HV MP8}} \times r_{\text{o,HV MP8}} \times r_{\text{o,MP1}} + r_{\text{o,HV MP8}} + r_{\text{o,MP1}}\right) \tag{5}$$

where A_{DC}, p is the DC gain, w_{z1} is the first zero of the p-type input stage, w_{p1} is the first pole of the p-type input stage, w_{p2} is the first pole of the LV voltage limiter, w_{p3} is the first pole of the output stage, and the $g_{\text{m,[X]}}$ and $r_{\text{o,[X]}}$ denote the transconductance and the output resistance, respectively. (The [X] is the name of the MOS.) Thus, the $\text{Av}(s), p$ can be written as

$$\text{Av}(s), p \approx \frac{A_{\text{DC}}, p \times \left(1 + \frac{1}{r_{\text{o,HV MP6}} \times C_{\text{gd,HV MP6}}} \times s\right)}{\left(1 + \frac{r_{\text{o,HV MN2}} \parallel r_{\text{o,HV MP6}}}{C_{\text{tot1}} \times C_{\text{gd,HV MP6}}} \times s\right)\left(1 + \frac{1}{R_{\text{tot2}} \times C_{\text{tot2}}} \times s\right)\left(1 + \frac{1}{R_{\text{tot3}} \times C_{\text{tot3}}} \times s\right)} \tag{6}$$

where $C_{\text{gd,HV MP6}}$ is the capacitance between gate and drain of HV MP6, C_{tot1} is the overall output capacitance of the p-type input stage, R_{tot2} is the overall output resistance, C_{tot2} is the capacitance of the LV voltage limiter, C_{tot3} is the overall output capacitance of the output stage, and R_{tot3} is shown as below:

$$R_{\text{tot3}} = \left(g_{\text{m,HV MP8}} \times r_{\text{o,HV MP8}} \times r_{\text{o,MP1}} + r_{\text{o,HV MP8}} + r_{\text{o,MP1}}\right) \tag{7}$$

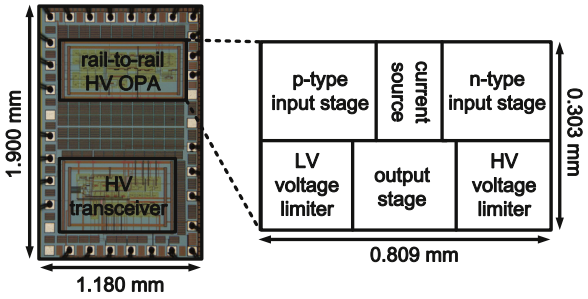

Fig. 7. Die photo of the proposed rail-to-rail HV OPA and HV transceiver.

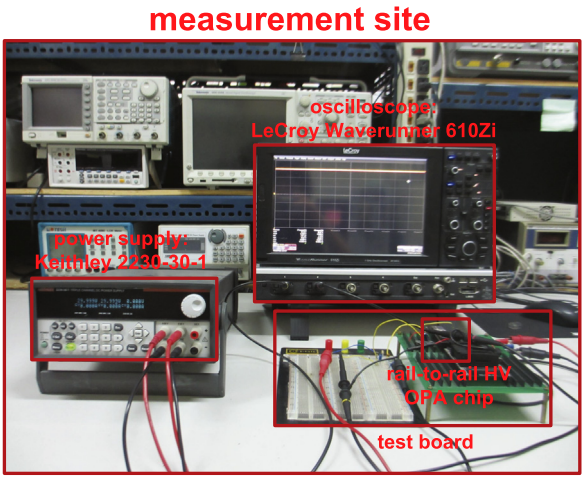

Fig. 8. Measurement site of this work.

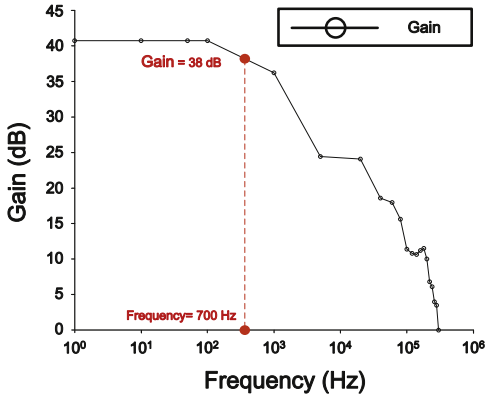

Fig. 9. Frequency response of the rail-to-rail HV OPA.

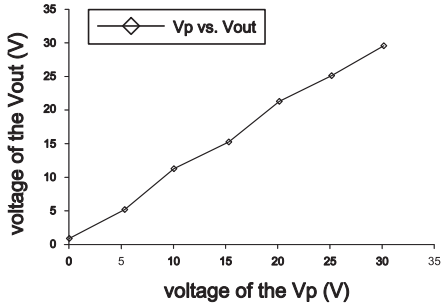

Fig. 10. Measured DC sweep of the proposed rail-to-rail HV OPA.

Table 1
Comparison between the proposed design and prior works.

	[20]	[21]	This work
Year	2011	2012	2014
Process (μm)	SOI SiGe bipolar	BCD6 SOI	0.25 μm BCD
Supply voltage (V)	40	±50	30
DC gain (dB)	N/A	40.9	41.0
GBW (MHz)	11	6.5	0.3
SR (V/μs)	20	1800	4.78
Average power (mW)	72	37	30
ICMR (V)	N/A	−3.5 to +3.5	0–30
Output swing (V)	N/A	90 (pk–pk)	0.4–29.6
Area (mm^2)	2.1	3.2	0.245

3. Implementation and measurement results

The proposed design is implemented using the 0.25 μm 1-poly 3-metal 60 V BCD process. Fig. 7 shows the die photo of the proposed rail-to-rail HV OPA and a HV transceiver, where the core area of the proposed rail-to-rail HV OPA is 0.809×0.303 mm^2. The measurement environment of this work is shown in Fig. 8. Fig. 9 shows the frequency response of the proposed rail-to-rail HV OPA, which is configured as a unit-gain buffer. DC gain and unit-gain bandwidth of the proposed HV OPA are 41 dB and 0.3 MHz, respectively. Besides, the −3 dB bandwidth is 0.07 MHz. Fig. 10 shows the DC sweep of the proposed rail-to-rail HV OPA. Notably, this design is meant to be a HV and LV interface, wide input and output ranges are top priority. Table 1 shows the comparison between the proposed rail-to-rail HV OPA design and several prior works. Notably, our design attains the widest input range, the best DC gain, the smallest power, and the smallest area.

4. Conclusion

In this paper, we propose a rail-to-rail HV OPA, which is physically implemented using a typical 0.25 μm 1-poly 3-metal 60 V BCD process. The on-silicon measurement results justify that the proposed rail-to-rail HV OPA attains rail-to-rail input range (0–30 V) and wide output ranges (0.4–29.6 V). Notably, our design attains the widest input range, the smallest area, and the lowest average power compared with the prior works.

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