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A ±3.07% frequency variation clock generator implemented using HV CMOS process

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ABSTRACT

In this paper, we propose a clock generator with a feedback TPC (temperature and process compensation) bias circuit fabricated by a high-voltage (HV) CMOS process. Particularly, the feedback TPC bias is composed of an OPA, MOS transistors and resistors, where large BJT devices are no longer needed such that it is easy to be integrated on chip with small area overhead. The feedback TPC bias circuit, including a MOS transistor, four resistors, and a differential amplifier, is used to provide temperature and process compensation. The proposed circuit design is implemented using 0.25 μm 60 V BCD process. Measurement of 10 dies in the range of 0 °C to 100 °C is carried out to verify that the worst frequency drifting error is ±3.07%.

1. Introduction

Advances in system-on-a-chip technology have made it possible to integrate a large number of products on silicon, such as microprocessors [1], digital radio [2], biomedical device [3], FlexRay-based automotive communication systems [4], and power management system [8], where a clock source with high precision is critical to the performance of all these applications. Notably, some of the above application ICs require HV processes to fabricate, e.g., automotive electronics and power ICs. Attaining a stable clock signal requires that the clock generator be immune to variations in environmental parameters, such as temperature and process variation [6–9]. What even worse is that the clock generator implemented by HV processes is long ignored. Kurita et al. presented a PLL-based clock generator designed to remove noise using a loop filter. This approach still requires an external clock which might be suffered from instability such that it is sensitive to process variation due to the analog components [1]. Zhang and Apsel modified the PLL-based clock generator using an improved control loop to compensate the process variation. However, their approach is susceptible to be temperature sensitive [2]. Digital trimming has shown certain advantage in adjusting the frequency of clock generators to resist process variation. This approach inevitably increases the overall size and cost of chips [10,11]. Zhang et al. also demonstrated a process and temperature compensated ring oscillator with an addition-based current source. However, for the low frequency applications, e.g., power management system [8] and SCS system [12], Sundaresan et al. proposed a process and temperature compensated clock generator based on a differential ring oscillator (DRO) [6] to obtain a better compensation result. This temperature compensation needs BJT transistors, which occupy large area. Even if parasitic BJT transistors are utilized, the modeling of these parasitic devices is still a problem for every high voltage process [7]. To resolve all the mentioned problems, the proposed clock generator in this paper utilizes a temperature and process compensation (TPC) feedback circuit, and a prototype is fabricated using 0.25 μm BCD high voltage CMOS process. The proposed design ensures a stable output frequency by adjusting the voltage of the differential ring oscillator according to temperature and process variation.

2. Clock generator with temperature and process compensation

The architecture of the clock generators in [4] and [6] is shown in Fig. 1. Voltage regulator provides a temperature-independent reference-regulated power source, V_{ref}. DRO generates a reference frequency using three cascaded delay stages. TPC circuit generates the compensation voltage (V_{COMP}), which is adjusted according to temperature and process variation to ensure the generation of a stable output frequency. Replica bias circuit generates a control signal (V_{CTRL}) which is a replica of V_{COMP}. Thus, DRO is indirectly biased by V_{COMP} (equal to V_{CTRL}) such that TPC circuit is isolated from the noisy

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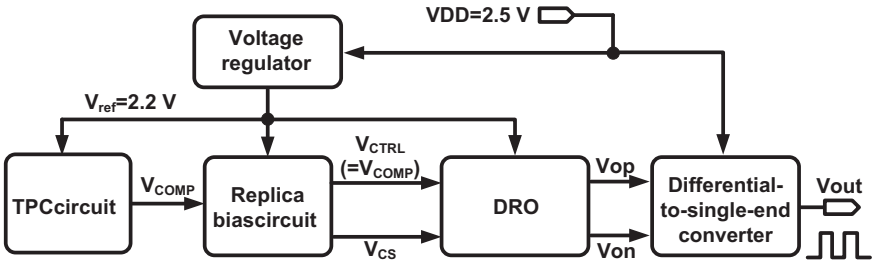

Fig. 1. Block diagram of proposed clock generator with temperature and process compensation.

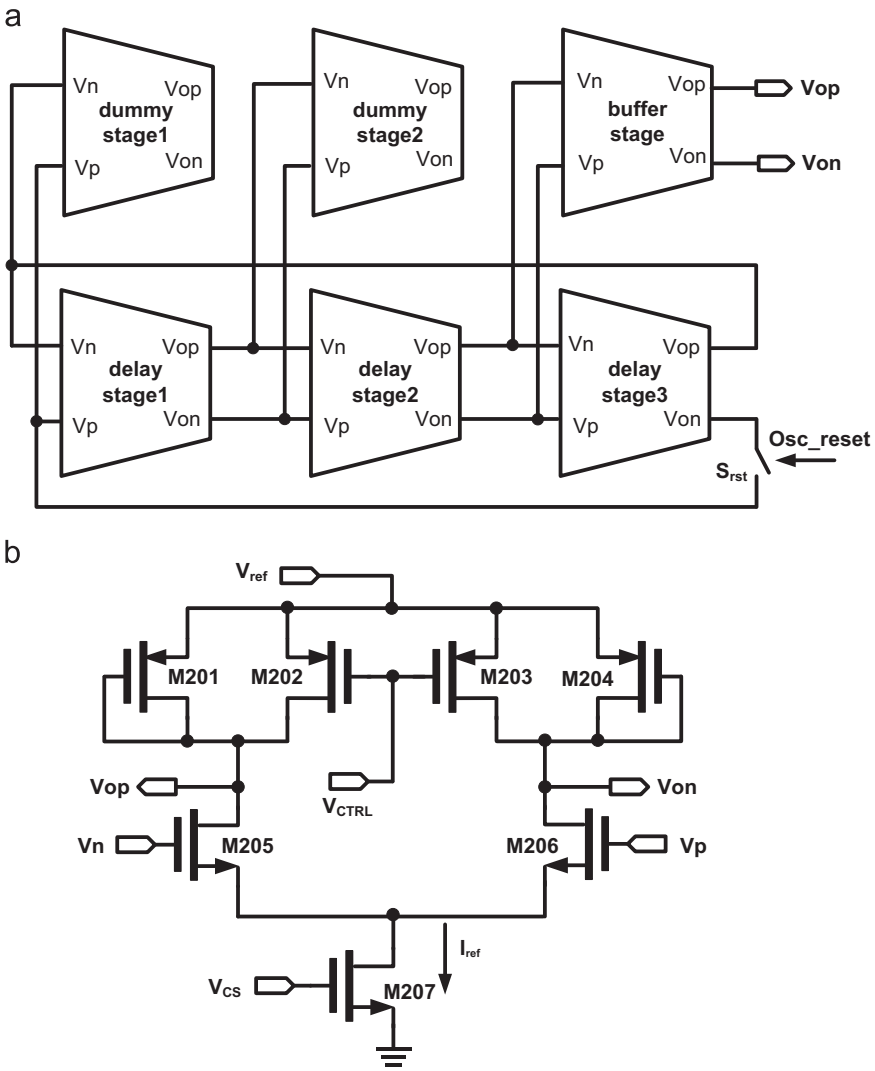

Fig. 2. Schematic diagram of (a) differential ring oscillator (DRO) and (b) delay stage [13].

oscillator. Besides, V_{CS} is the bias voltage required to generate an appropriate bias current for the delay stage in the DRO. The DRO design is based on a resistor-controlled structure. Differential-to-single-end converter receives the differential oscillating signals, Vop and Von, and converts into a single-end signal, Vout.

2.1. *Differential ring oscillator (DRO)*

Fig. 2(a) shows a block diagram of DRO, comprising three delay stages, two dummy stages, and a buffer stage [5–13]. The buffer and dummy stages were included in this circuit to eliminate asymmetric loading in the last delay stage caused by the following Differential-to-signal-end converter. The delay stage is a differential structure to reject common mode noise coupled from power lines and substrate. The buffer stage provides a large current to drive a large capacitive load. The dummy stage is used to match the load in stage1 and stage2 to that in stage3 to ensure the linearity of the DRO. Besides, the reset switch (S_{rst}) in the feedback loop of DRO is used to start the oscillation. Fig. 2(b) shows the schematic diagram of one delay stage. M203 behaves as an active load of the delay stage, providing large small-signal gain and wide oscillation swing. By simplifying the delay stage as an RC model,

the delay time of each delay stage can be given as follows:

$$t_d \approx \frac{C_0 \cdot (V_H - V_L)}{I_{ref}} \quad (1)$$

where C_0 is the equivalent capacitance at the output of each delay stage, V_H and V_L refer to the peak and valley voltages of the oscillation signals, which are equal to the voltage, V_{ref} and V_{CTRL}, respectively. I_{ref} is the tail current in each delay stage. The frequency of the output signal is determined by the number of delay stages. Thus, the frequency of output signal f can be derived as

$$f = \frac{1}{N \cdot t_d} \quad (2)$$

where N refers to the number of the delay stages. In this design, N is 3.

2.2. Replica bias circuit

Replica bias circuit in Fig. 3 provides appropriate bias voltages to the delay stages to generate independent frequencies with respect to the variations in temperature and process [5–8]. The compensation signal, V_{COMP}, is biased at the gate of the active load transistor, M208. Negative feedback from the operational amplifier, OPA2_1, is used to generate a bias signal, V_{cs}, which is coupled to the gate of M214 to provide bias current (I_{ref}) for M214 and M215. M214 and M215 have the same size, where the gate voltages are biased at the same voltage. Therefore, the bias current, I_{ref}, is mirrored to the other half of the circuit (M210, M211, M213 and M215). The critical parameters varying with temperature are the mobility of the charge carriers and threshold voltage [14]. As a result, the bias currents of M210 and M211 are the same as those of M208 and M209. Thus, the control signal, V_{CTRL}, can be used to trace the compensation signal, V_{COMP}. Besides, by replacing the saturation current equation into Eq. (2), the frequency of the output signal is derived as follows:

$$f = K_{209}\frac{(W/L)(V_{ref} - V_{COMP} - V_{T209})^2}{N \cdot C_0 \cdot (V_{ref} - V_{CTRL})} \quad (3)$$

where $K_{209} = \mu_0 C_{ox}$. W_{209} and L_{209} are the width and length of the transistor M209, respectively, while V_{T209} is the threshold voltage of M209. According to Eq. (3), the threshold voltage (V_{T209}) and reference voltage (V_{ref}) are affected by variations of temperature and process such that the frequency drift is predictable by the above parameters.

2.3. Temperature and process compensation (TPC) circuit

According to Eq. (3), a stable output frequency can only be attained by tuning the voltage, i.e., V_{CTRL}=(V_{COMP}), to compensate any deviation caused by variations of temperature and process.

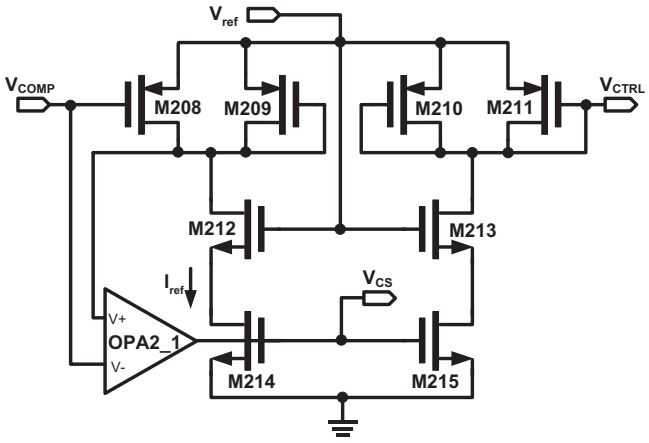

Fig. 3. Schematic of Replica bias circuit [6].

The proposed clock generator employs a feedback TPC (temperature and process compensation) circuit to provide a compensation voltage, as shown in Fig. 4 [5–8]. M216–M220 consist of a process sensor. A single-stage operational amplifier (OPA2_2) is composed of M221–M227. R201, R202, R203, R204 and M228 consist of a feedback circuit which is designed to compensate for variations of temperature and process. A description of this circuit is given in the following text.

2.3.1. Process compensation circuit

M217 and M220 consist of a current mirror pair with respect to M216 and M219. M217 is a diode-connected MOS transistor, which acts as a threshold voltage sensor. The sensed voltage, V_{CP}, can be denoted as

$$V_{CP} = V_{ref} - |V_{SG217}| \quad (4)$$

where V_{SG217} is the source-gate voltage of M217. When the process drifts from the fast to the slow corner, the threshold, V_{T217}, is increased such that the source-gate voltage, V_{SG217}, is also increased. Therefore, the voltage V_{CP} is pulled down. The reduced V_{CP} is coupled to the positive input of OPA2_2, namely, the gate drive of M224. By contrast, the negative input of OPA2_2 is coupled to the negative feedback loop output, V_{COMP}, to trace variations of V_{CP}. As previously mentioned, V_{CTRL} also traces V_{COMP} via Replica bias circuit, which means that V_{CTRL} also traces V_{CP}. Thus, we can compensate the drift of K_{209} and V_{T209} caused by process variations, as outlined in Eq. (3). In the numerator of Eq. (3), any increase in V_{T209} is canceled out by the decrease in V_{CTRL}. According to Eq. (3), the output frequency will be much faster as the corresponding compensation voltage (V_{COMP}=V_{CTRL}) drops. In addition, the decrease in V_{CTRL} in the denominator can compensate for any decrease of K_{209}. Therefore, the compensation of process variation is feasible.

2.3.2. Temperature compensation circuit

With reference to Fig. 4, the output voltage is as follows:

$$V_{COMP} = V_{CP} \cdot \left(1 + \frac{R202 + 1/gm_{228}}{R203 + R204}\right) \quad (5)$$

To determine the dependency of the compensation voltage (V_{COMP}) on the temperature (T), the partial derivative in Eq. (5) with respect to temperature, namely sensitivity [15], is attained as follows:

$$\frac{\partial V_{COMP}}{\partial T} = A \cdot \frac{\partial V_{CP}}{\partial T} + B \cdot \left(\frac{\partial R202}{\partial T} + \frac{\partial (1/gm_{228})}{\partial T}\right) - C \cdot \left(\frac{\partial R203}{\partial T} + \frac{\partial R204}{\partial T}\right) \quad (6)$$

$$A = 1 + \frac{R202 + 1/gm_{228}}{R203 + R204}$$

$$B = \frac{V_{CP}}{R203 + R204}$$

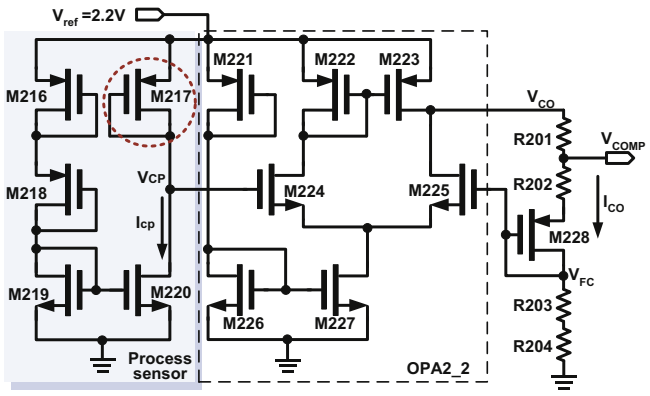

Fig. 4. Schematic of the proposed feedback TPC circuit.

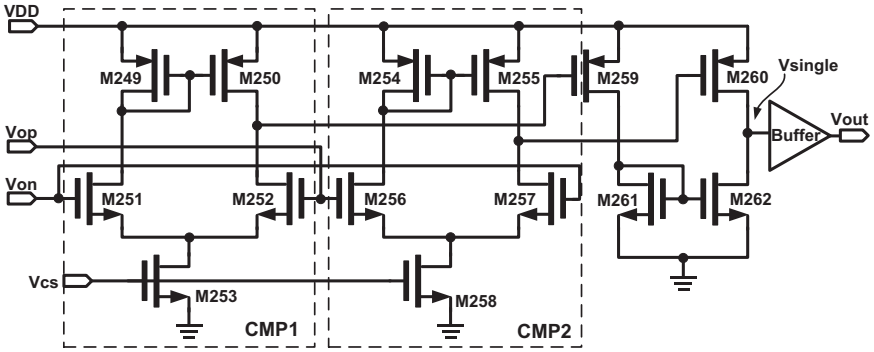

Fig. 5. Schematic of the differential-to-single-end converter.

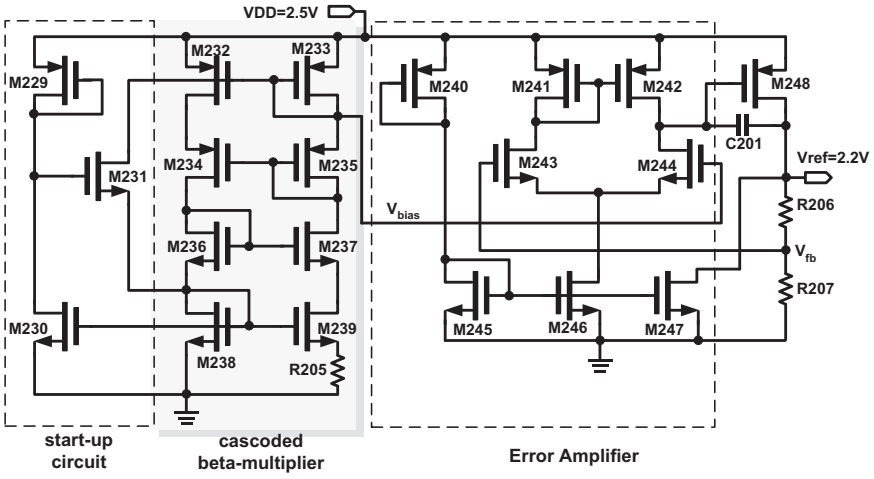

Fig. 6. Schematic of voltage regulator.

$$C = \frac{V_{CP} \cdot (R202 + 1/gm_{228})}{(R203 + R204)^2}$$

Referring to Eq. (6), the sensitivity of V_{COMP} vs. temperature is dominated by V_{CP}, the transconductance of M228 ($1/gm_{228}$) and resistors (R202, R203, R204). With reference to Eq. (6), one of the possible solutions is to make $\partial V_{comp}/\partial T$ as close to zero as possible by selecting resistors made of different materials. In this investigation, R202 and R203 are N-well resistors, while R204 is made of polysilicon. Notably, the partial derivative of N-well resistor with respect to temperature is positive. By contrast, the partial derivative of poly-silicon resistors is negative. Moreover, the conductivity value (gm) of the D-G-shorted M228 is another factor to be used for tuning in Eq. (6). However, if the proposed design is physically fabricated on silicon, the voltage of any internal node is almost impossible to adjust, including V_{CP}. Then, we select the maximum sizes of the transistor M228 and the registers R202–R204 allowed by the design rules. Finally, by using a mathematical software, MATLAB, we can derive the minimum of $\partial V_{COMP}/\partial T$ such that the compensation for variations caused by process and temperature is achieved. To verify that the compensation voltage enables the oscillator to generate a stable frequency, we derive the temperature coefficient of the frequency (TCF) of the oscillator by Eq. (3) to attain the Eq. (7) following equation:

$$TCF = \frac{1}{f}\frac{\partial f}{\partial T} = \frac{1}{f}\left[(D-E)\frac{\partial V_{ref}}{\partial T} - D\frac{\partial V_{T209}}{\partial T} - (D-E)\frac{\partial V_{CTRL}}{\partial T}\right] \quad (7)$$

$$D = K_{209}\frac{(W/L)_{209} \cdot 2(V_{ref} - V_{T209} - V_{CTRL})}{N \cdot C_0 \cdot (V_{ref} - V_{CTRL})^2}$$

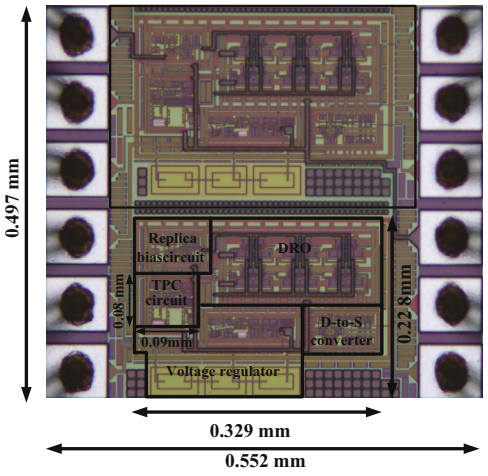

Fig. 7. Die photo of the proposed clock generator.

$$E = K_{209}\frac{(W/L)_{209} \cdot (V_{ref} - V_{T209} - V_{CTRL})^2}{N \cdot C_0 \cdot (V_{ref} - V_{CTRL})^2}$$

When the TCF is derived, the partial derivative of the compensation voltage ($V_{COMP} = V_{CTRL}$) with respect to the temperature (T), namely Eq. (6), is substituted into Eq. (7). Therefore, Eq. (8) is attained. If the generated frequency is stable, the temperature coefficient should be zero [15]. The partial derivative of frequency with respect to

temperature is zero ($\partial f/\partial T = 0$). Therefore, by carefully adjusting the tuning terms in Eq. (8), we will generate a compensation voltage (V_{COMP}) by using the positive temperature coefficient of the N-well resistor, and the negative temperature coefficient of the polysilicon resistor, respectively, in Eq. (8). The final summation can be substantially minimized and close to nullity. Therefore, an output frequency independent of temperature variation is generated.

$$\frac{\partial f}{\partial T} = (D-E)\left(\left|\frac{\partial V_{ref}}{\partial T}\right| - A\left|\frac{\partial V_{CP}}{\partial T}\right| - B\left(\left|\frac{\partial R202}{\partial T}\right| - \left|\frac{\partial(1/gm_{228})}{\partial T}\right|\right) + C\left(\left|\frac{\partial R203}{\partial T}\right| - \left|\frac{\partial R204}{\partial T}\right|\right)\right) + D\left|\frac{\partial V_{T209}}{\partial T}\right| \quad (8)$$

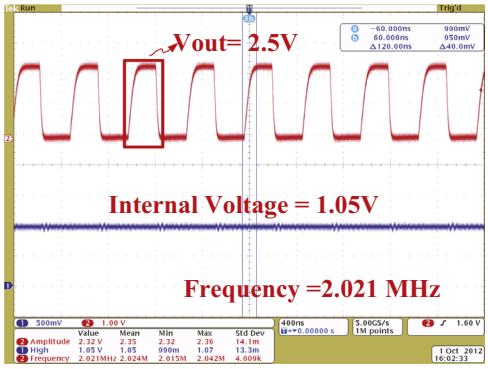

Fig. 8. Measured waveform of the output signal of clock generator.

Table 1
Frequency variation of uncompensated generator and compensated generator with TPC.

Temperature (°C)	Simulation (FF) uncompensated Error rate (%)	Simulation (FF) compensated Error rate (%)	Measurement compensated Error rate (%)
0	−19.35	2.45	3.07
10	−20.60	0.55	2.71
20	−21.75	−0.75	1.69
30	−23.60	−1.65	0.75
40	−24.90	−2.35	−0.04
50	−25.70	−2.40	−0.69
60	−27.90	−2.55	−1.20
70	−28.30	−2.35	−1.71
80	−29.70	−2.05	−1.56
90	−31.25	−1.05	−1.71
100	−32.35	0	−1.92
Average	−28.54	−1.215	1.705

2.4. Differential-to-single-end converter

Fig. 5 shows a schematic diagram of the Differential-to-single-end converter. M249–M253 and M254–M258 consist of two single stage voltage comparators, CMP1 and CMP2, respectively. The input differential oscillation signals, Vop and Von, are coupled to the negative node and the positive node of CMP1, respectively. By contrast, Vop and Von are coupled to the positive node and the negative node of CMP2, respectively. The outputs of CMP1 and CMP2 are connected to the gate of M259 and M260, respectively. With the comparison of CMP1 and CMP2 and the current mirror composed of M261 and M262, a single-end signal, Vsingle, is generated. In addition, the aspects of M259–M262 can be tuned to make the duty cycle of Vsingle close to 50%. Vsingle is then buffered and the output signal Vout is attained to enhance noise immunity.

2.5. Voltage regulator

Ensuring voltage stabilization and compensation requires a voltage regulator, which is shown in Fig. 6. The start-up circuit provides an initial DC voltage that enables the bias circuit to start up swiftly, acting only at the beginning of the circuit operation. The bias circuit in the cascode beta-multiplier provides a reference voltage source. When the currents flowing through the two current paths therein are nearly identical, the sensitivity to VDD variation is reduced, thereby generating a bias voltage (V_{bias}). This bias voltage is coupled to a single-stage high gain amplifier (Error Amplifier). Notably, two feedback resistors (R206 and R207) together with Error Amplifier consist of a quick and stable locked loop. The voltage divided by the resistors, V_{fb}, is used to detect and trace the output voltage. Generally, voltage regulators with resistance to temperature drifting employ BJTs with negative-TC characteristics. In this design, we utilize a resistor made of material $HV_{P\text{-well}}$ with the same characteristic to achieve the same function. Referring to Fig. 6, R206 and R207 are also realized using $HV_{P\text{-well}}$ resistors to consume less area and power consumption. It turns out that the temperature drifting of the output voltage in the range between 0 °C and 35 °C is less than 1.4% by the replacement of $HV_{P\text{-well}}$ material.

3. Implementation and measurement

The proposed clock generator with temperature and process compensation is fabricated using TSMC 0.25 μm 60 V BCD CMOS high voltage process. Fig. 7 shows the die photo of the proposed clock generator on silicon where the chip area is $0.497 \times 0.552\ mm^2$ (with pad). The area of TPC is $0.08 \times 0.09\ mm^2$. In other words, the proposed compensation circuit result in 10% overhead of the core area. Notably, a total of two proposed clock

Table 2
Comparison with prior works.

	This work	[17]	[16]	[5]	[2]
Year	2014	2013	2011	2010	2009
Process	0.25 μm HV BCD	0.13 μm CMOS	90 nm CMOS	0.18 μm CMOS	90 nm CMOS
Supply voltage (V)	2.5	2~3	1.0	1.8 ± 0.18	1.0
Output frequency	2.0 MHz	1 MHz	2.12–2.91 GHz	130 MHz	3 GHz
Frequency error	±3.07%	±3%	±2.6%	±4.99%	±11.7%*
Temperature range (°C)	0–100	25– 200	6.5– 56.5	0–100	−50–100
Duty cycle	48.93%	N/A	N/A	50.23%	N/A
Chip area (mm^2)	0.1356	N/A	N/A	0.1521	N/A
Core area (mm^2)	0.076	0.011	0.084	0.0042	N/A
Power consumption (mW)	0.625	0.391	3.3	2.74	2.55
FOM[a]	32.2	26.9	19.2	20.04	1.01

Note: *simulation result only.

[a] FOM = (Temp. range/Frequency error).

generators are realized on one die. One of the clock generators has a few PADs coupled to internal nodes to observe the function of corresponding subcircuits. By contrast, the other clock generator only has the required *I*/*O* PADs to avoid loading effects. To demonstrate the frequency stability with respect to temperature variation, we measure the clock generator in a thermal chamber, (X-Stream 4300). The measured output clock, Vout, is shown in Fig. 8. The output swing is 2.5 V and the frequency is 2.021 MHz. Table 1 shows the simulation results without and with compensation, and the measurement with compensation. The error rate is reduced to 3.07% (Measurement Compensated) from 32.35% (Simulation Uncompensated worst case). Table 2 compares the performance of the proposed design with several recent works. The proposed design possesses the best performance in the terms of frequency error and frequency to power ratio. In addition, the FOM (Figure-of-merit)=Temp. range/Frequency error reveals that the proposed design also attains the best result with regard to the temperature range and the frequency error. Most important of all, our design is the only one carried out using a HV CMOS process.

4. Conclusion

This paper proposes a clock generator employing a feedback TPC circuit and Replica bias to provide temperature and process compensation. We demonstrate that an on-silicon oscillator with low power consumption can be implemented using the 0.25 μm 60 V BCD process. The frequency error of the clock generator is measured in the range from 0 to 100 °C, where the worst case frequency error is ±3.07%.

Acknowledgments

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