

A 60 V Tolerance Transceiver With ESD Protection for FlexRay-Based Communication Systems

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Abstract—In this paper, a 60 V tolerance transceiver with ESD (electrostatic discharge) protection is proposed for FlexRay-based communication systems. The FlexRay transceiver comprises three protective devices, including an over-voltage detector, high-voltage ESD devices, and high-voltage diodes. The over-voltage detector is in charge of detecting bus (BP and BM) status to distinguish whether any hazard has happened. If the over-voltage detector is activated, the FlexRay transceiver must be turned off for safety. The high-voltage ESD device uses a base-floating PNP serving as a bi-directional device. Besides, it can protect the FlexRay transceiver whenever it is short-circuited in positive or negative high voltages. Notably, the high-voltage diode will eliminate the negative leakage current when negative high voltage hazards appear in FlexRay channels. An experimental prototype is implemented using a 0.18 μm CMOS mixed-signal based generation II HV BCD process. The measurement results justify the functional correctness and 60 V tolerance of the proposed FlexRay transceiver design.

Index Terms—FlexRay transceiver, high-voltage diode, high-voltage ESD device, over-voltage detector.

I. INTRODUCTION

IN RECENT years, in-vehicle systems on silicon became very popular due to the evolution of semiconductor technology [1], [2]. This trend will become more dominating when high voltage technologies are affordable, e.g., Bipolar/CMOS/DMOS (BCD) technology and HV (high voltage) CMOS technology. As a result, many electrical control units (ECUs) previously installed in automotive systems are now replaced with chips fabricated by HV processes to replace abundant discrete components. These ECUs cover telematics communication, in-vehicle networking, and X-by-wire control systems ($X = \text{steer, break, accelerate, A/V, safety, etc.}$). For the sake of safety, these transceivers in ECU are particularly required with high voltage tolerance and high current protection, e.g., a FlexRay transceiver must possess ± 60 V tolerance and 90 mA of maximum peak current when bus is short-circuited in 60 V within 400 ms [3].

Recently, many research or products regarding the FlexRay transceivers have been published [4]–[10]. For example, FlexRay transceivers fabricated using a typical 0.18 μm CMOS

process were proposed to justify their functionalities in low voltage domain [4]–[6]. According to FlexRay specification [3], they will not pass high voltage specifications, e.g., ± 60 V tolerance and $-10 \sim +15$ V common mode input voltage of the receiver (Rx). Although a FlexRay communication network with Active Star was physically implemented using ALTERA Excalibur ARM EPXA4F672C3 [7], it only verified the functionality, not the reliability and safety required by the physical FlexRay systems. Another FlexRay transceiver was implemented using a 0.35 μm CMOS high voltage technology [8], [9]. This design neither resolved the ± 60 V fault tolerance problem, nor did it address the high voltage ESD requirement. Another famous FlexRay transceiver was fabricated by SOI technology [10]. Referring to technical considerations for automotives [11], the SOI technology is not well suited for power devices, e.g., automotive chip, since the thermal conductivity of oxide is very low. In addition, the SOI technology is quite expensive and the integration is not very easy and straightforward, e.g., vertical components and ESD protection cells. By contrast, BCD technology with high power capabilities (BiMOS technology) and integration feasibility between analog and digital devices (CMOS technology) is considered a better alternative. Besides, BCD technology also has better area efficiency [12], where low voltage devices are widely used as much as possible and many external components are able to be implemented on silicon.

Another serious challenge in automotive systems is ESD protection, since multiple supply voltage systems are often needed [13]. Particularly, FlexRay transceivers must be tolerant of high voltage and temperature, i.e., $-40^\circ\text{C} \sim +125^\circ\text{C}$, besides the voltage requirements that mentioned above. Referring to [14], BCD technology provides excellent ESD protection because of the multiple layers. Moreover, several ESD protection designs are used in BCD technology which have been reported [14]–[16]. These prior works, however, could not apply to ± 60 V and bi-directional applications such that they are inappropriate for FlexRay transceivers.

Many advanced semiconductor processes have been provided to fabricate HV devices on silicon lately, e.g., 0.25 μm 1-poly 3-metal HV BCD process [17]. This particular process offers digital cell library, low voltage MOSs driven by 5 V, and several types of high voltage MOS devices. The most critical limitation is that the gate to source voltage of high-voltage MOS transistors must be limited under a low voltage ≈ 5 V. Therefore, those prior works are not easy to be directly implemented and used this HV BCD process. In this work, we propose a new FlexRay transceiver and a base-floating PNP in ESD protection to resolve all the problems we mentioned. In Section II, the proposed FlexRay transceiver is disclosed, where transmitter (Tx)

Manuscript received February 16, 2014; revised May 16, 2014, June 28, 2014, and September 25, 2014; accepted November 09, 2014. Date of publication December 08, 2014; date of current version February 23, 2015. This paper was recommended by Associate Editor A. Mazzanti.

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Digital Object Identifier 10.1109/TCSI.2014.2370192

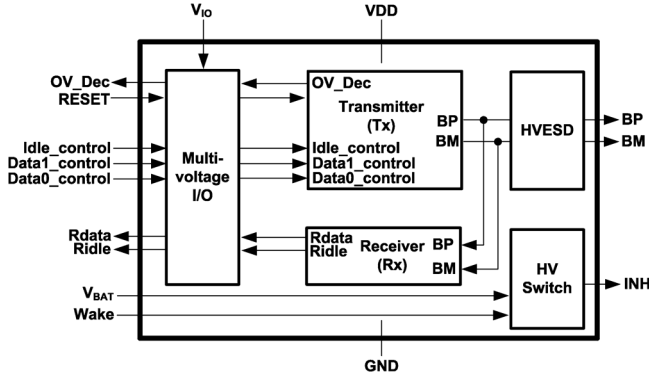


Fig. 1. Explosive view of the proposed FlexRay transceiver (FRT).

TABLE I
THE BASIC FUNCTIONS OF FLEXRAY TRANSCEIVER

State	S0	S1	S2	S3
Wake	0	0	1	1
RESET	1	0	0	0
Idle_control	0	1	0	0
Data1_control	0	0	0	1\0
Data0_control	0	0	0	0\1
BP/BM	0	0	Idle (2.5 V)	1\0
Rdata	0	0	0	1\0
Ridle	0	1	1	0
INH	0	0	V _{BAT}	V _{BAT}

S0: RESET is activated to reset the FlexRay transceiver

S1: FlexRay transceiver is in the sleep mode.

S2: FlexRay transceiver is in the standby mode.

S3: FlexRay transceiver is in the normal mode.

and receiver (Rx) are included. Particularly, an over-voltage detector is in charge of detecting the abnormal voltage status on bus (BP and BM). Notably, the proposed high-voltage diode can eliminate the negative leakage current. In Section III, the structure of the base-floating PNP is shown and analyzed, which is a bi-directional component. The device can protect the FlexRay transceiver whenever it is exposed to short-circuited hazards at the presence of a positive or negative high voltage. In Section IV, we demonstrate the measurement results of the proposed FlexRay Tx/Rx. The performance comparison between our proposed design and prior works is also discussed. Finally, a brief conclusion is given in Section V.

II. ARCHITECTURE OF 60 V TOLERANT FLEXRAY TRANSCEIVER

Fig. 1 shows the proposed FlexRay transceiver (FRT) in this work, including Multi-voltage I/O, HV switch, Transmitter (Tx), Receiver (Rx), and high-voltage ESD (HVESD). There are four states describing the functionality of the FlexRay transceiver, as shown in Table I, where Idle_control, Data1_control, and Data0_control are used to drive the Tx for transmitting data on bus (BP and BM). The Wake signal will turn on the HV Switch to drive off-chip power devices, including DC/DC converters. Multi-voltage I/O is in charge of converting these input signals into the voltage range between VDD and GND by adjusting V_{IO} . Notably, the Rx monitors the bus status to distinguish whether the data arrive or not. Most important of all, these high-voltage devices are protected by HVESD against electrostatic hazards. The functions of each block are described as follows:

A. Transmitter (Tx)

A delay-based transceiver with an over-voltage detector utilizing a LVDS-like transmitter design [18], [19] is proposed in this work, as shown in Fig. 2. When Idle_control is activated, BP and BM are locked on 0 V. Otherwise, BP and BM are pulled up to 2.5 V. Data0_control and Data1_control drive the high-voltage MOSs, i.e., MLH0~MLH3, MLL0~MLL3, MRH0~MRH3, and MRL0~MRL3. For instance, if Data0_control is 1 and Data1_control is 0, BP is pulled down and BM is pulled high such that a logic “0” is transmitted over the bus.

Notably, the transitions of high-voltage PMOS transistors and NMOS transistors could not be synchronized perfectly in prior works [18]. A large current will be generated on bus (BP and BM), if they are accidentally turned on at the same time, namely “glitch.” These delay buffers, i.e., delay buffer_0~delay_buffer_3, are added to resolve this problem. Besides, the high-voltage PMOS and NMOS transistors are equally divided into many transistors, e.g., MLH0~MLH3. Because the size of each transistor is relatively small and the transition time of gate drive thereof also is equally delayed, no large current will be introduced on bus. Therefore, the glitch will be apparently eliminated by properly delaying the transition time of each high-voltage MOS. The functions of the over-voltage detector and high-voltage diodes are described as follows:

1) *Over-Voltage Detector*: According to FlexRay specifications, BP and BM are required with high voltage tolerance, i.e., maximum ± 60 V. Therefore, the over-voltage detector is needed to distinguish whether BP or BM is normally operating. If the voltage of BP/BM is higher than VDD or lower than GND, the over-voltage detector is activated to turn off all high voltage MOSs. The over-voltage detector consists of a positive high voltage block, a negative high voltage block, and an over-voltage decider, as shown in Fig. 3. In the positive high voltage block, there are two symmetrical strings generating OV_V1 and OV_Vref1, respectively, where the only difference of these strings is the supply voltage. When the voltage of BM/BP is higher than VDD, OV_V1 will be larger than OV_Vref1. By contrast, When the voltage of BM/BP is lower than GND in negative high voltage part, OV_V2 will be smaller than OV_Vref2. Therefore, the over voltage decider compares these reference voltages to distinguish whether BP or BM is kept safely within VDD and GND.

2) *High-Voltage Diode*: The high-voltage diode is used to block any high voltage and reverse leakage current. For example, when BP or BM is short-circuited in a positive high voltage, the upper high-voltage diodes are used to block any high voltage, and then the bottom high-voltage diodes and MOSs are turned off by the over-voltage detector. By contrast, when BP or BM is short-circuited to a negative high voltage, a large leakage current will be introduced if the traditional diodes are used. The reason is that the traditional diode is implemented by P-N junction such that it is still turned on because the P node is coupled to the negative voltage. Therefore, the high-voltage diode is required to eliminate the leakage current by implanting the NBL layer as the isolation ring, as shown in Fig. 4, where the cross-section view of this diode is disclosed. It is mainly composed of an N- well surrounded with P- well implant layers to prevent the leakage current flowing into the substrate.

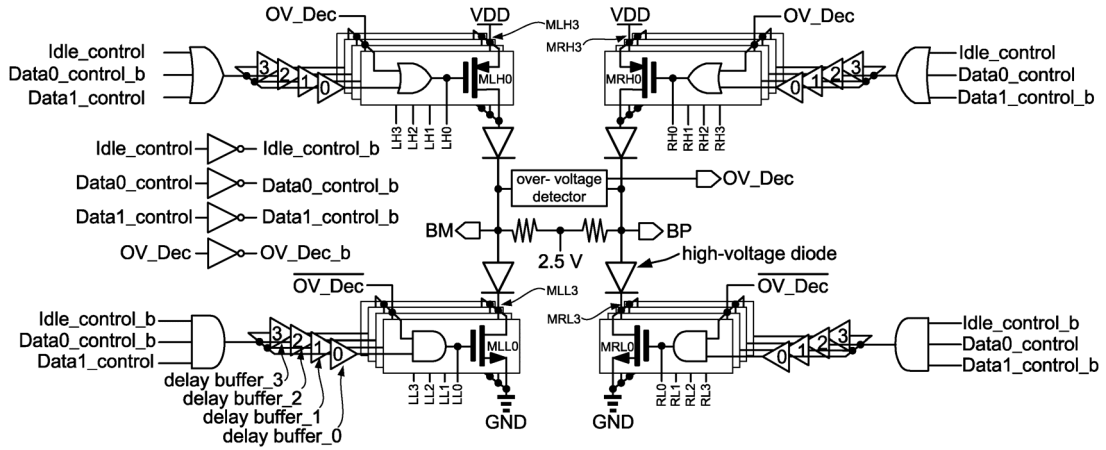


Fig. 2. Proposed transmitter (Tx) schematic.

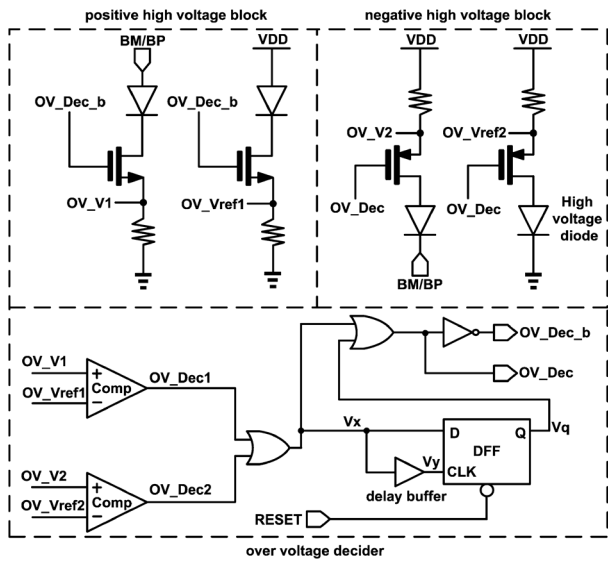


Fig. 3. Over-voltage detector schematic.

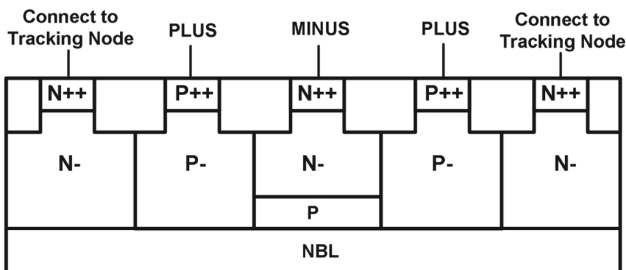


Fig. 4. Cross-section view of high-voltage diode.

Moreover, the NBL layer is internally connected to a tracking system, guaranteeing that the voltage of this well always is higher than that of the BP/PM and the substrate. With these two added layers, the diode can sustain high input voltages while maintaining a low leakage current.

B. Receiver (Rx)

FlexRay specifications require that the input common voltage of Rx is $-10 \sim +15$ V. Therefore, Rx has to convert the BP and BM into the input range of the following comparators, i.e., Comp_1~Comp_3, as shown in Fig. 5. The converting circuits consist of OTA, R1~R4, and a voltage clamp, generating BP_x

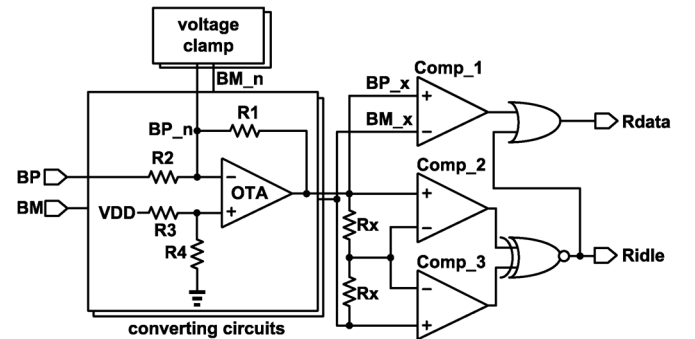


Fig. 5. Proposed receiver (Rx) schematic.

and BM_x voltage references. BP_x is constrained by the following equation:

$$BP_{-x} = VDD \times \frac{R4}{R3 + R4} \times \left(1 + \frac{R1}{R2}\right) - BP \times \frac{R1}{R2} \quad (1)$$

where the first term at the right hand side is adjusted as a common voltage. The conversion function is based upon the linear mapping from $-10 \sim +15$ V to $0 \sim 5$ V such that the ratios of R1/R2 and R3/R4 can be easily calculated. Similarly, BM_x can also be generated by the converting circuits. Therefore, the three comparators (Comp_1~Comp_3) are able to easily recognize the data status on bus, where the comparators are based on a three-stage comparator circuit [20]. Comp_1 is used to determine if the received data is low or high on bus. Comp_2 and Comp_3 are in charge of distinguishing whether any data are transmitted on bus.

To protect the receiver against high voltage hazards in Fig. 5, the voltage clamp is used to clamp the voltage of BP_n and BM_n. Referring to Fig. 6, the left MOS string is used to generate reference voltages, which are " $VDD - V_{th_{M603}}$ " and " $V_{th_{M606}}$," respectively. Therefore, M601 and M602 must be turned off when BP_n is within " $VDD - V_{th_{M603}} + V_{th_{M602}}$ " and " $V_{th_{M606}} - V_{th_{M601}}$." Assume all MOS transistors have same threshold voltage, M601 and M602 must be turned off when BP_n is within VDD and GND. For example, when BP is short-circuited in a positive high voltage, the voltage of BP_n is also raised over VDD such that M602 of voltage clamp is turned on to pull down the voltage of BP_n. By contrast, when BP is short-circuited in a negative high voltage, BP_n also can be clamped. Therefore, high voltages at BM or BP will be clamped

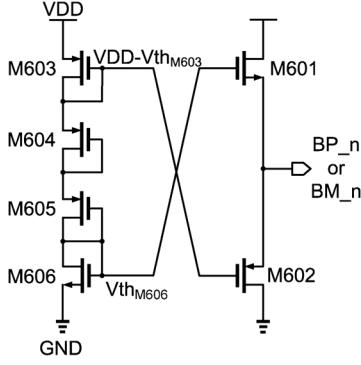


Fig. 6. Voltage clamp schematic.

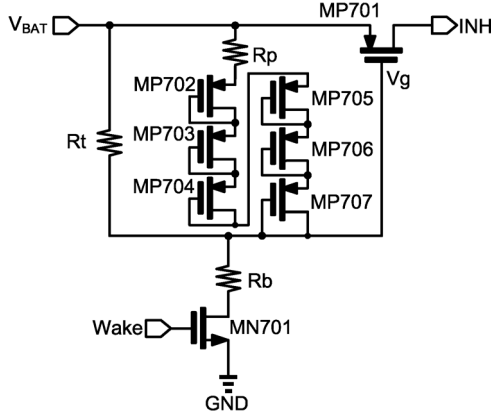


Fig. 7. The HV Switch schematic.

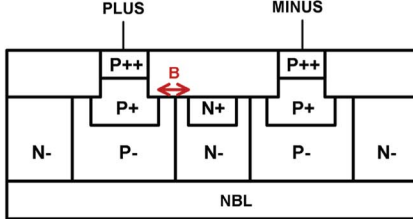


Fig. 8. Cross-section view of high-voltage ESD (HVESD).

such that the terminals of the OTAs and comparators won't be threatened.

C. HV Switch

The HV Switch in Fig. 1 is composed of three resistors (R_t , R_b , and R_p), MN701, and MP701~MP707, as shown in Fig. 7, where MN701 and MP701 are HV devices. Notably, V_{gs} of the HV devices must be smaller than 5 V. The V_{gs} of MN701 is driven by Wake signal, which is a digital signal with a swing from 0 to 5 V. Therefore, MN701 is ensured safely without any over-voltage hazard. To prevent the over-voltage damage of MP701, the voltage difference between V_{BAT} and V_g must be smaller than 5 V. Because V_g is generated by V_{BAT} , we separate the voltage range of V_{BAT} into two scenarios, i.e., low voltage mode ($V_{BAT} \leq 5$ V) and high voltage mode ($V_{BAT} > 5$ V).

In the high voltage mode, V_g is clamped by R_p and MP702~MP707. In other words, V_g is constrained by the following equation:

$$V_g = V_{BAT} - (V_{Rp} + V_{thpMP702} + V_{thpMP703} + V_{thpMP704} + V_{thpMP705} + V_{thpMP706} + V_{thpMP707}) \quad (2)$$

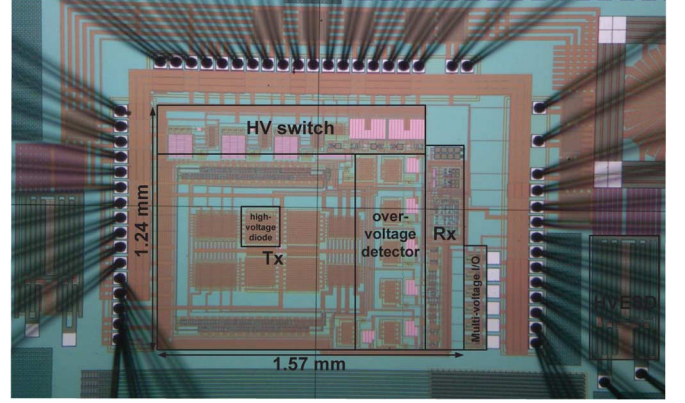


Fig. 9. Die photo of the proposed FlexRay transceiver.

where V_{Rp} is the voltage drop of R_p and $V_{thpMP702} \sim V_{thpMP707}$ are the threshold voltage of MN702~MN707, respectively. $V_{gsMP701}$ (V_{gs} of MP701) is then written as

$$V_{gsMP701} = V_{Rp} + V_{thpMP702} + V_{thpMP703} + V_{thpMP704} + V_{thpMP705} + V_{thpMP706} + V_{thpMP707} < 5 \text{ V} \quad (3)$$

where V_{Rp} is negligible because R_p is used to limit the peak current of V_{BAT} such that the MP702~MP707 are prevented from large current hazards.

In the low voltage mode, V_g is generated by R_t and R_b . Therefore, V_g is derived as follows:

$$V_g = V_{BAT} \times \frac{R_b}{R_t + R_b} \quad (4)$$

Assume R_t is equal to R_b , and V_g is the half of V_{BAT} . Thus, V_{gs} of MP701 is half of V_{BAT} (≤ 2.5 V). Therefore, MP701 is also ensured safely without any over-voltage hazard. Besides, R_t and R_b can be determined based on the requirement of power dissipation. For instance, large R_t and R_b shall reduce dc current to save power.

III. HIGH-VOLTAGE ESD (HVESD)

FlexRay specifications demand that bus (BP and BM) pins must pass high level ESD as well as to sustain low leakage current for both high positive and negative voltages, e.g., ± 60 V. Traditional ESD devices are usually designed to use in a single direction, e.g., power clamp and I/O ESD cell [14]–[16]. In this work, a high-voltage and bi-directional ESD device is proposed to protect BP and BM pins. As shown in Fig. 8, this ESD device is composed of P- and N- wells. P+ and N+ wells are added to adjust the breakdown voltage. N- well is floating for the bi-directional design. Both PLUS and MINUS nodes provide discharging paths for the ESD current. With a moderate B value in Fig. 8, the proposed ESD device can sustain 60 V breakdown voltage. Besides, this base-floating PNP structure has high holding characteristic and low on-resistance, providing circuit designers a better design window.

IV. IMPLEMENTATION AND MEASUREMENT

The proposed design is implemented using a 0.18 μm CMOS mixed-signal based generation II HV BCD process to justify the functionality as well as the reliability. Fig. 9 shows the die photo of the proposed FlexRay transceiver on silicon. The core area is

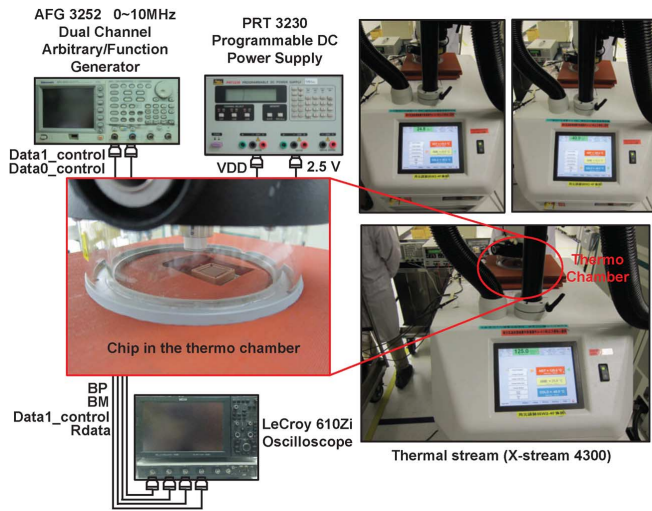


Fig. 10. Measurement settings of the proposed system.

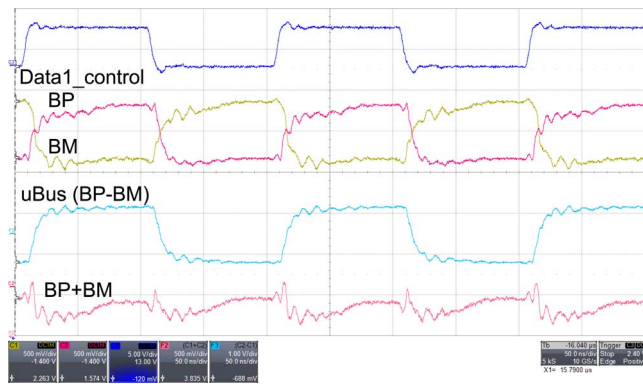


Fig. 11. Measurement waveforms of Tx.

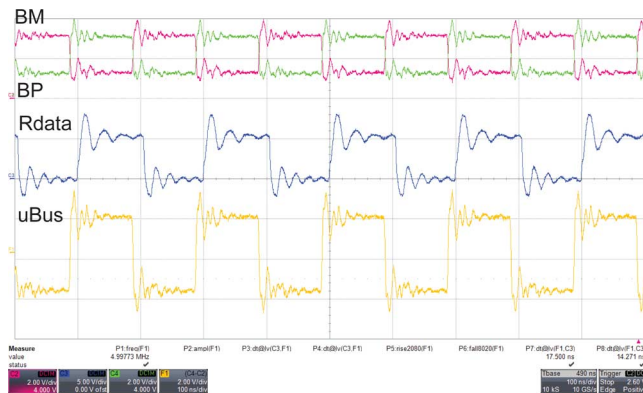


Fig. 12. Measurement waveforms of Rx.

$1.57 \times 1.24 \text{ mm}^2$. Fig. 10 shows the measurement settings for thermo test between $-40^\circ\text{C} \sim +125^\circ\text{C}$. Fig. 11 shows the physical on-silicon measurement waveforms of the proposed Tx, where Data1_control and Data0_control are a pair of digital differential signals. The measurement results show a very good symmetry behavior on BP and BM, where uBus is the difference between BP and BM. The measurement results of Rx are shown in Fig. 12. The comparison between our design and FlexRay specification in different temperature is listed in Table II. All functions are confirmed to FlexRay specifications.

Referring to [21], the output signals of a push-pull type transmitter, e.g., the proposed Tx, will likely become asymmetrical after physical implementation such that a common mode

TABLE II
MEASUREMENT RESULTS OF THE TX/RX IN DIFFERENT TEMPERATURE

FlexRay Tx Specification	-40°C	25°C	$+125^\circ\text{C}$
Absolute value of uBus, while sending	1517 mV	1282 mV	1081 mV
Transmitter delay, negative edge	15.014 ns	17.227 ns	20.047 ns
Transmitter delay, positive edge	18.634 ns	20.309 ns	23.957 ns
Transmitter delay mismatch	3.62 ns	3.082 ns	3.91 ns
Fall time of uBus	10.032 ns	12.273 ns	13.933 ns
Rise time of uBus	12.713 ns	13.581 ns	16.826 ns
Transition time mismatch	2.618 ns	1.308 ns	2.893 ns
Receiver delay, negative edge	16.788 ns	17.5 ns	24.302 ns
Receiver delay, positive edge	14.172 ns	14.271 ns	21.835 ns
Receiver delay mismatch	2.616 ns	3.229 ns	2.467 ns

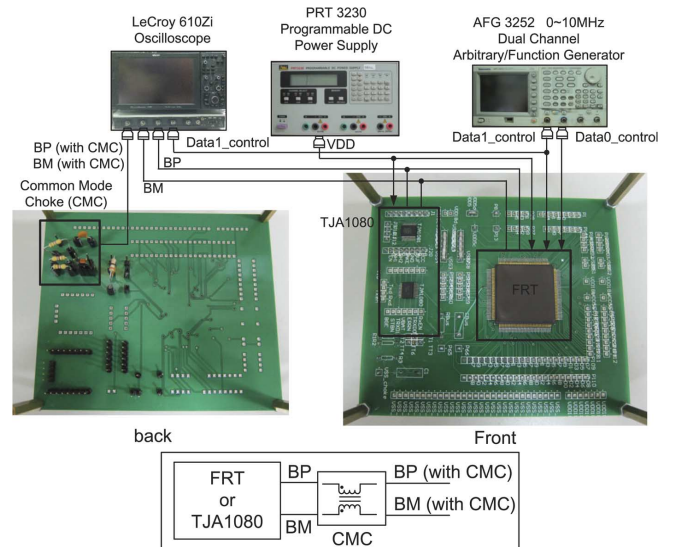


Fig. 13. Measurement setting of our FRT and NXP TJA1080 with common mode chokes (CMC).

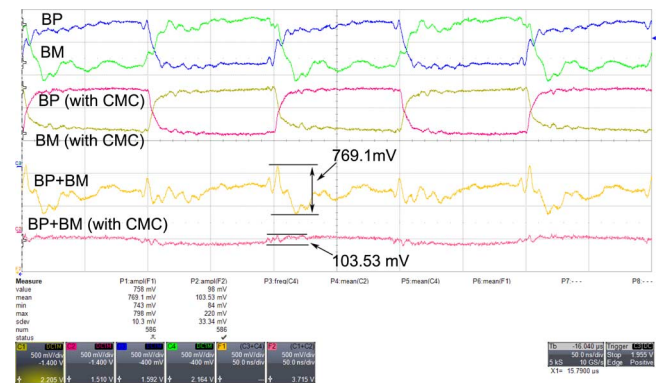


Fig. 14. Measurement results of our FRT with and without CMC.

voltage noise is generated. To justify the emission and immunity of the proposed design, a common mode choke (CMC) is used to filter the common mode voltage noise. According to the FlexRay specification [22], the resistance and inductance of CMC are $< 1.5 \Omega$ and $100 \mu\text{H}$, respectively. Therefore, a commercially available CMC for FlexRay-based systems is used to verify the electromagnetic compatibility (EMC) for differential transmission, namely ACT45R-101-2P [23]. The measurement setting of our FRT and NXP TJA1080 with CMC is shown in Fig. 13. Notably, NXP TJA1080 has been renowned so that it is used as a golden sample here. Fig. 14 shows the measurement results of FRT with and without CMC, where BP and BM are outputs of FRT without CMC, and BP (with CMC)

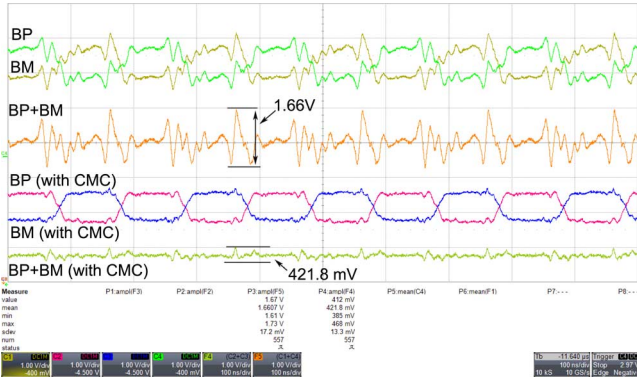


Fig. 15. Measurement results of NXP TJA1080 with and without CMC.

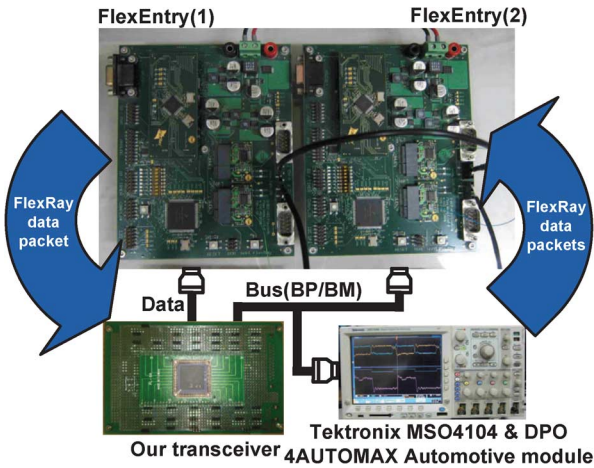


Fig. 16. Measurement setting with a FlexRay FlexEntry development board.

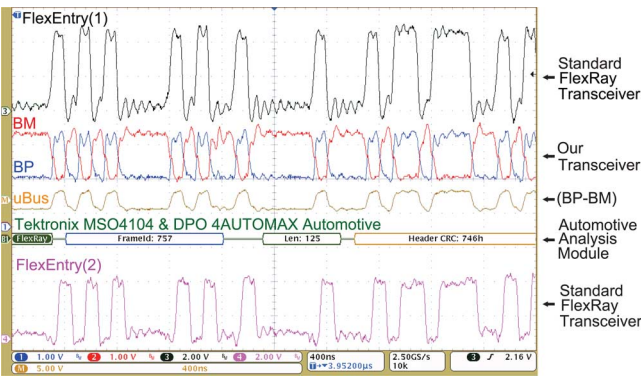


Fig. 17. Measurement results with a FlexRay FlexEntry development board and DPO 4AUTOMAX automotive module.

and BM (with CMC) are outputs of FRT with CMC. Obviously, the amplitude of common mode voltage noise is reduced from 384.55 mV (0.7691/2 V) to 51.765 mV (0.10353/2 V). To make a fair comparison, the common mode voltage noise of NXP TJA1080 is also measured, as shown in Fig. 15. According to the measurement results, the common mode voltage noise of our proposed FRT is lower than NXP TJA1080, namely 51.765 mV vs. 210.9 mV (0.4218/2 V).

A FlexRay FlexEntry development board is used in the experiment to set up a FlexRay system test environment, as shown in Fig. 16. The FlexEntry(1) generates standard FlexRay packet frames to the proposed transceiver, and then Tx in our transceiver transmits the received data packets to FlexEntry(2) via Bus. The oscilloscope shows the BP and BM signals decoded

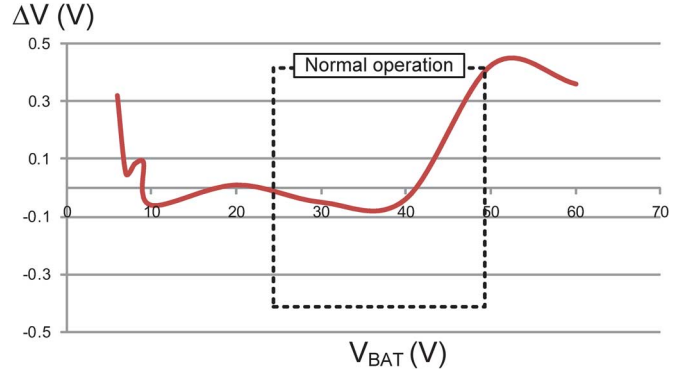


Fig. 18. Measurement results of the HV Switch given different V_{BAT} and 9.1 K Ω load resistors (RL).

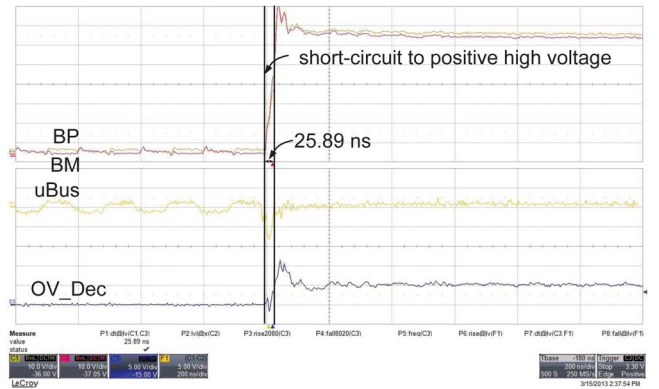


Fig. 19. Measurement results of the over-voltage detector given positive high voltage on BP and BM.

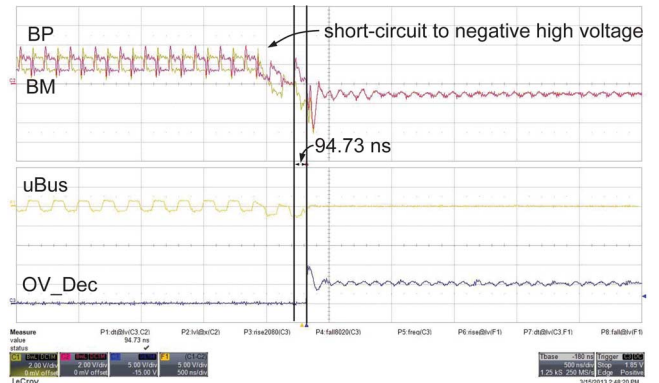


Fig. 20. Measurement results of the over-voltage detector given negative high voltage on BP and BM.

by DPO 4AUTOMAX Automotive module and FlexEntry(2). As expected, all measurement results are matched, as shown in Fig. 17.

Fig. 18 shows the error distribution with different V_{BAT} and 9.1 K Ω load resistors (RL) present at INH in Fig. 1. In the normal operation range ($24\text{ V} \leq V_{BAT} \leq 48\text{ V}$), the worst-case voltage between V_{BAT} and INH (ΔV) is smaller than 0.5 V at $> 200\ \mu\text{A}$ current load. According to FlexRay specifications, the ΔV must be less than 1 V at $200\ \mu\text{A}$ current load. Therefore, our proposed HV Switch is confirmed to such a FlexRay specification. Regarding the reliability and safety, the over-voltage detector is tested, as shown in Fig. 19 and Fig. 20, respectively. Referring to Fig. 19, when BP or BM is short-circuited in a positive high voltage, the OV_Dec is activated to turn off Tx after 25.89 ns. By contrast, Fig. 20 shows the scenario that BP and

TABLE III
COMPARISON OF THE PROPOSED DESIGN AND PRIOR WORKS

FlexRay Tx/Rx Specification	This work	[5]	[4]	[24]	[10]	FlexRay Specification
Year	2014	2012	2010	2010	2007	2010
Absolute value of uBus, while sending	1282 mV	950 mV	1380 mV	4000 mV	1600 mV	600~2000 mV
Absolute value of uBus, while Idle	≈ 17 mV	≈ 0 mV	≈ 30 mV	30 mV	25 mV	0~30 mV
Transmitter delay, negative edge	17.227 ns	14.8 ns	13.32 ns	50 ns	31 ns	< 75 ns
Transmitter delay, positive edge	20.309 ns	16.4 ns	13.29 ns	50 ns	32 ns	< 75 ns
Transmitter delay mismatch	3.62 ns	1.6 ns	0.029 ns	4 ns	1 ns	< 4 ns
Receiver delay, negative edge	16.788 ns	36.8 ns	9.492 ns	80 ns	28 ns	< 75 ns
Receiver delay, positive edge	14.172 ns	37.2 ns	9.065 ns	80 ns	30 ns	< 75 ns
Receiver delay mismatch	2.616 ns	0.4 ns	0.427 ns	5 ns	2 ns	< 5 ns
Supply voltage	5 V	3.3 V	3.3 V	7 V	5.5 V	5 V
ESD (HBM)	8 kV	N/A	N/A	6 kV	8 kV	6 kV
High voltage tolerance on BP/BM	±60 V	3.3 V	3.3 V	±40 V	±60 V	±60 V
Power dissipation	181.5 mW	76.62 mW	43.01 mW	315 mW	192.5 mW	N/A

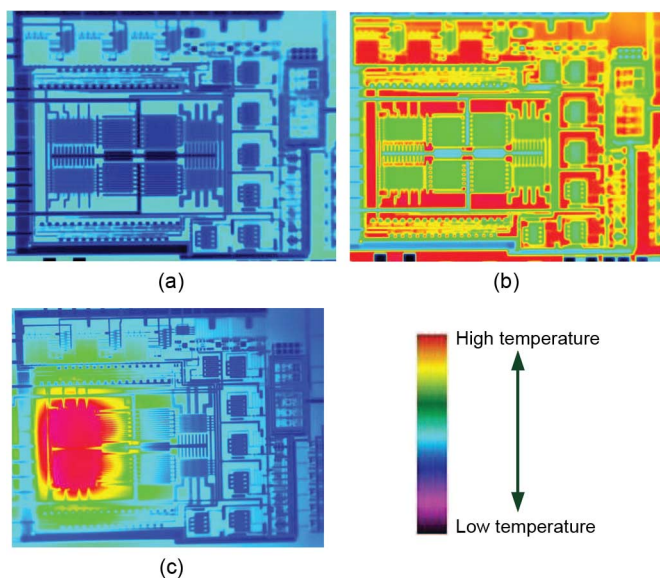


Fig. 21. Infrared images of the proposed design before short-circuiting and after short-circuiting.

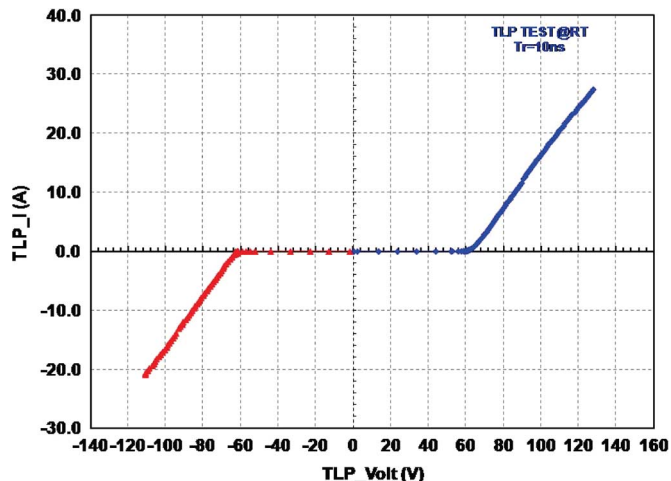


Fig. 22. Measurement results of high-voltage ESD (HVESD).

BM are short-circuited in a negative high voltage, where the activating time is less than 94.73 ns. In order to prove the effect of the over-voltage detector, the infrared images demonstrate the relative temperature distribution before and after BP/BM are short-circuited in high voltages, as shown in Fig. 21, where the measurement settings are described as follows:

- Fig. 21(a): Over-voltage detector is activated before short-circuiting.

- Fig. 21(b): Over-voltage detector is activated after when BP and BM are short-circuited in high voltages.
- Fig. 21(c): Over-voltage detector is turned off when BP and BM are short-circuited in high voltages.

Because the over-voltage detector turns off Tx after short-circuiting, the temperature of our proposed design is lower than that of the p-substrate, as shown in Fig. 21(b). By contrast, when the over-voltage detector is turned off, a large leakage current will be generated in Tx after short-circuiting, as shown in Fig. 21(c). Notably, in the scenarios of Fig. 21(c), high voltages on BP and BM cause a huge current to flow back into VDD or GND through these high-voltage MOSs. If the time of such an attack is long, the HV devices will break down.

Fig. 22 shows measurement TLP IV curve of the standalone ESD device. Positive and negative voltage are above ± 60 V, which are qualified for FlexRay applications. It has reached up to 20 A and HBM test passes 8 kV.

Table III shows the comparison of this work and several prior works. Because the common voltage of Tx is set to 2.5 V in our work, the power consumption is larger than that of the prior works. By contrast, the FlexRay transceivers in [4] and [5] did not have high-voltage tolerance design and high-voltage ESD, which is why their power dissipation is smaller. Referring to Table III, the proposed design attains the lowest power dissipation in those solutions compliant with the FlexRay specifications, including functionality and reliability requirements.

V. CONCLUSION

In this work, the proposed FlexRay transceiver is equipped with high-voltage tolerance design and high-voltage ESD, which perform the protections of all the required faults in the FlexRay specification. Notably, the proposed design is implemented using a $0.18 \mu\text{m}$ CMOS mixed-signal based generation II HV BCD process such that it is easily integrated with digital circuits. Besides, these protective devices, i.e., high-voltage ESD, high-voltage diode, and the over-voltage detector, are fabricated on the same die and measured to justify their performance. Most important of all, they are able to protect the transceiver from any fault condition of high voltage.

ACKNOWLEDGMENT

This investigation is supported by Taiwan Semiconductor Manufacturing Company (TSMC), Taiwan, for their thoughtful chip fabrication service. The authors also like to thank Aim for Top University Plan project of NSYSU and MOE, Taiwan, for partially supporting this investigation. The authors would also like to thank Dr. C.-F. Wu and Mr. W.-F. Tsai of NXP

Semiconductors (Taiwan) Ltd. and CIC (Chip Implementation Center) of NARL (Nation Applied Research Laboratories), Taiwan, for their strong support of the thermo chamber equipment and infrared image measurements.

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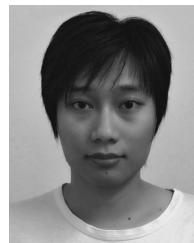
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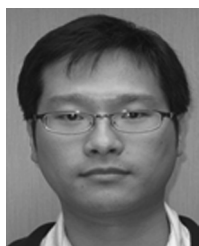


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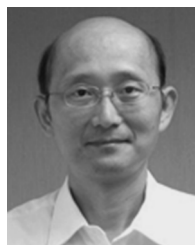
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