±10.5 V 16-channel programmable pulse generator using high-voltage BCD CMOS process

Chua-Chin Wang, Deng-Shian Wang, Tzu-Chiao Sung, Yi-Hong Wu and Doron Shmilovitz

A ±10.5 V programmable pulse generator (PPG) fabricated by high-voltage (HV) BCD CMOS technology is demonstrated, where a charge pump composed of five cascaded voltage doublers is included to boost the voltage from 2.5 V to be higher than 10 V. A cross-voltage-domain operational amplifier is proposed to carry out voltage level conversion and amplification. HV analogue switches are also proposed to change the direction of output currents. The proposed 16-channel PPG is realised on silicon, where the die area is 5.43 mm^2. Physical measurements justify that the maximum output current is 525 μA, and the largest voltage of the pulses is ±10.5 V.

Introduction: Currently, high-voltage (HV) devices are widely employed in many applications. One of the most critical problems caused by these HV signals is that the voltage level is very much higher than that of existing processes, particularly nano-scale technology. Thus, the HV discretes are generally integrated with logic ICs on PCB-based systems to prevent HV signals from damaging low-voltage (LV) ICs. Ethier and Sawan [1] presented a pulse generator (PG) design to provide a stimulation pulse current and drive HV output electrodes on an electrode–tissue interface. This approach mainly used a high pulse current to generate a HV output, namely, current-controlled stimulator, which features advantages such as good safety and high controllability. However, if we tend to enlarge amplitude voltage to drive electrodes with higher impedance, a set of positive and negative charge pumps are needed to generate output voltages higher than 9 V and deliver a sufficiently large constant current at the same time. Notably, the parasitic diodes in the negative charge pump could introduce a positive feedback path to cause latch-up issues. The consequence is circuit burnout. Lin *et al.* [2] proposed a neural stimulator based on 0.18 μm standard CMOS process. Using cascaded transistors and a voltage divider composed of resistors to generate a bias voltage, this report features that LV transistors are used to generate a voltage higher than 10 V, which is even higher than its supply voltage (VDD). Besides, every transistor is well operated in a normal range such that the output electrical stimulation signals are not affected. However, this method did not demonstrate HV output on its own such that it still needed external HV voltage supplies [2]. Another reported approach showed that HV supply for chips could be generated by charge pumps [3]. However, this method only provided the simulations results without any validation on silicon. Although we have revealed the programmable PG (PPG) theory in [4], it was never physically proved in any hardware realisation. To resolve all the mentioned problems, this Letter presents a 16-channel HV PPG on silicon such that output pulses with different amplitudes for various applications will be generated.

16-channel HV PPG: Fig. 1 shows the overview of the proposed 16-channel HV PPG consisting of four blocks, i.e. a five-stage charge pump, an 8 bit current steering digital-to-analogue converter (DAC), a 16-channel sample and hold circuit (S/H) and 16 PGs (PGi, $i = 0$–15). The five-stage charge pump generates a HV larger than VDD, providing the supply voltage required by the PGs, and the five-stage charge pump will theoretically boost the 2.5 V input voltage to be about 15 V [5]. On the basis of an 8 bit pulse amplitude code, the DAC generates a corresponding reference voltage, DAC_out (0–1.8 V), which is coupled to the PGs chosen by the 4 bit channel select coupled to 16-channel S/H. The 4 bit channel select input determines which channels and PGs are chosen to excite. The output voltage of the selected PGs, namely, o_pg_i, 0–±10.5 V, $i = 0$–15, will be proportionally determined by DAC_out, Vcp_out (i.e. output of the charge pump), and the corresponding pulse type code, where the 32 bit pulse type code notifies the selected PGs the features of the required output signals, including amplitude, duty cycle, pulse width etc. In short, the proposed HV PPG is able to generate HV internally and provide various voltage output pulses. Since the DAC and S/H circuitry are carried out by conventional designs, and the charge pump is referenced to [5], there is no need to rephrase hereby. The details of PGs block is described as follows.

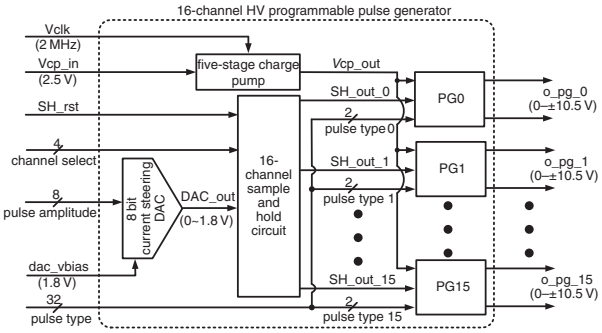

Fig. 1 *Block diagram of proposed 16-channel HV PPG*

The proposed PG is composed of HV operational amplifier (HV OPA) and HV analogue switch (HV analogue switch), as shown in Fig. 2*a*. If the channel is enabled, the S/H circuit sends a voltage, SH_out_(i) (0–1.8 V) to the corresponding HV OPA, which will then proportionally amplify the voltage to 0–10.5 V at the output.

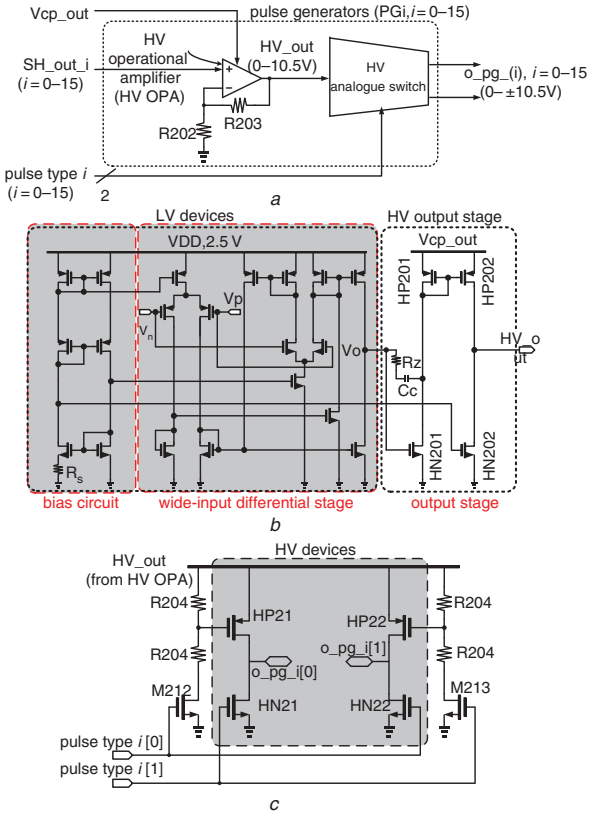

Fig. 2 *Schmetic of each circuit*

a PGs
b HV OPA [6]
c HV analogue switch

The HV OPA has three states capable of converting an LV signal into a HV signal, as shown in Fig. 2*b* [6]. The LV differential stage generates a voltage V_o, whereas the HV output stage is basically a common source amplifier with an RC couple to V_o (namely, Rz and Cc) to generate an output with a swing as high as Vcp_out at HV_out. Referring to Fig. 2*b*, HP201, HP202, HN201 and HN202 are HV PMOS and NMOS transistors, respectively. Notably, Rz and Cc are also compensation paths to provide a better step response of the HV OPA.

Fig. 2*c* shows the schematic of the HV analogue switch circuit, which is composed of four HV transistors: HP21, HP22, HN21, HN22 and four resistors: R204. The resistors are used as voltage dividers to provide gate drives of HP21 and HP22. When pulse type *i*[0] turns high and pulse type *i*[1] stays low, the LV transistor M212 and the HV transistor HN22 are turned on. Then, HP21 is turned on due to the voltage drop of R204. Therefore, the output of the HV OPA, HV_out, is coupled to o_pg_i[0] and o_pg_i[1] is pulled down to ground. In contrast,

when pulse type i[1] turns high and pulse type i[0] stays low, the output of the HV OPA, HV_out, is coupled to o_pg_i[1] and o_pg_i[0] is pulled down to ground.

Implementation and measurement: Taiwan Semiconductor Manufacturing Company (TSMC) 0.25 µm 60 V BCD CMOS technology is used to carry out the proposed design on silicon. Fig. 3 shows the die photo of the proposed PPG, where the area is 2862 × 1900 µm^2 (with PAD). To investigate the high-impedance driving ability PPG, we use a 200 kΩ resistor as the load in this experiment. Fig. 4*a* shows a HV output pulse (±10.5 V) at 100 Hz, whereas Fig. 4*b* demonstrates an LV output pulse (±4.5 V). In contrast, Figs. 4*c* and *d* demonstrate that the PPG generates 200 Hz positive and negative pulses with different voltage levels, respectively.

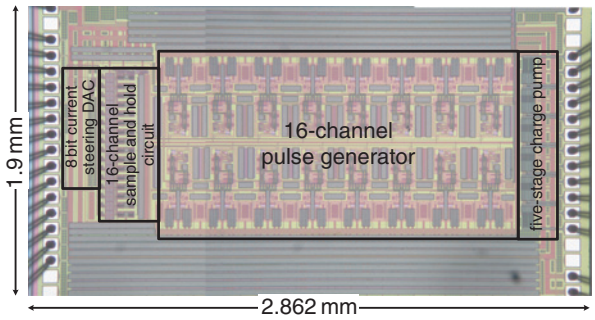

Fig. 3 *Die photo of proposed PG*

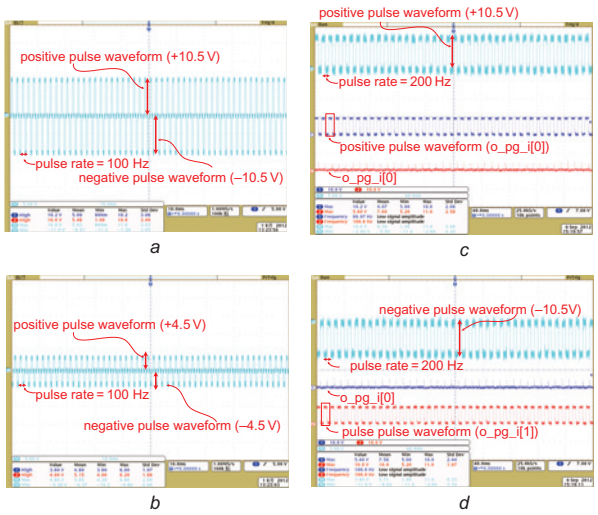

Fig. 4 *Generated HV (measurement result)*
a 100 Hz with pulse voltage +10.5 V to −10.5 V
b 100 Hz with pulse voltage +4.5 V to −4.5 V
c 200 Hz with pulse voltage +10.5 V to 0 V
d 200 Hz with negative voltage 0 V to −10.5 V

Table 1: Comparison of HV PGs

Device	Proposed	[1]	[7]
Process (µm)	0.25	0.18 (LV) and 0.8 (HV)	0.18
Amplitude (V)	±10.5	±8.5	~10.5
Number of channels	16	16	4
Output current (µA)	525	200	136
Power/channel (mW)	5.4	54.91	200
Programmable mode	yes	no	yes
Operating Freq. (Hz)	2–1200	N/A	N/A
Number of discretes	0	N/A	>30
Die size	5.43 mm^2	8.96 mm^2	32 cm^2 (PCB)
Year	2013	2011	2010

The performance comparison of our design with prior PGs is tabulated in Table 1. Since the proposed PPG is fabricated by HV process, the entire circuit is fully integrated on silicon without any discrete. Therefore, compared with the previous work [7], the area of the proposed PPG is significantly reduced. Besides, the proposed design provides more flexible pulse frequency range (2–1200 Hz) and HVs to drive the high-impendence load. On the basis of the maximum output voltage over 10 V, the proposed HV PPG has met the standards of many fields applications, e.g. implantable spinal cord stimulation systems [8].

Conclusion: In this Letter, a PPG using 60 V BCD CMOS process is demonstrated. Compared with the prior PG circuits, the size of the proposed design is significantly reduced using the semiconductor technology. Besides, the low power and small area demands are also achieved. Most important of all, the proposed design provides the programmable flexibility such that it can be easily integrated in many field applications.

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One or more of the Figures in this Letter are available in colour online.

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