



Process corner detection by skew inverters for 500 MHz $2 \times VDD$ output buffer using 40-nm CMOS technology



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ABSTRACT

A PVT detection and compensation technique is proposed to automatically adjust the slew rate of a high-speed $2 \times VDD$ output buffer. Based on the detected PVT (Process, Voltage, Temperature) corner, the output buffer will turn on different current paths correspondingly to either increase or decrease the output driving current such that the slew rate of the output signal is adaptive. The proposed design is implemented using a typical 40 nm CMOS process to justify the slew rate compensation performance. By on-silicon measurements, the data rate is 500/460 MHz given 0.9/1.8 V supply voltage with a 20 pF load. Particularly, the maximum slew rate improvement is 8%, the core area of the proposed design is $0.052 \times 0.254 \text{ mm}^2$, the maximum slew rate is 0.53 (V/ns), and the area overhead is only 31% for one single output buffer.

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1. Introduction

Many transistors have been integrated on a single die particularly when advanced CMOS technology is employed. What even better is that the circuits consisting of advanced transistors operate faster than ever. The nano-scale CMOS technology undoubtedly provides these advantages, e.g., high operating speed, low power supply voltage, and small area in system-on-chip (SoC) integration. However, in a PCB-based system, all the chips are unlikely fabricated by the same advanced process. That is, some of the chips or discretes in a PCB-based system were fabricated by not-so-advanced processes, e.g., 5 V or 3 V CMOS process. Therefore, buffers (namely, level converter) for the chips fabricated by the advanced processes to accommodate high or low voltage swings from “older” circuits are needed in such a scenario, as shown in Fig. 1 [1–11]. Notably, these buffer will occupy a significant portion of the PCB.

Besides, I/O interfaces must be designed to prevent hazards such as leakage current, and electrical overstress on the gate oxide,

and offset caused by applied signals with different voltage levels [12]. These hazards will become even worse if the nanometer CMOS technology is used and PVT variations appear [13–16]. However, most of the prior designs did not consider the slew rate deviation caused by the PVT variation [17–22]. In fact, PVT variations have been proved to affect the slew rate of the output buffer severely, as shown in Fig. 2 [17,23]. Thus, many recent works have been proposed to enhance the capability against PVT variation and enlarge the acceptable envelope as much as possible to elevate the yield. Though delay-based methods have been widely utilized to the detect PVT variation [18,23], those methods can only recognize three corners, i.e., TT, FF, and SS. The FS and SF corners were left unsolved in these works. To resolve this problem, we propose a novel corner detection technique to detect all process corners, i.e., TT, FF, SS, SF, and FS, in this work. Another problem of the prior work is that the transmitting and receiving speeds were not fast enough to meet certain high-speed specifications, e.g., PCI-express, which might be up to 266 MHz [24,25]. Apparently, high speed operation becomes another demand for mixed-voltage I/O buffers besides the PVT detection and the slew rate compensation.

In this study, we propose a high-speed $2 \times VDD$ output buffer with self-adjust slew rate using 40-nm CMOS technology. By using the compensation mechanism as well as the process corner detectors, the slew rate of the output buffer is self-adjusted given a 500 MHz data rate.

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2. 2 × VDD output buffer circuit design

Fig. 3 shows the block diagram of the proposed output buffer comprising 3 major blocks, i.e., PVT sensor, PVT decoder, and a 2 × VDD output buffer. The details of these function blocks are given in the following text.

2.1. PVT sensor

The PVT sensor in Fig. 3 is composed of a PMOS Process sensor, an NMOS Process sensor, and a Voltage & Temperature sensor. The PMOS Process sensor and NMOS Process sensor deliver four signals, PF, PS, NF, and NS, so as to show the detected process corner. Voltage & Temperature sensor sends out VT to show voltage and temperature status. Notably, the process corners are only needed to be detected once, while the voltage and temperature status can be acquired when needed. This is why two different reset signals, the reset1 and reset2, are needed and

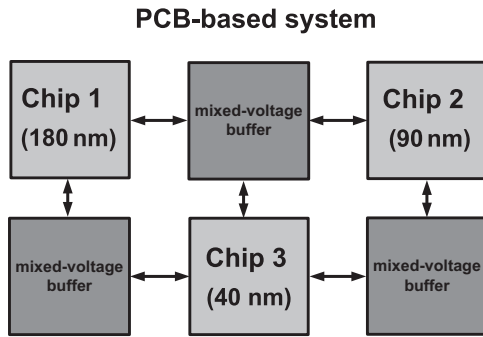


Fig. 1. An illustrative example of a PCB-based system with chips using different processes.

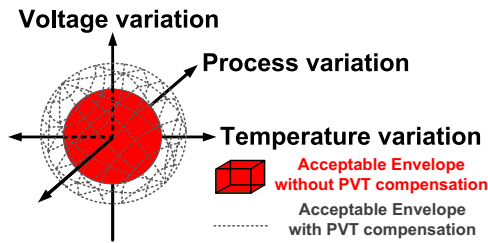


Fig. 2. Performance envelope as a function of PVT variation.

driven by an external source. The schematic and function details of the sensors are described in the following text.

2.1.1. PMOS Process sensor

Figs. 4 (a) and 5(a) show the schematics of the PMOS F and S corner sensors, which are composed of 4 cascaded inverters, respectively. Notably, inv1 ~ inv3 sizes are designed as high skew: low skew: low skew, while inv4–inv6 are high skew: high skew: low skew, respectively. The approach of these designs is that the threshold voltage difference of PMOS at S and F corners will be enlarged by those skew inverters such that the S or F corners of the PMOS transistor will be identified.

Fig. 4(a) shows a PMOS F corner sensor composed of two types of skew inverters to identify the F corner. If the F corner of PMOS is detected, PF is pulled low as logic “0”. The function of this sensor circuit is given as follows.

- Step 1 : Fig. 4 (b) shows reset1 signal of the proposed sensor circuit. When the reset1 is activated, node P1 is pulled high to $VDD-2 \times V_{thp}$. Due to voltage and temperature (V&T) variations, the input of inv1, i.e., P1, cannot be used to tell S, T, or F corner, as shown in Fig. 4 (c).
- Step 2 : inv1 is a high skew inverter, which provides a switching voltage higher than $VDD/2$, as shown in Fig. 4 (d). Though the voltage at P1 can be inverted into the voltage at P2, and separated into a high or low level by inv1, the overlapping problem still exists between F and T corners, or between T and S corners, as shown in Fig. 4 (e). The corners cannot be identified at this stage.
- Step 3 : By a similar thought, we add the inv2 following inv1. Notably, inv2 is a low skew inverter, providing a switching point voltage lower than $VDD/2$, as shown in Fig. 4(f). The aspect ratio of inv2 is chosen to generate a switching point voltage lower than that of T corner but higher than that of F corner. Thus, the F and T corners will be discriminated, as shown in Fig. 4 (g).
- Step 4 : Lastly, inv3 provides a switching point voltage, lower than $VDD/2$ as shown in Fig. 4(h). Notably, though the voltage of P3 might occur at the switching point, the output of inv3, PF, will be forced to move away such that there will be a decisive logic level at PF. Thus, the F corner of the PMOS process sensor is clearly identified, as shown in Fig. 4 (i).

By a similarly thought, a PMOS S corner sensor composed of two types of skew inverters to identify the S corner is demonstrated in Fig. 5 (a). If the S corner of PMOS is detected, PS is pulled

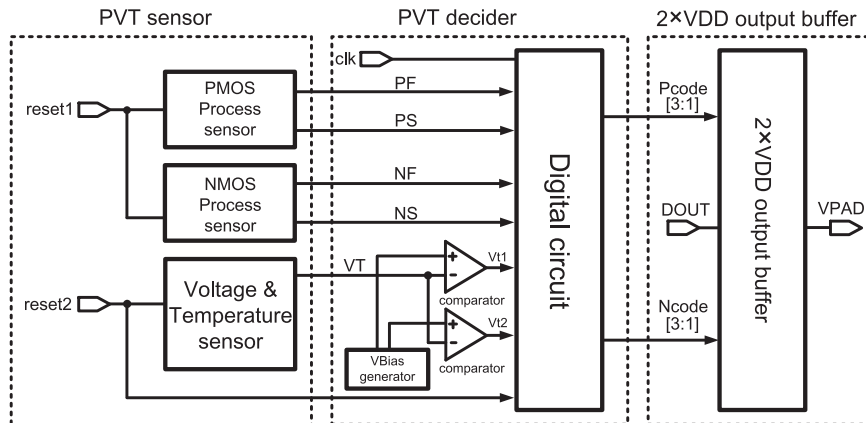


Fig. 3. The block diagram of the proposed output buffer.

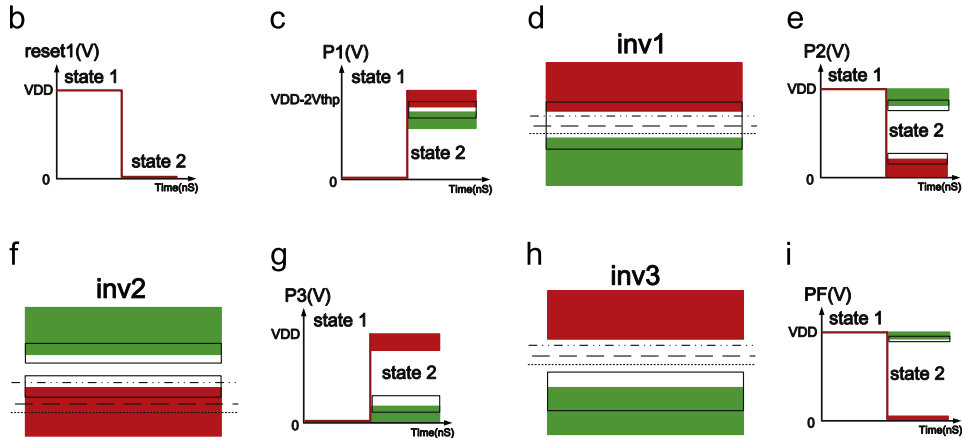
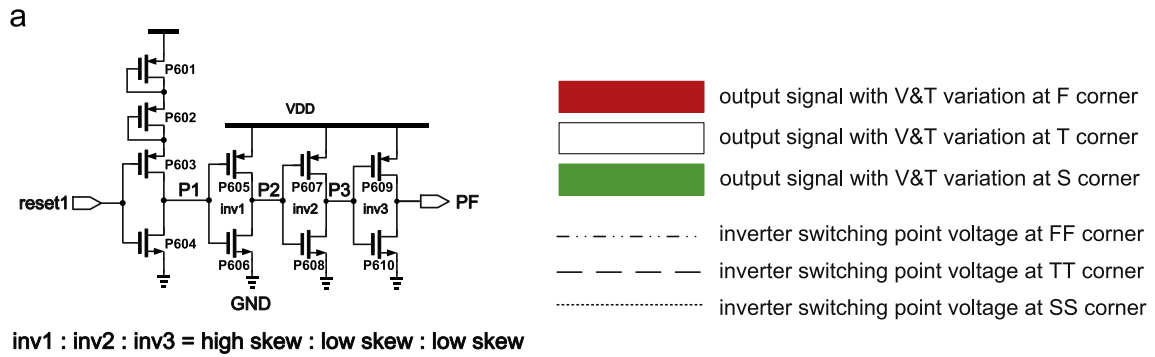


Fig. 4. (a) PMOS F corner sensor, (b) reset1 input waveform, (c) P1 output waveform, (d) inverter switching point voltage of inv1 at SS, TT, and FF corners, (e) P2 output waveform, (f) inverter switching point voltage of inv2 at SS, TT, and FF corners, (g) P3 output waveform, (h) inverter switching point voltage of inv3 at SS, TT, and FF corners, and (i) PF output waveform.

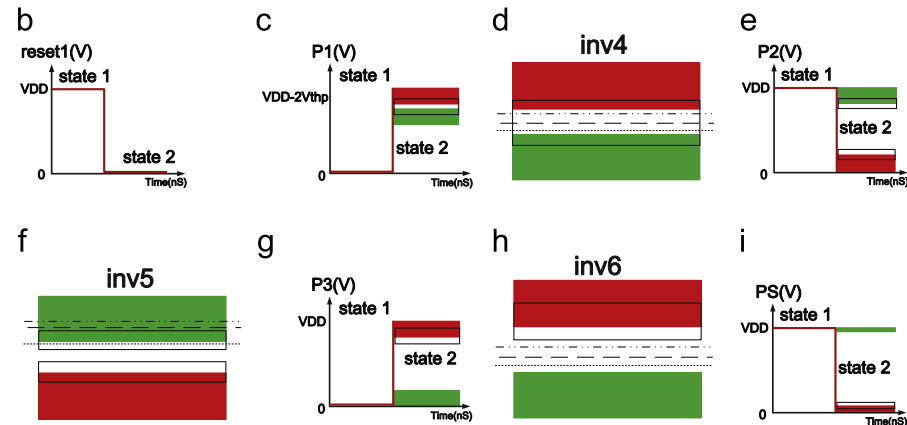
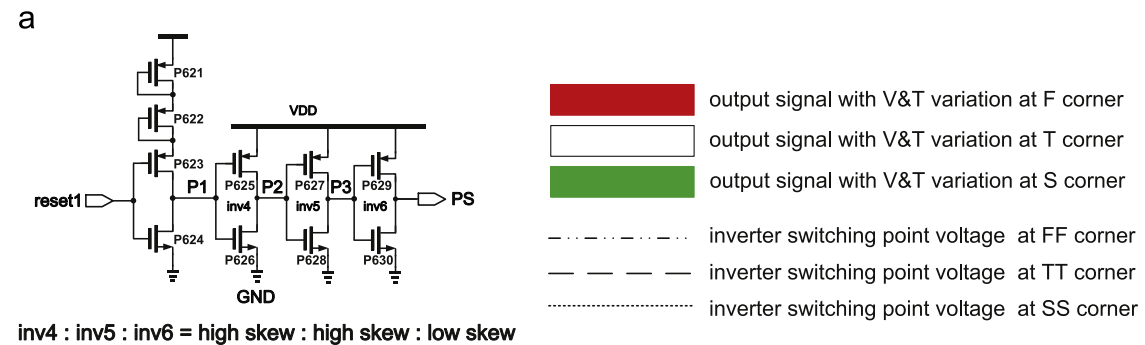


Fig. 5. (a) PMOS S corner sensor, (b) reset1 input waveform, (c) P1 output waveform, (d) inverter switching point voltage of inv4 at SS, TT, and FF corners, (e) P2 output waveform, (f) inverter switching point voltage of inv5 at SS, TT, and FF corners, (g) P3 output waveform, (h) inverter switching point voltage of inv6 at SS, TT, and FF corners, and (i) PS output waveform.

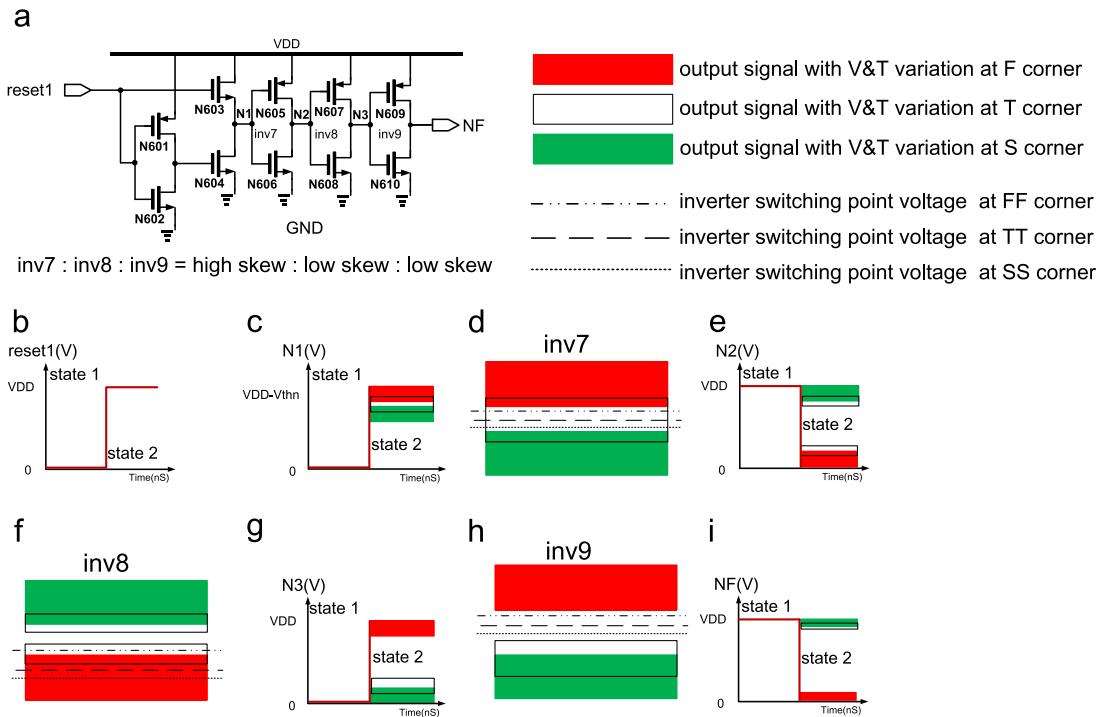


Fig. 6. (a) NMOS F corner sensor, (b) reset1 input waveform, (c) N1 output waveform, (d) inverter switching point voltage of inv7 at SS, TT, and FF corners, (e) N2 output waveform, (f) inverter switching point voltage of inv8 at SS, TT, and FF corners, (g) N3 output waveform, (h) inverter switching point voltage of inv9 at SS, TT, and FF corners, and (i) NF output waveform.

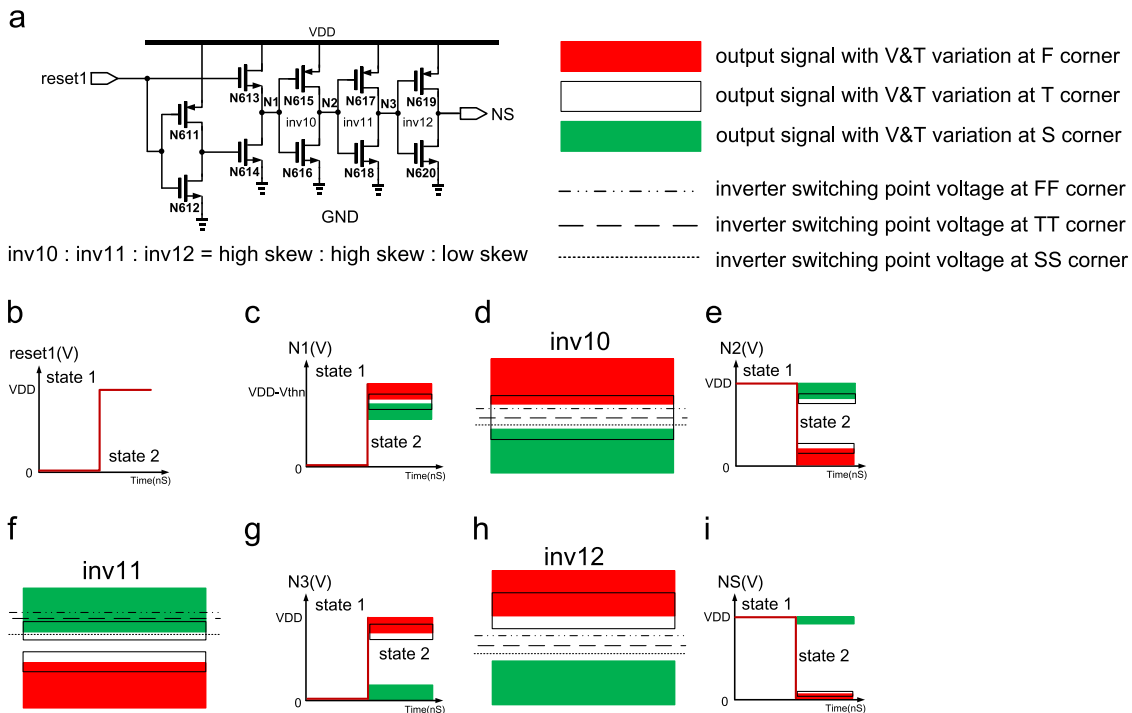


Fig. 7. (a) NMOS S corner sensor, (b) reset1 input waveform, (c) N1 output waveform, (d) inverter switching point voltage of inv10 at SS, TT, and FF corners, (e) N2 output waveform, (f) inverter switching point voltage of inv11 at SS, TT, and FF corners, (g) N3 output waveform, (h) inverter switching point voltage of inv12 at SS, TT, and FF corners, and (i) NS output waveform.

high as logic “1”. The function of this sensor circuit is given as follows.

- *Step 1* : Fig. 5(b) shows reset1 signal of the proposed sensor circuit. When the reset1 is activated, node P1 is pulled high to

$VDD - 2 \times V_{thp}$. Due to voltage and temperature variations, the input of inv4, i.e., P1, cannot be used to tell S, T, or F corner, as shown in Fig. 5 (c).

- *Step 2* : inv4 is a high skew inverter, which provides a switching voltage higher than $VDD/2$, as shown in Fig. 5(d). Though the

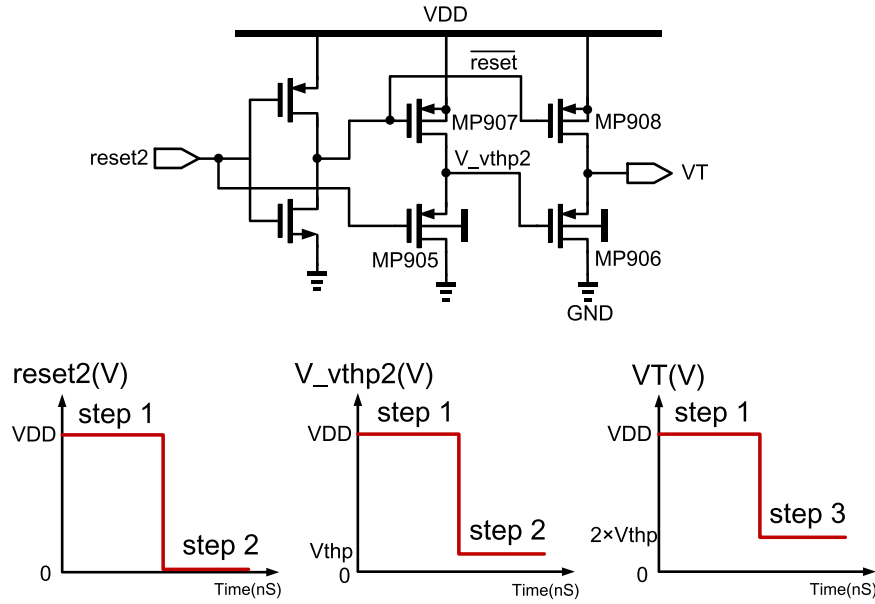


Fig. 8. Schematic of voltage and temperature sensor.

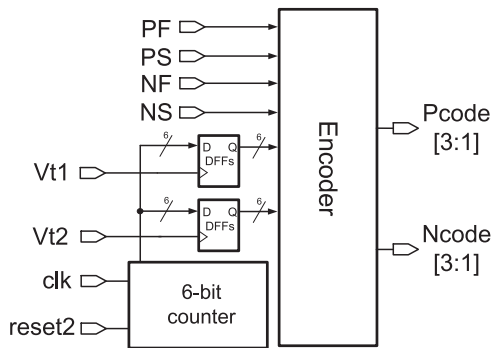


Fig. 9. Schematic of digital circuit.

- Step 3 : Similarly, inv5, which is a high skew inverter providing a switching point voltage higher than $VDD/2$, is added following inv4, as shown in Fig. 5(f). Notably, the aspect ratio of inv5 is chosen to generate a switching point voltage higher than that of T corner but lower than that of S corner. Thus, the S and T corners will be discriminated, as shown in Fig. 5 (g).
- Step 4 : Lastly, inv6 provides a switching point voltage, lower than $VDD/2$ as shown in Fig. 5(h). Though the voltage of P3 might occur at the switching point, the output of inv6, PS, will be forced to move away such that there will be a decisive logic level at PS. Thus, the S corner of the PMOS process sensor is clearly identified, as shown in Fig. 5(i).

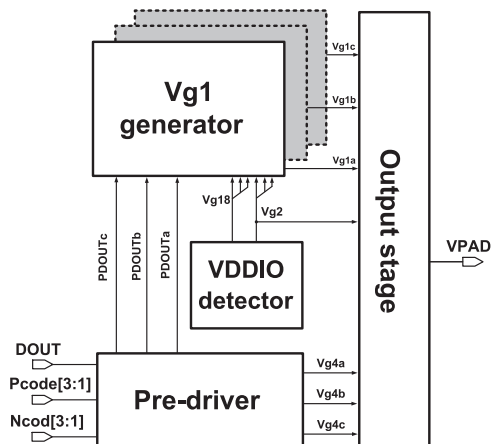


Fig. 10. Schematic of $2 \times VDD$ mixed-voltage tolerant output buffer.

voltage at P1 can be inverted into the voltage at P2, and separated into a high or low level by inv4, the overlapping problem still exists between F and T corners, or between T and S corners, as shown in Fig. 5 (e). The corners cannot be identified at this stage.

2.1.2. NMOS Process sensor

Figs. 6(a) and 7(a) show the schematics of the NMOS F and S corner sensors, which are composed of 4 cascaded inverters, respectively. Notably, inv7–inv9 sizes are designed as high skew : low skew : low skew, while inv10 ~ inv12 are high skew: high skew: low skew, respectively. The approach of these designs is that the threshold voltage difference of NMOS at S and F corners will be enlarged by those skew inverters such that the S or F corners of the NMOS transistor will be identified. The entire operations of those circuits in Figs. 6 and 7 are very much the same as those in Figs. 4 and 5 so that there is no need to rephrase the lengthy descriptions.

2.1.3. Voltage and temperature sensor

Fig. 8 shows the schematic of Voltage & Temperature sensor, comprising 2 cascaded PMOS source followers and an inverter. The PMOS source follower is composed of MP905–MP908. Notably, MP905–MP906 and MP907–MP908, which are without the body effect and with body effect, respectively. The function description of this sensor circuit is given as follows.

- Step 1 : When the reset2 is activated, V_{vthp2} and VT are pulled high to VDD ($=0.9 V$).
- Step 2 : When the reset2 is pulled low, V_{vthp2} is discharged till V_{thp} , which is the threshold voltage of MP905.

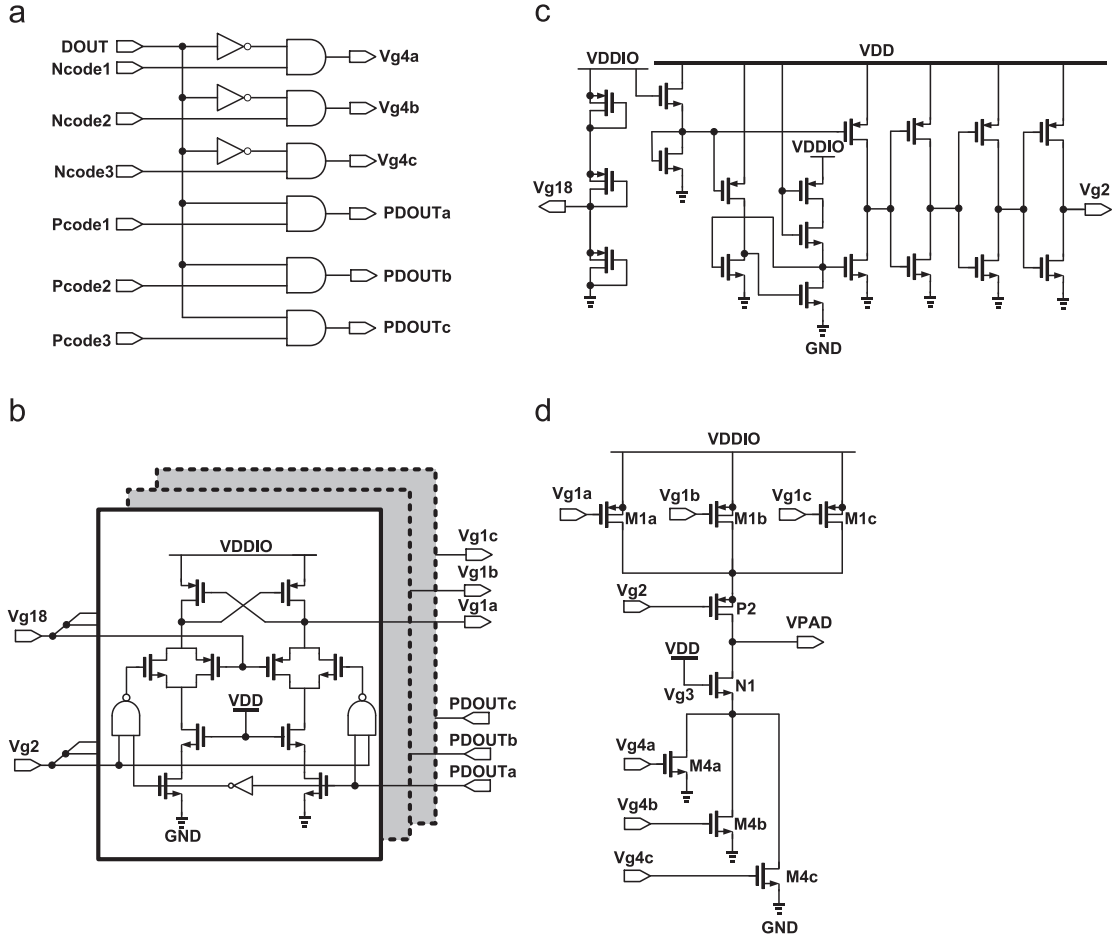


Fig. 11. Schematic of (a) Pre-driver, (b) Vg1 generator, (c) VDDIO detector, and (d) output stage.

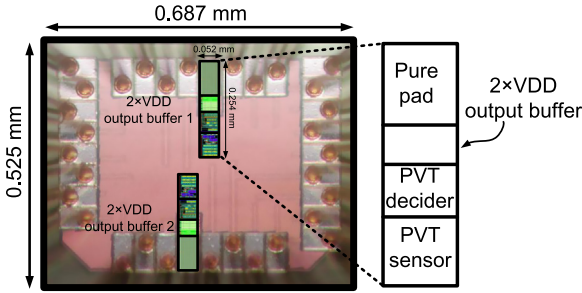


Fig. 12. Die photo of the proposed design.

- **Step 3 :** By a similar operation, V_T will be discharged till $2 \times V_{thp}$ in the next repeated cycle the same as the previous steps 1 and 2.

According to Eq. (1), V_{thp} of MOS with body effect will drift depending on the variation of V_{bs} , which is the voltage difference between bulk ($=VDD$) and source voltage of MOS. Notably, V_{thp0} is the no body effect threshold voltage, γ_p is the body effect coefficient, V_{fn} is the bulk surface potential, and V_{bs} is the voltage difference between bulk and source of MOS.

$$V_{thp} = V_{thp0} + \gamma_p (\sqrt{2|V_{fn}| + V_{bs}} - \sqrt{2|V_{fn}|}) \quad (1)$$

where γ_p can be written as $\gamma_p = \sqrt{2q\epsilon_s N_A / C_{ox}}$, q is electronic charge, ϵ_s is silicon dielectric constant, N_A is doping concentration, and C_{ox} is oxide capacitance. N_A will be changed by the mobility of q , which is related to temperature. Since γ_p of the V_{thp} comprises temperature factors, the 2 cascaded source followers generate a

$2 \times V_{thp}$ voltage, namely V_T , which is also indirectly an indicator of VDD and temperature variation.

2.2. PVT decider

PVT decider in Fig. 3 consists of a V_{Bias} generator, two comparators, and a Digital circuit. Fig. 9 shows the block diagram of Digital circuit composed of a 6-bit counter, an Encoder, and D flip-flops. According to the outputs of PMOS Process sensor, NMOS Process sensor, and Voltage & Temperature sensor, the PVT decider derives two digital codes, Pcode [3:1] and Ncode [3:1], to notify the following $2 \times VDD$ output buffer what the sensed PVT status is. That is, the codes indicate the required compensation status so as to control the output currents in the following $2 \times VDD$ output buffer.

2.3. $2 \times VDD$ output buffer

The $2 \times VDD$ output buffer in Fig. 3 is composed of a Pre-driver, a Vg1 generator, a VDDIO detector, and an Output stage, as shown in Fig. 10. The Pre-driver generates 6 signals, PDOUTa ~ c, Vg4a ~ c, based on three received signals, DOUT, Pcode [3:1], and Ncode [3:1], to adjust output currents. The VDDIO detector and Vg1 generator will then generate appropriate gate drive voltages in different voltage modes to avoid leakage currents and overstress problems. The schematic and function details are described in the following text.

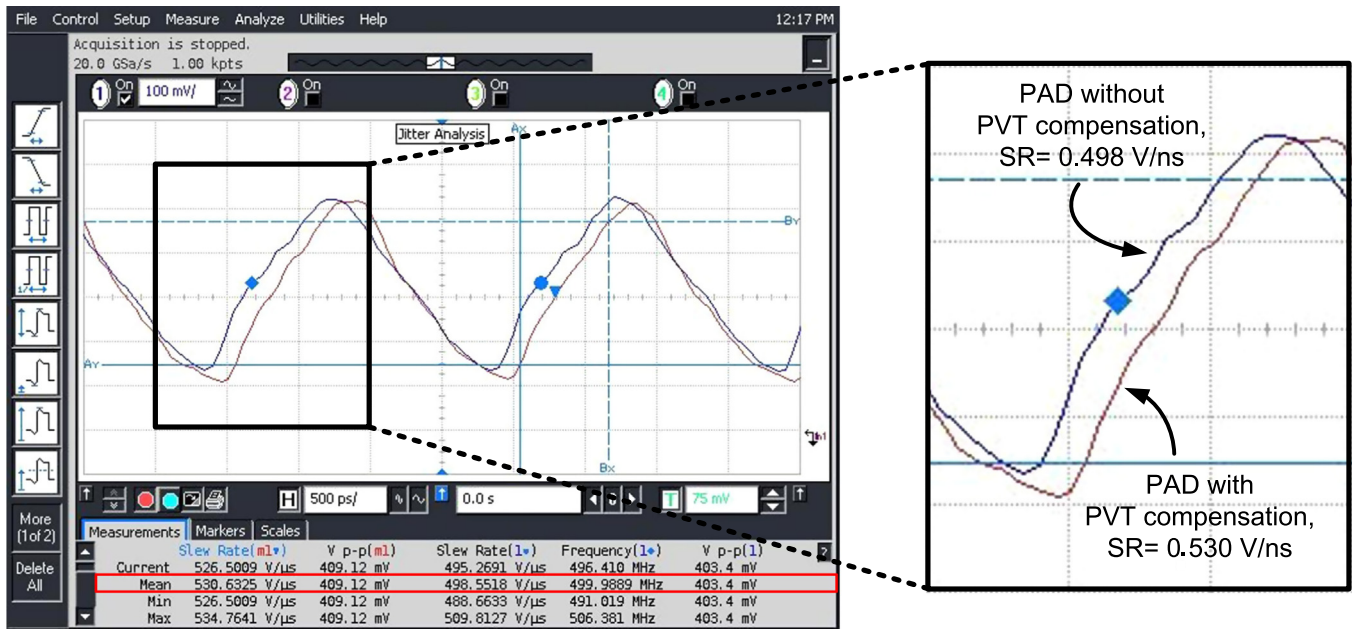


Fig. 13. VPAD waveforms of the uncompensated and compensated output buffers given VDDIO=0.9 V.

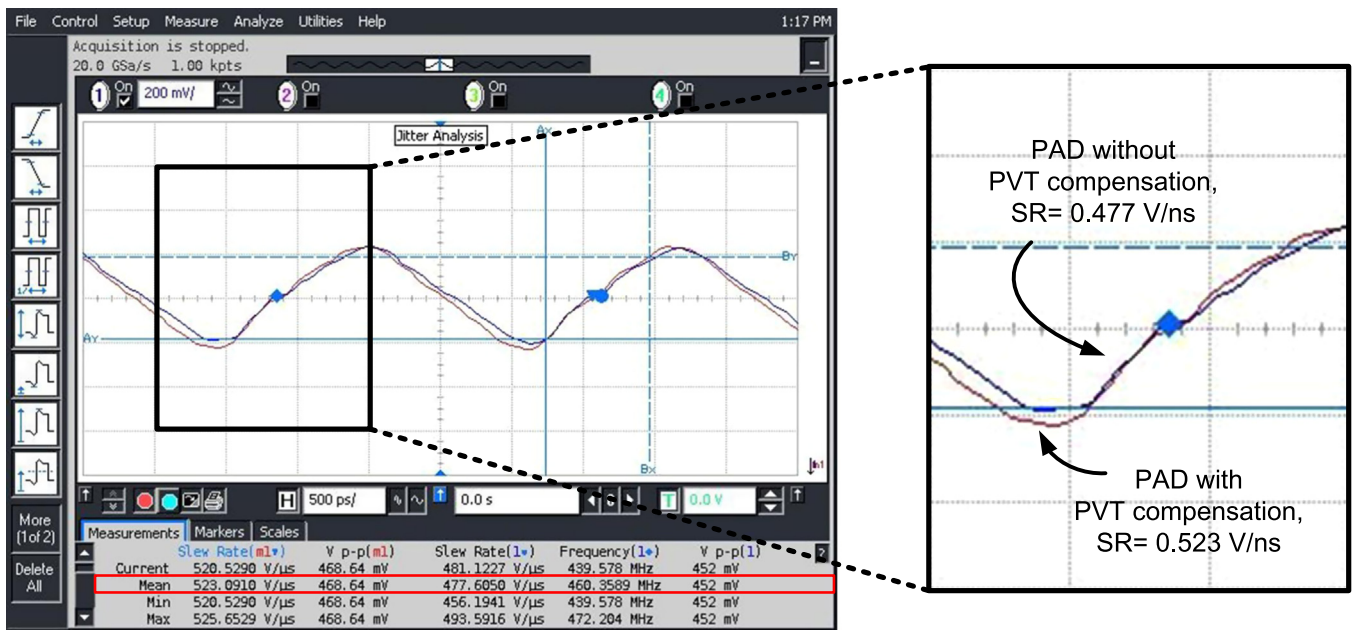


Fig. 14. VPAD waveforms of the uncompensated and compensated output buffers given VDDIO=1.8 V.

2.3.1. Pre-driver

Fig. 11 (a) shows the Pre-driver circuit, which is composed of simple digital logic circuits. The Pre-driver accepts Pcode [3:1], and Ncode [3:1] signals from the PMOS Process sensor, the NMOS Process sensor, and the Voltage & Temperature sensor. After decoding Pcode [3:1] and Ncode [3:1] into Vg4a ~ c, the current paths will be selected in the Output stage.

2.3.2. Vg1 generator

Fig. 11 (b) shows the Vg1 generator composed of three voltage level converters. The Vg1 generator generates Vg1a ~ c based on the Pre-driver output signals (PDOUt a ~ c) and Vg2 from VDDIO detector to prevent over-voltage hazards in the Output stage.

2.3.3. VDDIO detector

Fig. 11(c) shows the VDDIO detector circuit, which provides a 0/1.2 V gate drive on P2 in Fig. 11(d) to prevent the stress problem of the transistor gate oxide when VDDIO=0.9/1.8 V. Besides, the VDDIO detector provides a bias voltage (Vg18) for Vg1 generator.

2.3.4. Output stage

Fig. 11(d) shows the Output stage of the proposed $2 \times VDD$ output buffer. The supply voltage (VDD) of the core circuits using 40 nm CMOS process is 0.9 V. Thus, the Output stage must be realized using two groups of stacked PMOS and NMOS transistors, respectively, to transmit $2 \times VDD$ signals, as shown in Fig. 10. PMOSs M1a ~ c are in parallel such that the slew rate of the output signal can be

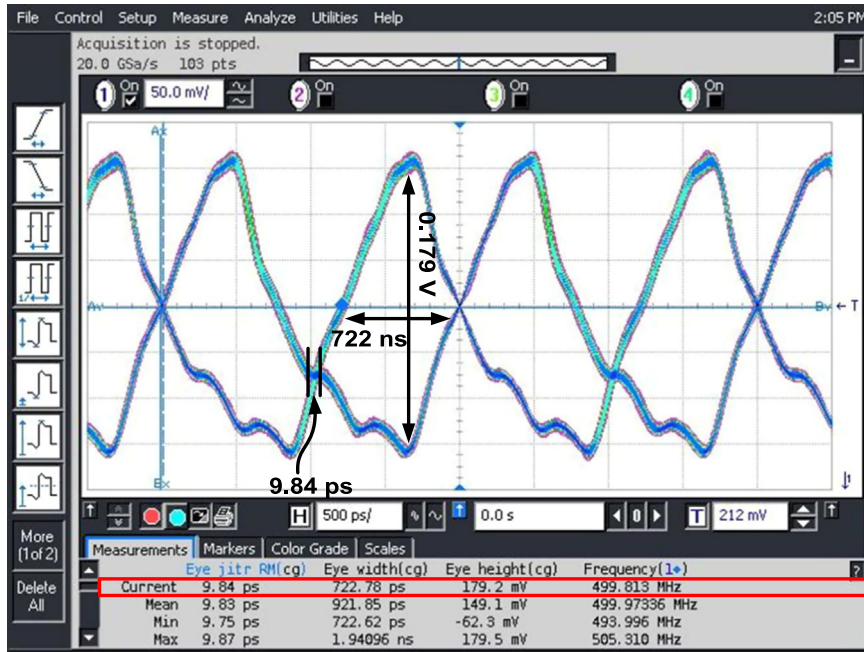


Fig. 15. VPAD eye diagram of the uncompensated buffer given $VDDIO=0.9$ V in Tx mode.

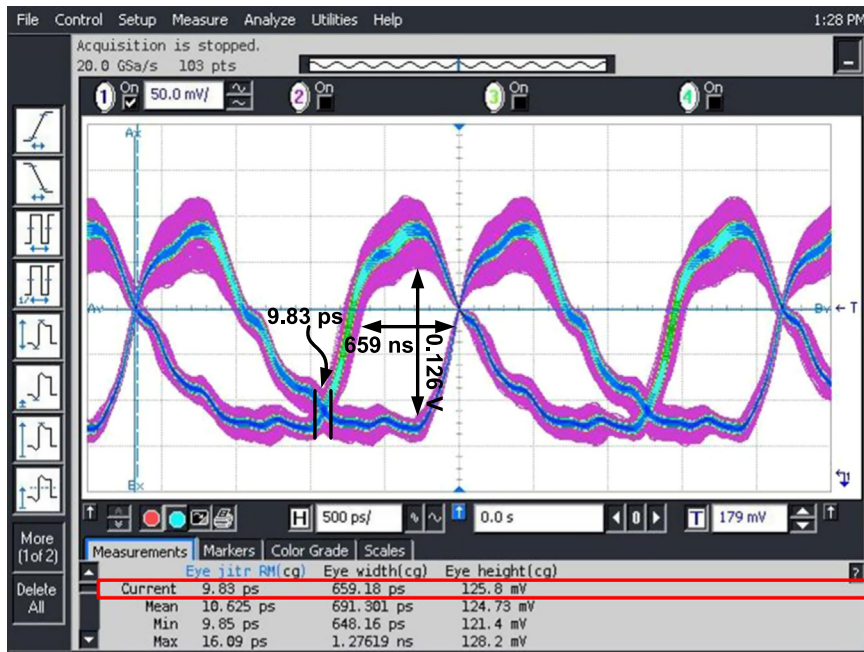


Fig. 16. VPAD eye diagram of the uncompensated buffer given $VDDIO=1.8$ V in Tx mode.

compensated by turning on or off the current paths flowing through M1a ~ c individually. According to the detected different process and temperature status, Pcode [3:1] and Ncode [3:1] will select corresponding turned-on PMOSs and NMOSs in the Output stage, respectively. Notably, PMOSs M1a ~ c and NMOSs M4a ~ c are designed with different sizes to generate currents with different magnitudes, which are also allowed to deliver a larger current if two or more current paths are selected.

3. Implementation and measurement

This work is implemented using 40 nm CMOS technology without any thick-oxide device. Fig. 12 shows the die photo of

this work, where the overall chip size is only 0.687×0.525 mm² and the compensation circuit is only 0.052×0.254 mm², the area overhead for a single buffer is 31%. Notably, the compensation circuit can be shared among many buffers such that the overhead will be reduced drastically. To reveal the performance of the proposed PVT detection and slew rate self-adjustment circuit, we realize two identical buffer circuits on the same die. The uncompensated and compensated measurements are carried out on $2 \times VDD$ output buffer 1 and $2 \times VDD$ output buffer 2, respectively. In $2 \times VDD$ output buffer 1, we turn off the compensation circuit to run the testing and measurement of the uncompensated buffer. By contrast, the compensated measurement is carried out on $2 \times VDD$ output buffer 2, where the compensation circuit is activated. The output waveforms of the uncompensated and compensated VPAD

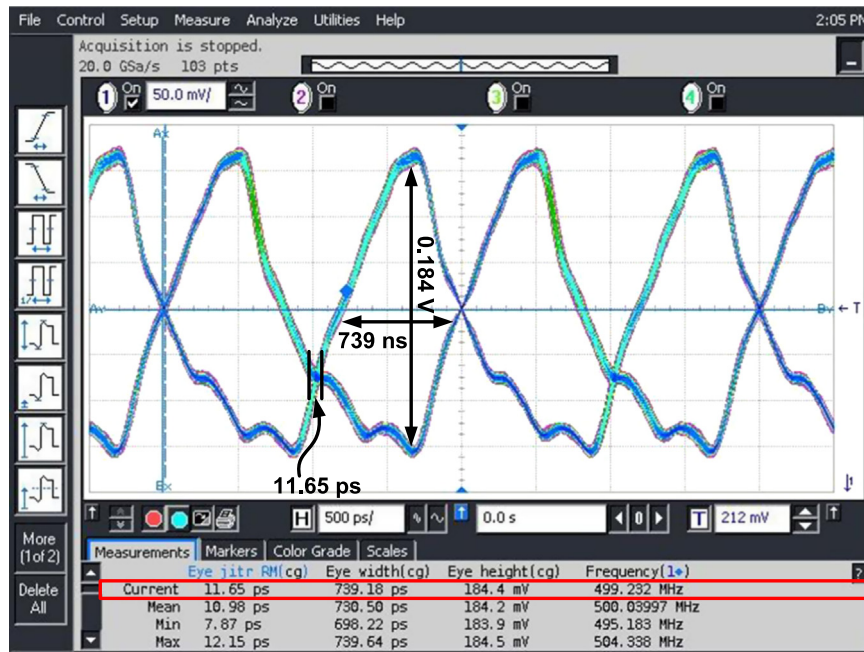


Fig. 17. VPAD eye diagram of the compensated buffer given VDDIO=0.9 V in Tx mode.

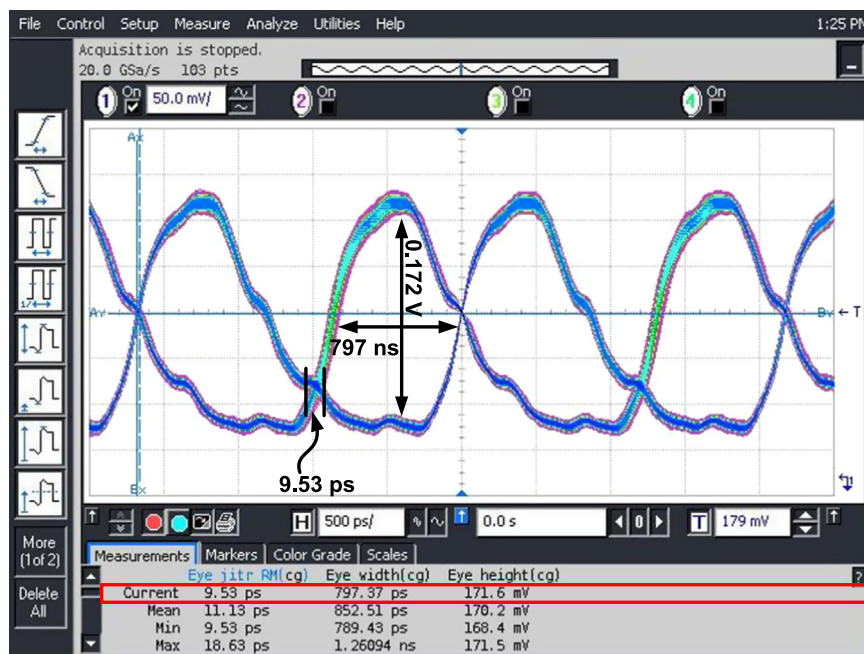


Fig. 18. VPAD eye diagram of the compensated buffer given VDDIO=1.8 V in Tx mode.

Table 1
Measurement results at different VDDIOs.

VDDIO	0.9 V	1.8 V
Data rate (MHz)	500	460
Eye jitter (ps)	111.65	9.53
Eye width (ns)	739	797
Eye height (V)	0.184	0.172
Slew rate improvement (V/ns)	8% (0.498→0.530)	6% (0.477→0.523)

given VDDIO=0.9/1.8 V in Tx mode are shown in Figs. 13 and 14, respectively. After compensation, the slew rate is enhanced to 0.530 (V/ns) from 0.498 (V/ns) when VDDIO=0.9 V, and 0.523

(V/ns) from 0.477 (V/ns) given VDDIO=1.8 V, respectively. Besides, the data rate is 500/460 MHz when VDDIO=0.9/1.8 V, respectively. The eye diagrams of VPAD of the uncompensated and compensated buffers are shown in Figs. 15 and 16 and Figs. 17 and 18, respectively. The eye is widened by 2.3%/20% when VDDIO=0.9/1.8 V, respectively. The performance of the proposed design is summarized in Table 1. Table 2 shows the comparison between this work and several prior works. This work is the only one to provide all-PVT-corner detection and the slew rate compensation. Meanwhile, our design is also the only one to meet the data rate specifications of PCI-express given VDDIO=0.9/1.8 V. Besides, Monte Carlo simulations of the proposed $2 \times$ VDD mixed-voltage tolerant output buffer is also carried out, as shown in Figs. 19 and 20. The frequency ranges of

Table 2
Performance comparison of output buffers.

	[23] JSSC	[9] TCAS-II	[1] TCAS-I	[2] TCAS-I	[12] ICICDT	This work
Year	2003	2007	2009	2010	2014	2013
Process (μm)	0.18	0.13	0.35	0.18	0.09	0.04
Voltage (V)	3.3	3.3	3.3	1.8	1	0.9
Transmitting voltage mode (V)	3.3	1/2.5	1.8/3.3/5.0	0.9/1.2/1.8/3.3/5.0	1.8/1.2/1.0	0.9/1.8
Results	Measured	Measured	Measured	Measured	Simulation	Measured
Data rate (MHz)	N/A	133	80/120/84	10/40/50 /40/10	454/370/500	500/460
Slew rate (V/ns)	0.40–0.99	N/A	Max. 0.71	N/A	1.3–3.0	0.530/0.523
Process corner detection	TT, FF, SS	N/A	N/A	N/A	TT, FF, SS, FS, SF	TT, FF, SS, FS, SF
Slew rate improvement	32%	N/A	N/A	N/A	Max. 32%	8% /6%

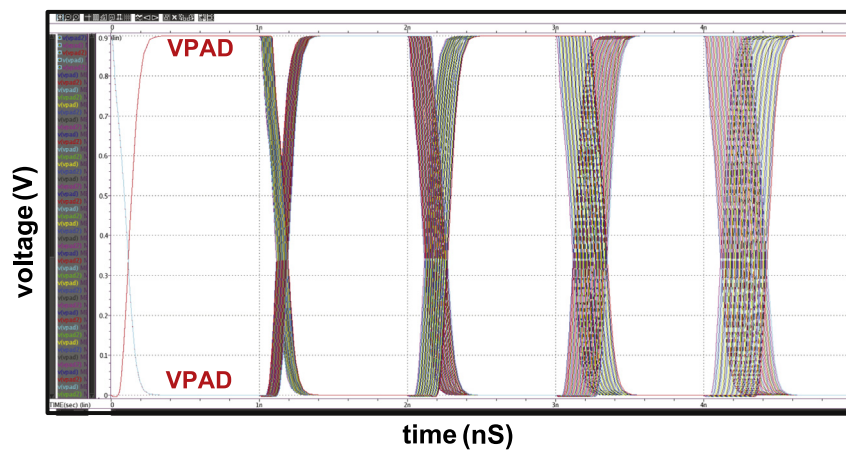


Fig. 19. Monte-Carlo simulations of the proposed $2 \times V_{DD}$ mixed-voltage tolerant output buffer given a 0.9 V supply voltage.

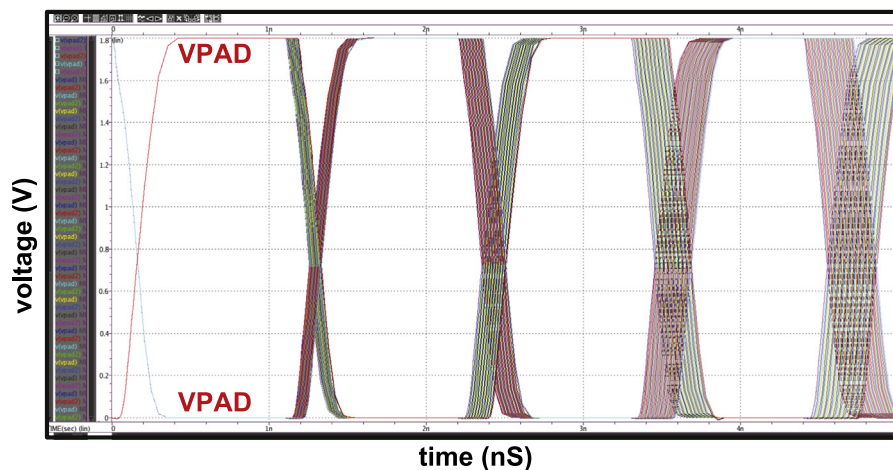


Fig. 20. Monte-Carlo simulations of the proposed $2 \times V_{DD}$ mixed-voltage tolerant output buffer given a 1.8 V supply voltage.

Figs. 19 and 20 are 500 MHz–480 MHz and 460 MHz–440 MHz, respectively, where the sampling rate is 0.5 MHz and the number of sweeps is 80.

4. Conclusion

In this work, a high-speed $2 \times V_{DD}$ output buffer with self-adjust slew rate is implemented using a typical 40 nm CMOS process. The data rate is 500/460 MHz when $V_{DDIO}=0.9/1.8$ V. The maximum slew rate and the maximum slew rate improvement are 0.53 (V/ns) and 8% when $V_{DDIO}=0.9$ V, respectively.

Notably, the area overhead is only 31% for a single output buffer. This work is proved on silicon to detect all PVT corners of PMOS and NMOS, respectively. Besides, this work is the only one to meet the data rate specifications of PCI-express given $V_{DDIO}=0.9/1.8$ V.

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