A Voltage Monitoring IC With HV Multiplexer and HV Transceiver for Battery Management Systems

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***Abstract*— This paper presents a voltage monitoring IC with high-voltage multiplexer (HVMUX) and HV transceiver for battery interconnect module (BIM) used in battery management systems (BMSs). The voltage monitoring IC must be able to accommodate input voltage up to tens of volts, perhaps even hundreds of volts, which is difficult to be realized using a logic-based solution. To realize a solution on silicon, the voltage monitoring IC shall be fabricated using an advanced HV semiconductor process, which usually is constrained by the voltage drop limitation between gate and source of HV devices. To overcome such a limitation, an HV switch is proposed in this paper, including an HV gate voltage driver (HVGVD) driving the HV MOS without any over-voltage hazard. In addition, an HV transceiver is proposed using CMOS transistors without any isolator. An experimental prototype is fabricated using a typical 0.25 μm 1-poly 3-metal 60 V BCD process. The measurement results reveal that the error and off-isolation of HVMUX is less than 2.54% and −92 dB@1 MHz, respectively. Meanwhile, the HV transceiver can transmit and receive data with a −32 ∼ +32 V common voltage.**

***Index Terms*— Analog high-voltage multiplexer (HVMUX), battery management system (BMS), high voltage (HV), high voltage transceiver.**

I. Introduction

HIGH-VOLTAGE (HV) battery management system (BMS) is widely needed in many applications, e.g., electric vehicle and hybrid electric vehicle, where many battery modules are assembled and integrated. One of the popular BMS architectures is the modular formation, i.e., a module monitors several batteries with a daisy-chain interface. For example, a distributed BMS is composed of at least five blocks, including battery interconnect modules (BIM), main controller, analysis, communication, and logging and telemetry, as shown in Fig. 1 [1], [2]. In addition to BIMs, the other four blocks are operated in low voltage (LV) domain. BIM is in charge of detecting the battery status by HV multiplexer (HVMUX), e.g., voltage, current, and temperature. Meanwhile, these battery information can be transmitted/received between adjacent BIMs by HV transceiver (upper BIM link and lower BIM link). Due to the recent HV process availability, each BIM can monitor more and more batteries. Notably, the communication methods between adjacent BIMs are realized with or without discrete components, e.g., opto-coupler [3], [4].

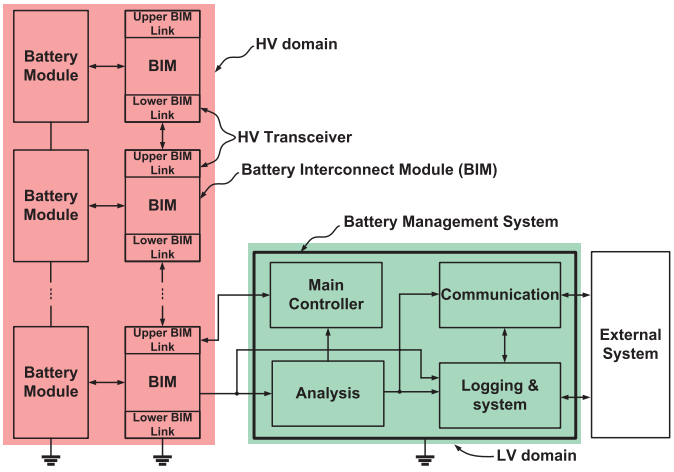

Fig. 1. Explosive view of a typical distributed BMS.

Several HVMUXs and HV switches have been reported [5]–[9]. A 2 × VDD switch was proposed using a conventional 0.18 μm CMOS process [5], [6]. However, the switch in these reports only has 7-V tolerance, it is not possible to be used in a large scale HV BMS. An 32 × 32 channel multiplexer was fabricated with a 0.35 μm silicon on insulator (SOI) process to apply in an ultrasound imaging system [7]. For field applications, the input voltage must be close to 0 V before the multiplexer is turned off. However, the batteries in BMS are always connected to BIM such that the input voltage of the multiplexer is impossible to be 0 V. Therefore, the multiplexer cannot be turned off completely, and cause a significant voltage error during voltage measurement. It is then not a good option for

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BMS designs. An integrated HVMUX was fabricated with a 0.35 μm 50-V CMOS process [8], where a large floating gate drive voltage in the HV switch ($\approx$15 V) was generated directly due to the voltage drop over the resistor. Therefore, it could result in a leakage current flowing into the output and causing large voltage distortion. A 16:1 analog MUX was revealed using a combination of process (CMOS/SOI) techniques [9], where 5-V CMOS logic circuits are shifted up to $\pm$15 V to drive HV analog switches. Referring to technology considerations for automotives [10], the SOI technology is not welcomed for power devices, since the thermal conductivity of the oxide is very low. In addition, the SOI technology is quite expensive and the integration is not very easy and straightforward, e.g., vertical components and ESD protection cells.

Another critical issue in the BMS is to the data communication among BIMs by HV transceivers or digital isolators. They are usually implemented by discrete devices, e.g., optocoupler, magnetic isolator, and capacitive isolator. Several HV transceivers or digital isolators have been reported [3], [4], [11]–[16]. An optical coupler is used to isolate and communicate between HV and LV systems [3], [4]. The disadvantages of optical couplers are high power consumption, poor integration, low speed, and degradation of light emitting diode (LED). Digital isolators using magnetic coupling [11]–[13] or capacitive coupling [14], [15] methods were proposed. However, no matter magnetic or capacitive coupling transmissions, they will generate electromagnetic interference (EMI) effect to jam other circuits or be corrupted by external wireless signals to endanger the reliability. In addition, they usually use a lot of discrete components, i.e., transformer and capacitor. Therefore, it is not easily integrated in system-on-chip (SoC) designs. A wireless battery monitor was also proposed [16]. However, it is not cost effective to realize a large scale battery system because it needs a lot of wireless modules. In other words, the cost and area efficiency will be problems.

Recently, many advanced semiconductor processes have been proposed to fabricate HV devices on silicon, e.g., TSMC 0.25 μm 1-poly 3-metal 60-V BCD process [17], [18]. This particular process offers digital cell library, LV MOSs driven by 2.5 V/5 V, and several types of HV MOS devices. Especially, the BCD technology with high power capabilities (BiCMOS technology) and integration feasibility between analog and digital devices (CMOS technology) is considered a better solution. Furthermore, the BCD technology also provide better area efficiency [19], where low voltage devices are widely used as much as possible and many external components are able to be implemented on silicon. The most critical limitation, however, is that the gate to source voltage of the HV MOS transistor must be limited under a LV $\approx$5 V. Therefore, those mentioned prior works are not easy to be directly implemented using this HV BCD process.

In this paper, we propose novel HVMUX and HV transceiver to resolve all the mentioned problems. In Section II, we explain the specifications of HVMUX and HV transceiver. In Section III, the HVMUX is disclosed, including HV switch and HV gate voltage driver (HVGVD). For field applications, HVMUX converts the voltage drop of each battery in the same string into the input range of an analod-to-digital converter (ADC). In Section IV, the schematic of HV transceiver is shown and analyzed. Notably, the proposed HV transceiver can transmit and receive data with -32 to $+32$ V common voltage. In Section V, we demonstrate the measurement results of the proposed HVMUX and HV transceiver. The performance comparison between our design and several prior works is also discussed. Finally, a brief conclusion is given in Section VI.

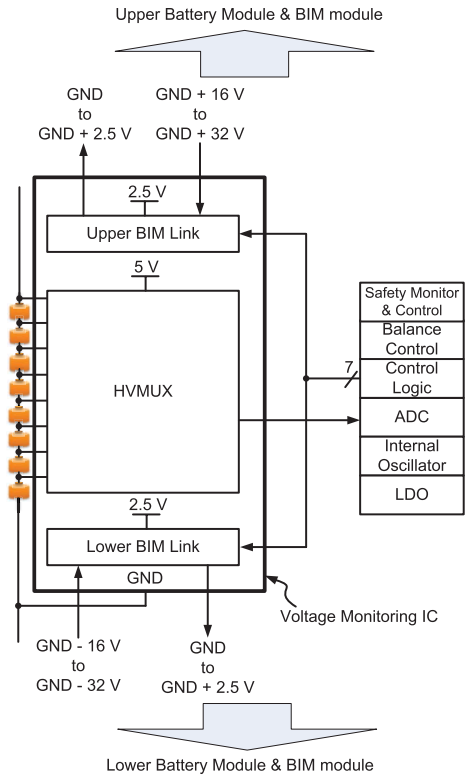

Fig. 2. Block diagram of BIM.

II. BIM System Specifications

A conceptual architecture of BIM is shown in Fig. 2, where voltage monitoring IC is composed of HVMUX and HV transceiver (upper BIM link and lower BIM link). The ADC is used to convert the output of HVMUX into a digital code, which will be passed via a serial link to HV transceiver by control logic to communicate with main controller in Fig. 1 [20]. Notably, the HVMUX and HV transceiver is operated in HV domain. The HVMUX is in charge of down-converting HV of each battery into the input range of the corresponding ADC. According to voltage measurement approaches [1], using the HVMUX is deemed as a better solution to save power and area, because each battery cell is not parallelly coupled to a corresponding ADC. Notably, a differential approach in HVMUX is good for autocancelling the common noise. The bottom line of such a design is that the voltage distortion caused by the HVMUX must be as small as possible.

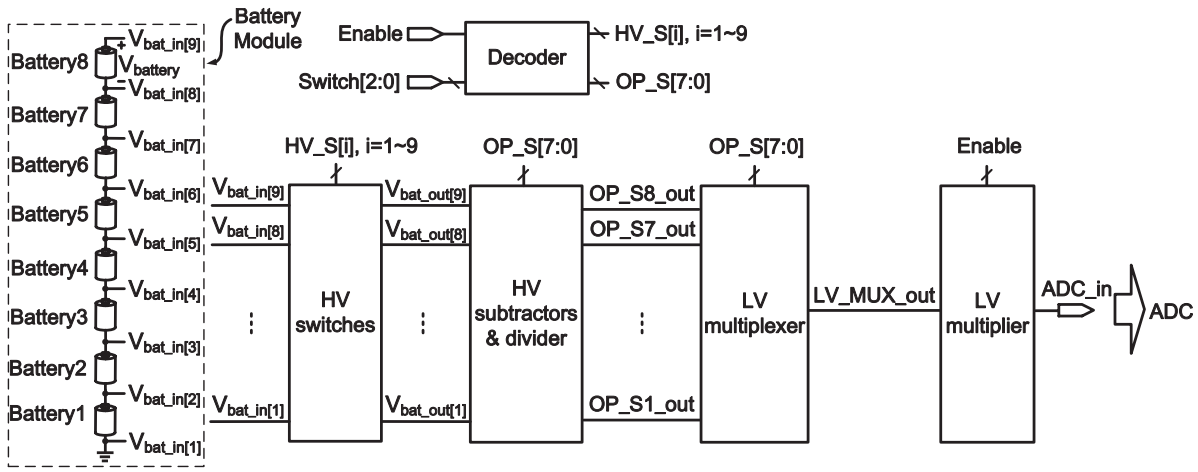

Fig. 3. Schematic of 8:1 analog HVMUX.

For example, the voltage range of each battery is around 2–4 V. Therefore, the input range of HVMUX is from 2 to 32 V. HV switches in HVMUX should possess voltage tolerance up to maximum 32 V, which will be introduced and explained in Section III. In addition, if each transmitter in HV transceiver transmits data between GND +2.5 V and GND level, the receiver in upper BIM link must receive the voltage range between GND +16 and GND +32 V, where 16 and 32 V mean that all batteries are operated in 2 or 4 V, respectively. By contrast, the receiver in lower BIM link must receive the voltage range between GND −16 and GND −32 V. In short, our HV transceiver can exchange data with a −32 to +32 V common voltage to meet the mentioned system signal requirements, which will be introduced and explained in Section IV.

III. HV Multiplexer

The proposed 8:1 analog HVMUX is shown in Fig. 3, including HV switches, HV subtractors and divider, LV multiplexer (LVMUX), and LV multiplier. The HVMUX selects a pair of input voltages, e.g., $V_{\text{bat\_in[1]}}$ and $V_{\text{bat\_in[2]}}$, and passes them to ADC, namely ADC_in. Switch[2:0] selects one battery in battery module to be sensed. Notably, the decoder converts Switch[2:0] into HV_S[i], i = 1–9 and OP_S[7:0] to drive the HV switches, HV subtractors and divider, and LVMUX. Enable is used to turn on or off the HVMUX for power saving. Take an example to acquire the voltage of Battery8 (V_{battery}).

1) First, Switch[2:0] is set to 111.
2) The top and bottom of Battery8 ($V_{\text{bat\_in[9]}}$ and $V_{\text{bat\_in[8]}}$) are selected to HV subtractors and divider by HV switches.
3) Because the OTA in HV subtractors and divider is LV domain, $V_{\text{bat\_in[9]}}$ and $V_{\text{bat\_in[8]}}$ must be scaled down by eight. In other words, the difference of $V_{\text{bat\_in[9]}}$ and $V_{\text{bat\_in[8]}}$ (V_{battery}) is also scaled down by eight.
4) Finally, the LV multiplier is used to restore the V_{battery}.

The function description of each block of HVMUX is given in the following text.

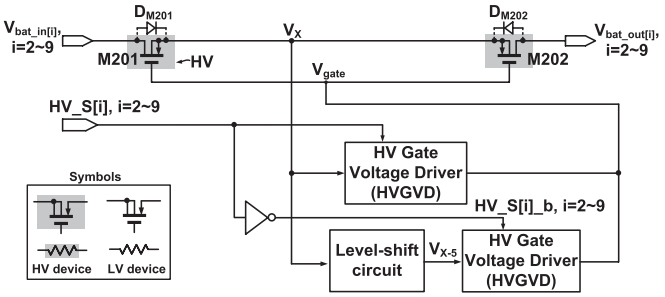

Fig. 4. Schematic of HV switch cell.

A. HV Switches

The HV switches are composed of eight HV switch cells, where each HV switch cell comprises M201, M202, level-shift circuit, HVGVD, and an inverter, as shown in Fig. 4. M201 and M202 are HV devices. D_{M201} and D_{M202} are parasitic diodes of M201 and M202, respectively. Notably, $|V_{\text{gs}}|$ of the HV devices must be smaller than 5 V. In other words, the voltage difference between V_X and V_{gate} must be clamped under 5 V. When V_{gate} is equal to V_X, M201 and M202 are turned off. By contrast, when V_{gate} is equal to $V_X - 5V$, M201 and M202 are turned on. The level-shift circuit is used to generate $V_X - 5V$, namely V_{X-5}. Referring to Fig. 4, the HV switch is driven by HV_S[i], i = 2–9, which chooses $V_{\text{gate}} = V_X$ or $V_{\text{gate}} = V_{X-5}$ by HVGVD. Therefore, M201 and M202 are protected from any over-voltage hazard.

B. HV Gate Voltage Driver

Fig. 5 shows the schematic of HVGVD, including three HV resistors (R_t, R_b, and R_p), MN501, and MP501 − MP507, where MN501 and MP501 are HV devices. Again, $|V_{\text{sg}}|$ of the HV devices must be smaller than 5 V. The V_{sg} of MN501 is driven by HV_S[i], i = 2–9, which is a digital signal. Therefore, MN501 is ensured without any over-voltage hazard. To prevent the over-voltage damage of MP501, the voltage difference between V_X and V_a must be smaller than 5 V. Because V_a is derived from V_X, the voltage range of V_X is

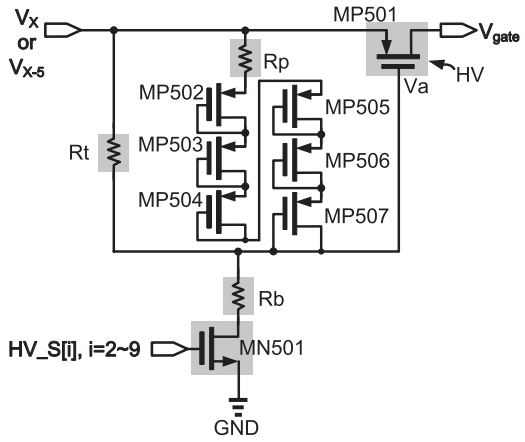

Fig. 5. Schematic of HVGVD.

analyzed in two scenarios, i.e., LV mode ($V_X \leq 5$ V) and HV mode ($V_X > 5$ V).

In HV mode, V_a is clamped by R_p and MP502–MP507. In other words, V_a is constrained by following:

$$V_a = V_X - (V_{R_p} + 6 \times |V_{\text{thp}}|) \tag{1}$$

where V_{R_p} is the voltage drop of R_p, and $|V_{\text{thp}}|$ is the threshold voltage of MN502–MN507. The V_{sg} of MP501 is then written as follows:

$$V_{\text{sg}} \text{ of MP501} = V_{R_p} + 6 \times |V_{\text{thp}}| < 5 \text{ V} \tag{2}$$

where V_{R_p} is negligible because R_p is used to limit the peak current from V_X such that the MP502–MP507 are protected from large current hazards.

In LV mode, V_a is generated by R_t and R_b. Assumed R_t is equal to R_b, V_a is the half of V_X. Thus, V_{sg} of MP501 is half of V_X ($\leq$2.5 V). Therefore, MP501 is also ensured without any over-voltage hazard.

C. Level-Shift Circuit

Level-shift circuit is composed of a current source, I_{bias}, two current mirrors, M601–M604, and a load resistor, R601, as shown in Fig. 6. Current source, I_{bias}, and M601 and M602 are LV devices. M603, M604, and R601 are HV devices. Level-shift circuit generates V_{X-5}, which can be constrained by the following:

$$V_{X-5} = V_X - \text{R601} \times I_3 \tag{3}$$

where I_3 is the current through R601. Assume the voltage difference between V_X and V_{X-5} is equal to 5 V, R601 can be written as

$$\text{R601} = \frac{5}{I_3} = \frac{5}{I_1 + I_2} \tag{4}$$

where I_1 is the drain current of M604, which is supplied by the I_{bias}, I_2 is the input current of HVGVD. Referring to Fig. 5, I_2 can be derived as

$$I_2 = \frac{V_X}{R_t + R_b + R_{o\text{MN501}}} \tag{5}$$

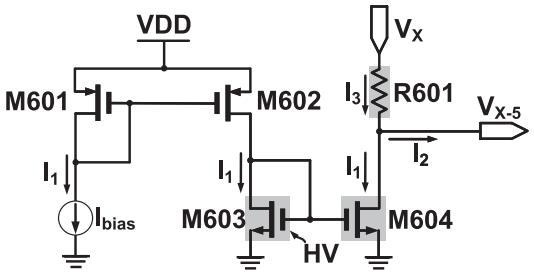

Fig. 6. Schematic of level-shift circuit.

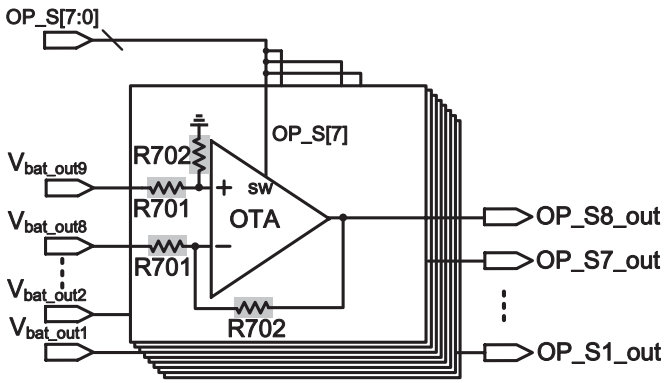

Fig. 7. Schematic of HV subtractors and divider.

where $R_{o\text{MN501}}$ is the output resistor of MN501. Substituting (5) into (4), R601 can be found as

$$\text{R601} = \frac{5}{I_1 + \dfrac{V_X}{R_t + R_b + R_{o\text{MN501}}}}. \tag{6}$$

Equation (6) shows how to calculate the device parameter of R601, where I_1, R_t, R_b, and $R_{o\text{MN501}}$ can be determined based on the limitation of power dissipation.

D. HV Subtractors and Divider

Fig. 7 shows the schematic of HV subtractors and divider composed of an operational transconductance amplifiers (OTA), R701, and R702, where R701 and R702 can be selected based on the voltage and current tolerance.

Take V_{battery} in Fig. 3 as an example, it can be derived as follows:

$$V_{\text{battery}} = \frac{R_{702}}{R_{701}} \times (V_{\text{bat\_in[9]}} - V_{\text{bat\_in[8]}}) \tag{7}$$

where $(V_{\text{bat\_in[9]}} - V_{\text{bat\_in[8]}})$ is the voltage drop of the first battery on the top, while the ratio of R_{702} and R_{701} is utilized to shift the voltage of this battery into a lower voltage range.

A rail-to-rail amplifier topology [21] is adopted to implement the OTA in Fig. 7. The detailed schematic of the OTA is shown in Fig. 8. The input pairs, i.e., n-type and p-type input stages, allow a wide input range. The gain stage use a cascode architecture to boost the gain. The Miller resistors and capacitors in the output stage are in charge of phase compensation. The n-type and p-type common source

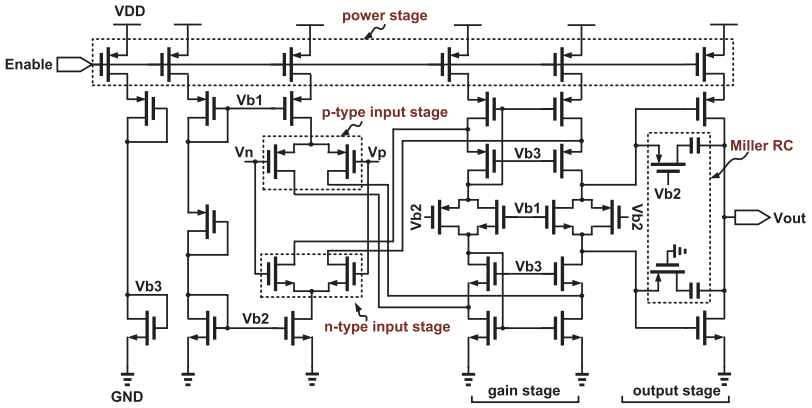

Fig. 8. Schematic of OTA.

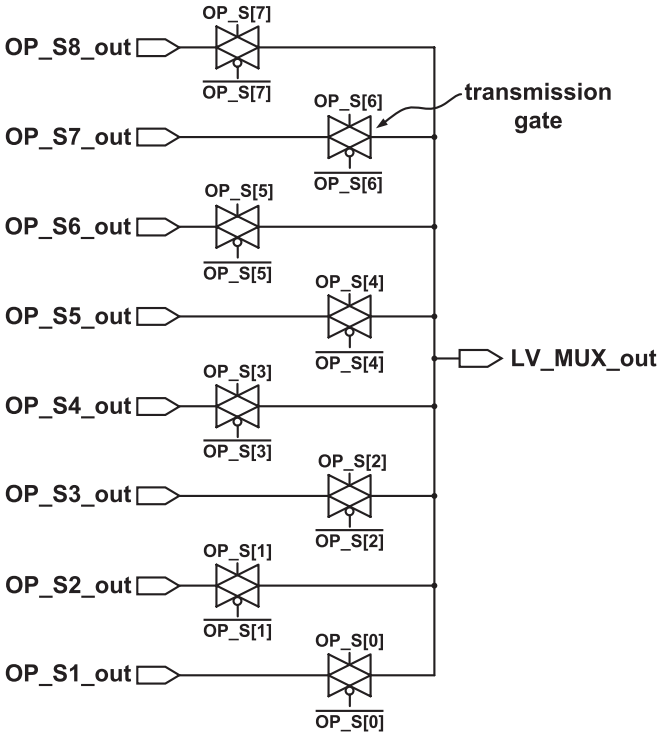

Fig. 9. Schematic of LVMUX.

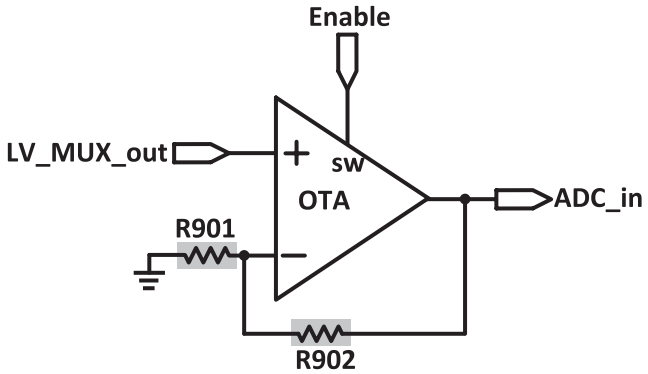

Fig. 10. Schematic of LV multiplier.

amplifiers (output stage) are used to enlarge output voltage range. In addition, enable pin is the power gating signal to activate the entire OTA for the sake of power saving.

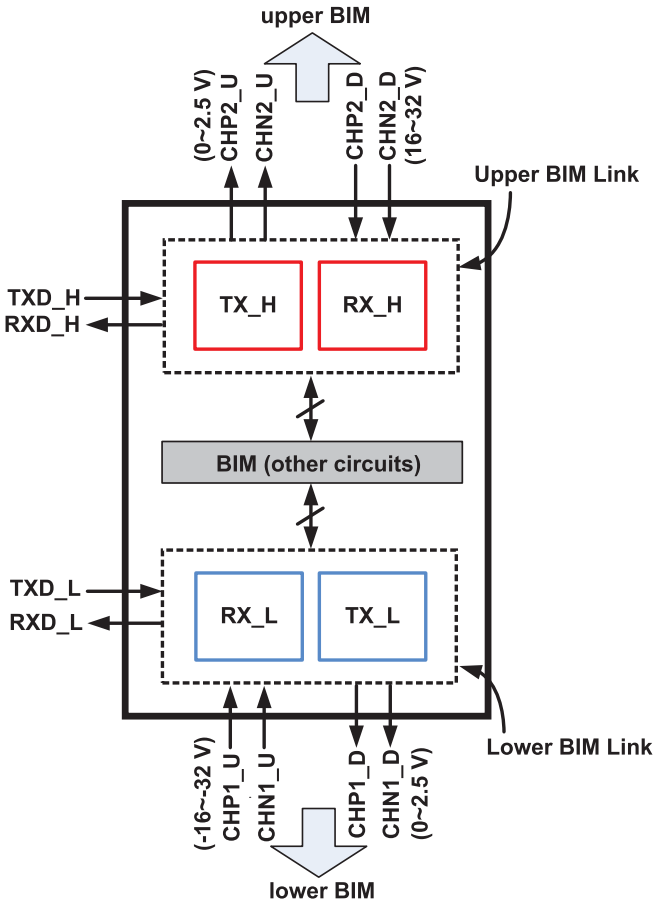

Fig. 11. Floorplan of HV transceiver.

E. LVMUX and LV Multiplier

LVMUX in Fig. 3 is composed of eight transmission gates, which are, respectively, driven by OP_S[0]–OP_S[7], as shown in Fig. 9. LVMUX selects one of OP_S8_out–OP_S1_out to be LV_MUX_out. The last stage in Fig. 3 is LV multiplier, as shown in Fig. 10. LV multiplier multiplies the voltage at LV_MUX_out with R_{902}/R_{901} to generate a scaled output voltage, ADC_in, for the following ADC in Fig. 2:

$$\text{ADC\_in} = \left(1 + \frac{R_{902}}{R_{901}}\right) \times \text{LVMUX\_out} \tag{8}$$

TABLE I
FUNCTIONALITIES OF HV TRANSCEIVER

Name	Functionality
TX_H	BIM transmits data (TXD_H) to upper BIM by CHP2_U and CHN2_U.
RX_H	BIM receives differential signals (CHP2_D and CHN2_D) from the upper BIM.
TX_L	BIM transmits data (TXD_L) to lower BIM by CHP1_D and CHN1_D.
RX_L	BIM receives differential signals (CHP1_U and CHN1_U) from the lower BIM.

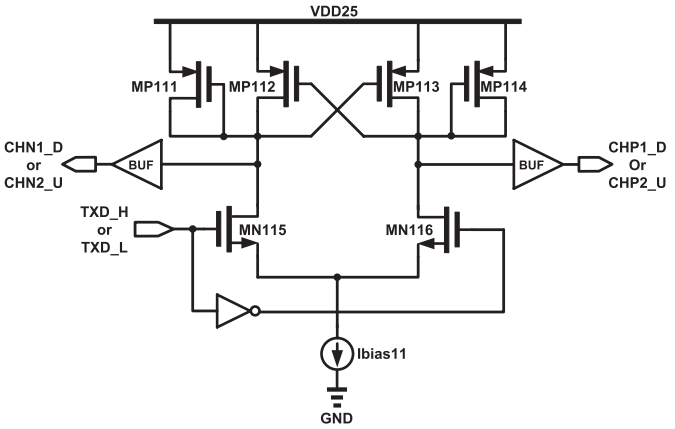

Fig. 12. Schematic of TX_H and TX_L [22].

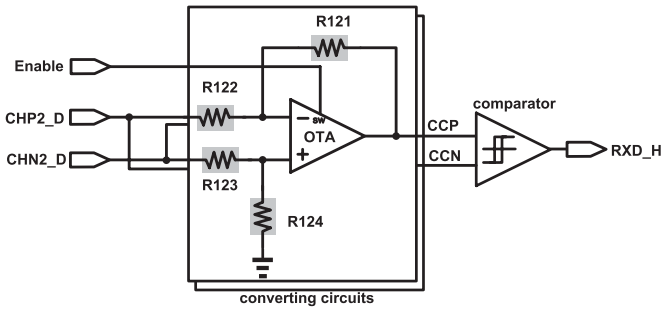

Fig. 13. Schematic of RX_H.

where R_{902} and R_{901} are used to adjust the LV_MUX_out into the voltage range of ADC, and LV_MUX_out is the output voltage of LVMUX.

IV. HV TRANSCEIVER

Referring to Figs. 1 and 2 again, HV transceiver is composed of upper BIM link and lower BIM link, as shown in Fig. 11. Upper BIM link is used to communicate with the upper adjacent BIM by TX_H and RX_H. By contrast, lower BIM link is in charge of communicating with the lower adjacent BIM by TX_L and RX_L. The functionalities of HV transceiver are summarized in Table I. Notably, RX_H must receive positive HV signals (assumed using in a series of eight batteries and common voltage is 16–32 V) from the upper adjacent BIM, and RX_L receive negative HV signals (common voltage: −16 to −32 V) from the lower adjacent BIM.

A. TX_H and TX_L

The two transmitters, TX_H and TX_L, are used to transfer data to upper and lower adjacent BIMs at the same time. Therefore, they are realized using same circuits to convert TXD_H (or TXD_L) to CHN1_D and CHP1_D (or CHN2_U and CHP2_U), as shown in Fig. 12 [22], where BUF is a buffer to supply a large drive current. Referring to Fig. 12, M111–M114 consists of a cross coupling and positive feedback loop to speed up the transition. In addition, it can decrease the phase delay between CHN1_D and CHP1_D (or CHN2_U and CHP2_U). Most important of all, the voltage swing of all outputs is from VDD25 (2.5 V) to GND (0 V) for control logic.

B. RX_H and RX_L

To receive data from upper and lower adjacent BIMs, the two receivers, RX_H and RX_L, must convert the positive and negative HV signals (16–32 V and −16 to −32 V) into 0–2.5 V. Notably, they are equipped with HV tolerance. Fig. 13 shows the schematic of RX_H, including two converting circuits and a comparator with hysteresis [23]. The converting circuit has to convert the CHP2_D and CHN2_D into the input range of the following comparator. Each converting circuit consists of OTA, R121–R124, generating CCP and CCN voltage references. CCP is constrained by the following:

$$\begin{aligned}\text{CCP} = \text{CHN2\_D} \times \frac{R124}{R123+R124} \times \left(1+\frac{R121}{R122}\right) \\ -\text{CHP2\_D} \times \frac{R121}{R122}\end{aligned} \tag{9}$$

where the first term at the right hand is adjusted as a common voltage. The conversion function is based upon the linear mapping from 16–32 to 0–2.5 V such that the ratios of R121/R122 and R124/R123 can be easily calculated. Similar to CCP, CCN is also derived. Therefore, the comparator can compare CCP with CCN to generate RXD_H. Assumed R122 and R123 are more than 10 times of R121 and R124. RXD_H can be rewritten as

$$\begin{aligned}\text{RXD\_H} = A_o \times (\text{CHP2\_D} - \text{CHN2\_D}) \\ \times \left(\frac{R121}{R122}+\frac{R124}{R123}\right)\end{aligned} \tag{10}$$

where A_o is the dc gain of the comparator and is far larger than the last term (R121/R122 + R124/R123). Therefore, when CHP2_D is larger than CHN2_D, RXD_H is pulled high as logic 1. By contrast, when CHP2_D is lower than CHN2_D, RXD_H is pulled low as logic 0.

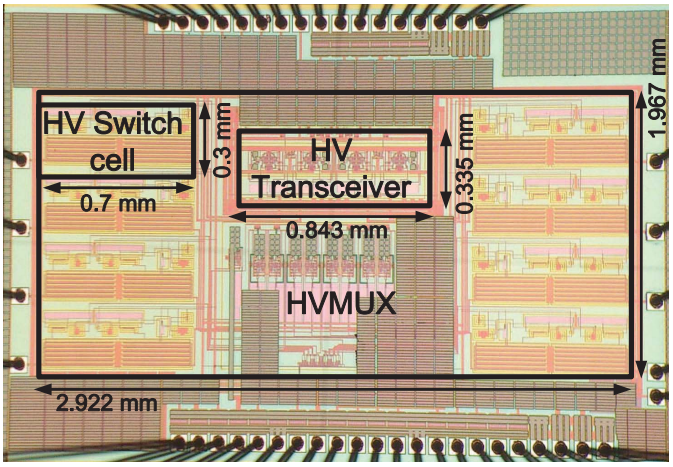

Fig. 14. Die photo of the proposed design.

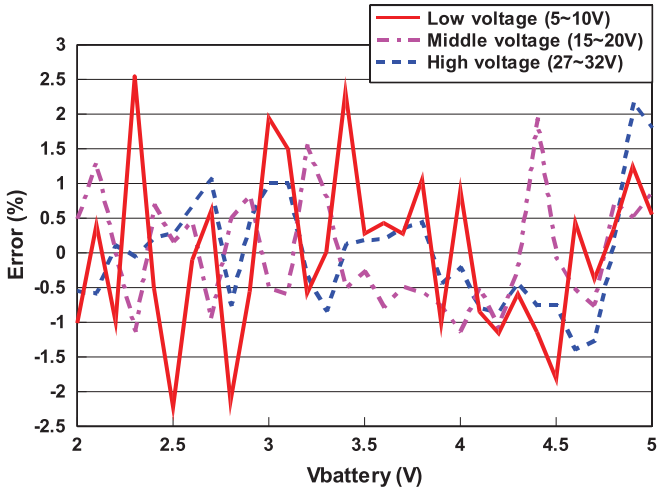

Fig. 15. Error distribution given three different input range of HVMUX.

By contrast, RX_L is in charge of converting negative HV signals from (−16 to −32 V) into (0 to 2.5 V). The schematic of RX_L is similar to that of RX_H. Notably, the output of RX_L is RXD_L, as shown in Fig. 11.

V. Implementation and Measurement

The proposed design is implemented using 0.25 μm 1-poly 3-metal 60 V BCD process to justify the performance. Fig. 14 shows the die photo of the proposed voltage monitoring IC on silicon. The core area is 2.922 × 1.967 mm^2, where the area of one HV transceiver and one HV switch cell are 0.843 × 0.335 and 0.7 × 0.3 mm^2, respectively.

Fig. 15 shows the error distribution of HVMUX given three different input ranges, where V_{battery} is voltage of battery from 2 to 5 V. These input ranges are described as follows.

1) LV (5–10 V): lower range of input voltage range in HVMUX.
2) Middle voltage (15–20 V): typical range of input voltage range in HVMUX.

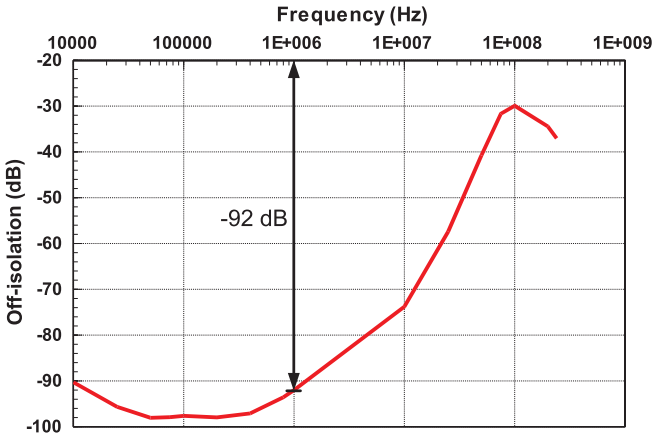

Fig. 16. Measurement results of off-isolation of HVMUX.

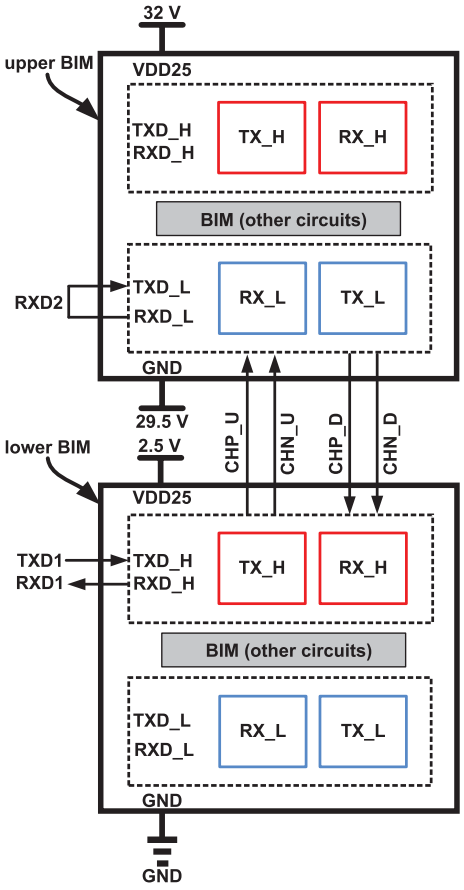

Fig. 17. Measurement configuration of the proposed HV transceiver.

3) HV (27–32 V): upper range of input voltage range in HVMUX.

The worst-case error of HVMUX is less than ±2.54%. Fig. 16 shows the off-isolation of HVMUX. Given a normal 1 MHz data rate, the performance of off-isolation achieves −92 dB. Therefore, the proposed HVMUX will not be contaminated by digital control logic signals in Fig. 2.

The measurement setting of the proposed HV transceiver is shown in Figs. 17 and 18. TXD1 is the input data. The lower BIM transmits data to the upper BIM by CHP_U

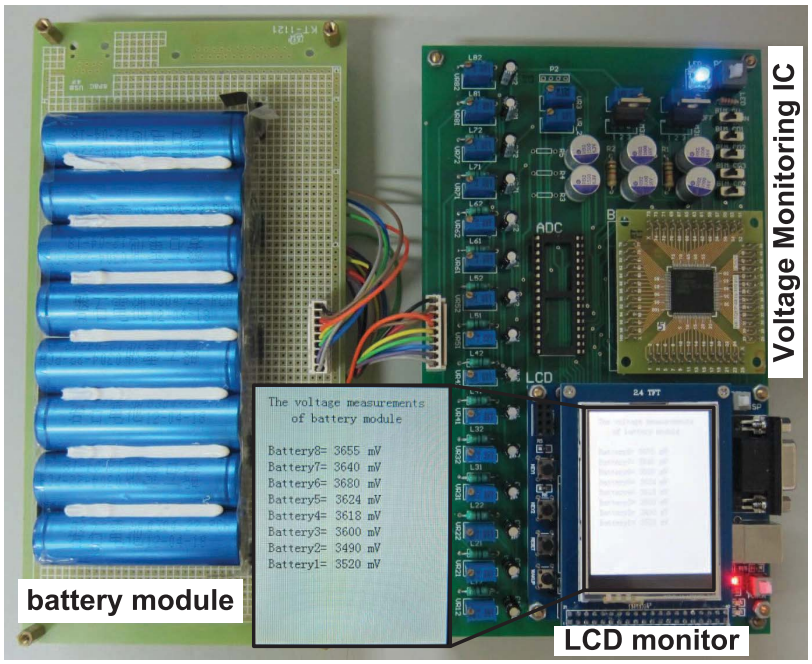

Fig. 18. Photo of the measurement prototype with the proposed voltage monitoring IC.

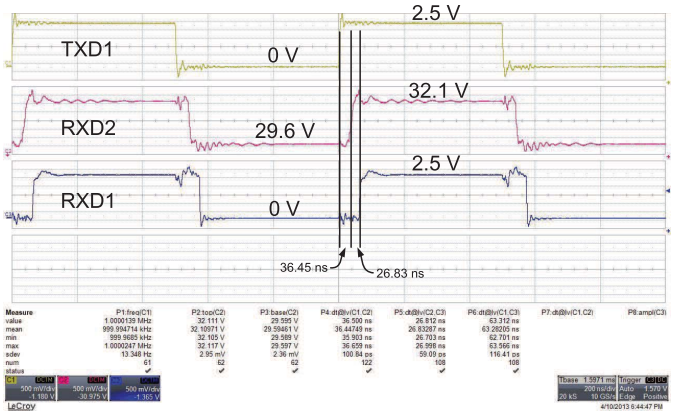

Fig. 19. Measurement results of HV transceiver.

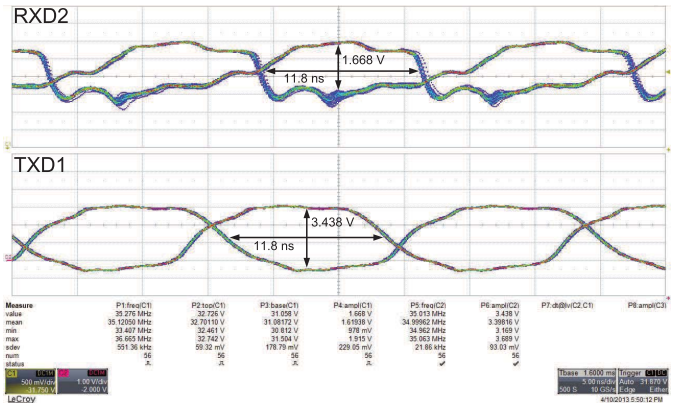

Fig. 20. Eye diagrams of HV transceiver given 70 Mb/s data rate (maximum) from lower BIM to upper BIM.

and CHN_U. The upper BIM receives the data to generate RXD2, and then it transmits the data to the lower BIM. Finally, the lower BIM receives the data to generate RXD1.

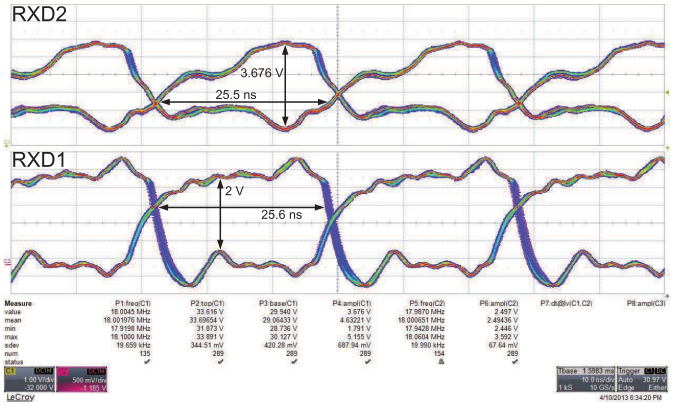

Fig. 21. Eye diagrams of HV transceiver given 36 Mb/s data rate (maximum) from upper BIM to lower BIM.

All of the measurement results are shown in Fig. 19. All of these signals, TXD1, RXD2, RXD1, should demonstrate the same logic values, except the delays there between. The propagation delays are 36.45 and 26.83 ns, respectively. The eye diagrams of HV transceiver given maximum data rates are also measured, as shown in Figs. 20 and 21. The maximum date rate from TX_H to RX_L and from TX_L to RX_H are 70 and 36 Mb/s, respectively.

The performance of the proposed HVMUX and HV transceiver is summarized and compared with several prior works in Tables II and III. Referring to Table II, our proposed HVMUX without SOI technology attains the second best isolation, −92 dB@1 MHz. Referring to Table III, the proposed HV transceiver achieves the second best propagation delay and power dissipation. Most important of all, no isolator nor any discrete (opto-couplers) is needed in our proposed HV transceiver.

TABLE II
COMPARISON BETWEEN THE PROPOSED HVMUX AND PRIOR WORKS

Specifications	This work	[7]	[9]	[8]	[17]
Year	2013	2005	2008	2011	2012
Results	Measured	Measured	Measured	Measured	Post-sim
Process (μm)	0.25 μm 60 V BCD	0.35 μm SOI	30 V CMOS/SOI	0.35 μm 50 V CMOS	0.25 μm 60 V BCD
Number of switches	8	32×32	16	4	8
Analog input range	4∼32 V	-40∼40 V	-5∼25 V	0∼40 V	2∼29.2 V
Isolation	-92 dB@1 MHz	-53 dB@4 MHz	-45 dB@0.2 MHz	-90 dB@10 MHz	-79.4 dB@10 MHz
Power dissipation	18.781 mW	10 mW/switch	<15 mW	N/A	17.79 mW
Area	3.45 mm^2	N/A	N/A	N/A	1.95 mm^2

TABLE III
COMPARISON BETWEEN THE PROPOSED HV TRANSCEIVER AND PRIOR WORKS

Specifications	This work	[3]	[14]	[12]
Year	2013	2003	2005	2012
Results	Measured	Measured	Measured	Measured
Process (μm)	0.25 μm 60 V BCD	GaAs & BiCMOS	SOI	5V CMOS
Maximum data rate	70 Mbps	25 Mbps	1 Mbps	250 Mbps
Communication between adjacent BIMs	4 wires	2 wires	4 wires	4 wires
Number of isolator	0	2 opto-couplers	4 capacitors	2 transformers
Propagation delay	26.83∼36.45 ns	>40 ns	30∼80 ns	5.5 ns
Power dissipation	10.1 mW	20∼100 mW	40 mW	8 mW
Area	0.282 mm^2 2×(Tx & Rx)	N/A	N/A	0.12 mm^{2†} (Tx & Rx)

(†) Not include the area between Tx and transformer

VI. CONCLUSION

In this paper, we propose a total HV solution on silicon for BIMs. The proposed design is implemented using a typical 0.25 μm 1-poly 3-metal 60-V BCD process such that it can be easily integrated in a possible SoC solution for BMS. The measurement results justify our design to be a high performance analog HV multiplexer (HVMUX) with HV transceiver. The error of the proposed HVMUX is smaller than 2.54% from 5 to 32 V, as shown in Fig. 15. In addition, the off-isolation of HVMUX is -92 dB@1 MHz. Lastly and most importantly, the proposed HV transceiver does not need additional discrete components and isolators.

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