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A 2×VDD output buffer with PVT detector for slew rate compensation

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ABSTRACT

A novel PVT (process, voltage, temperature) detection and compensation technique is proposed to automatically adjust the slew rate of a 2×VDD output buffer. The threshold voltage (Vth) of PMOSs and NMOSs varying with process, supply voltage, and temperature (PVT) is detected, respectively. Based on the detected PVT corner, the output buffer will turn on different current paths correspondingly to either increase or decrease the output driving current such that the slew rate of the output can be adjusted as well. The proposed design is implemented using a typical 90 nm CMOS process to justify the slew rate performance. By the on-silicon measurements, the slew rate of output signal is compensated over 26%, the maximum slew rate is 1.65 (V/ns), the maximum data rate is 330 MHz given 1.2/0.9 V supply voltage with a 20 pF load, the core area of the proposed design is 0.056×0.406 mm^2, and the power consumption is 2.2 mW at 330 MHz data rate.

1. Introduction

It is well known that the process, voltage, and temperature (PVT) variation severely degrades performance and yield. Particularly, such a phenomenon is worsen in nano-scale processes. Fig. 1 shows that the performance of IC, in fact, is seriously affected by PVT variation [1]. Therefore, many recent works have proposed different techniques to enhance the capability against PVT variation and enlarge the acceptable envelope as much as possible to enhance the yield. Though the logic delay method has been widely utilized to detect PVT variation [2–7], it can only recognize three corners, i.e., TT, FF, and SS. By contrast, the FS and SF corners have been long ignored in these delay-based methods. This work, by contrast, proposes a novel corner detection technique to detect all process corners, i.e., TT, FF, SS, SF, and FS.

I/O buffers unavoidably are also bothered by the PVT variations. Particularly, the slew rate of the output of these buffers, namely the output buffer, is often required to meet different I/O interface standards, e.g., PCI, ATA, PCI-express, etc. Many mixed-voltage I/O buffers were reported to resolve the slew rate issues [8,9] and various voltage level issues [10–13]. Sawigun et al. proposed a low-power consumption, high slew rate, and high signal-to-noise I/O buffer based on a compact class-AB transconductance amplifier circuit with rail-to-rail CMR (common-mode range) [9]. However, the transmitting and receiving frequencies of this work and other previous works were not fast enough to meet certain specifications, e.g., PCI-express, which is up to 266 MHz. Therefore, a wide range I/O buffer able to simultaneously transmit and receive high-speed signals is deemed as a total solution for these scenarios. To communicate the signal with large voltage swings, stacked transistors are used in the output stage to avoid the gate-oxide overstress [14–18]. Moreover, for the high-speed interface circuits, the specification of the slew rate is definitely required by communication system protocols, as shown in Table 1 [2]. Thus, the high-speed output buffer is needed to self-adjust the slew rate by using compensation mechanism, as shown in Fig. 2.

2. 2×VDD output buffer circuit design

Fig. 3 shows the block diagram of the proposed output buffer, which is composed of PVT sensors, PVT decider, and a 2×VDD output buffer. The PVT sensors consist of PMOS process sensor, NMOS process sensor, and voltage & temperature sensor. The PVT decider comprises three comparators, a V_{Bias} generator, and a digital circuit.

2.1. The PMOS process sensor

Fig. 4 shows the schematic of the PMOS process sensor in Fig. 3, comprising 2 cascaded PMOS source followers. The PMOS source

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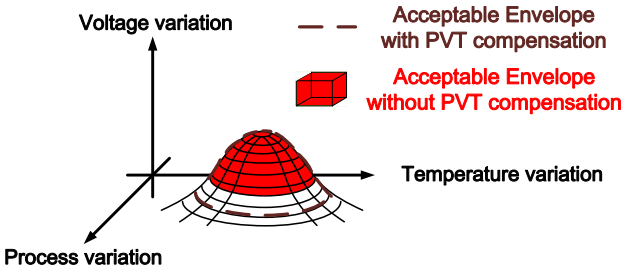

Fig. 1. Performance envelope as a function of process and temperature variation.

Table 1
Slew rate specifications of ATA.

ATA mode	Signal frequency (MHz)	Slew rate specification (V/ns)
UDMA33	8.25	Min. t_r, t_r 5
UDMA66	16.5	Max. 1.25
UDMA100	25	0.4–1.0

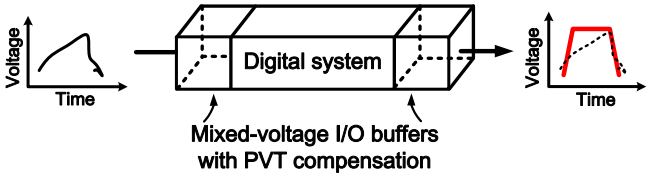

Fig. 2. The slew rate is compensated through our design.

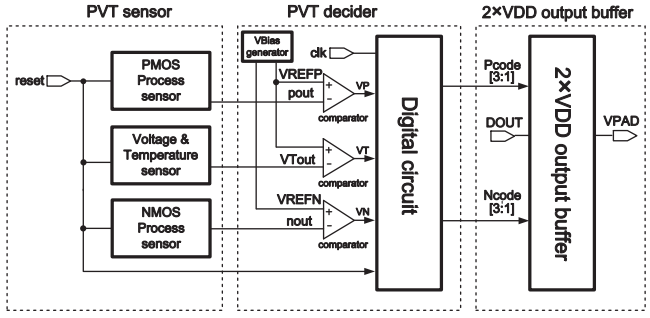

Fig. 3. The block diagram of the proposed output buffer.

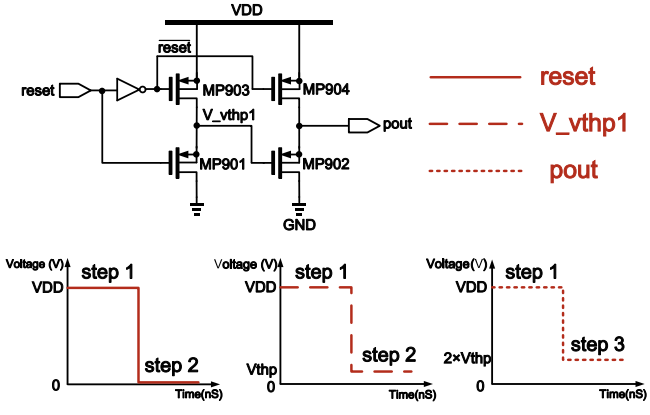

Fig. 4. Schematic of the PMOS process sensor.

follower is composed of MP901–MP904. The function description of this sensor circuit is given as follows:

(1) Step 1: When the reset is activated high, V_vthp1 and pout are pulled high to VDD (=1.2 V).

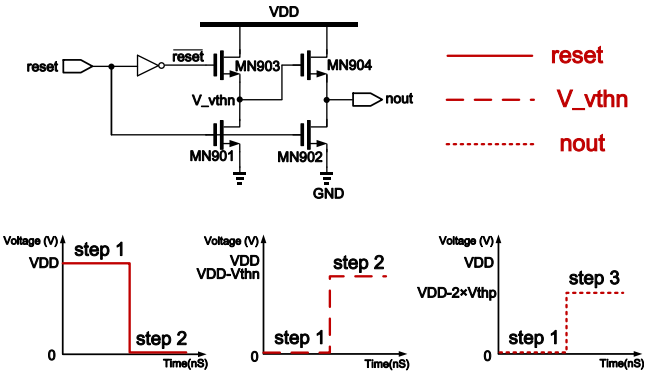

Fig. 5. Schematic of the NMOS process sensor.

(2) Step 2: When the reset is pulled low, V_vthp1 is discharged till Vthp, which is the threshold voltage of MP901.
(3) Step 3: By a similar operation, pout will be discharged till 2×Vthp in the next repeated cycle as the previous steps 1 and 2. In other words, the variation of PMOS threshold voltage is "magnified" twice at the output, pout.

Finally, the voltage of pout is delivered to the following PVT decider to detect the PMOS corner.

2.2. The NMOS process sensor

The schematic of the NMOS process sensor, as shown in Fig. 5, which is deemed as the dual circuit of the PMOS sensor. The NMOS process sensor uses 2 cascaded NMOS source followers, which are composed of MN901–MN904. The NMOS process sensor detects the NMOS threshold voltage deviation by using MN901–MN904.

(1) Step 1: When the reset is activated high, V_vthn and nout are pulled low to GND (=0 V).
(2) Step 2: After the reset is pulled low, V_vthn is charged till VDD-Vthn, where Vthn is the threshold voltage of MN904.
(3) Step 3: By a similar operation, nout will be charged till VDD-2×Vthn in the next repeated cycle as the previous steps 1 and 2. That is, the 2 cascaded NMOS source followers generate a VDD-2×Vthn voltage, which is nout, to transmit to PVT decider.

Again, the cascaded source follower again "magnifies" the NMOS threshold voltage and the variation therewith.

2.3. The voltage & temperature sensor

Fig. 6 shows the schematic of the voltage & temperature sensor. This sub-circuit uses cascaded source followers to generate 2×Vthp, which is similar to the PMOS process sensor. The major difference is that all bulks are coupled to VDD to generate the body effect in each PMOS. By monitoring the Vthp variation of PMOS transistor, the voltage and temperature variations can be derived as long as the bulk of the PMOS transistor is coupled to VDD. The theory behind this design is given as follows:

(1) According to Eq. (1), the Vthp of MOS with body effect will drift at different Vbs, which is the voltage difference between VDD and source voltage of MOS. Notably, Vthp0 is the no body effect threshold voltage, γ_p is the body effect coefficient, Vfn is the bulk surface potential, and Vbs is the voltage difference

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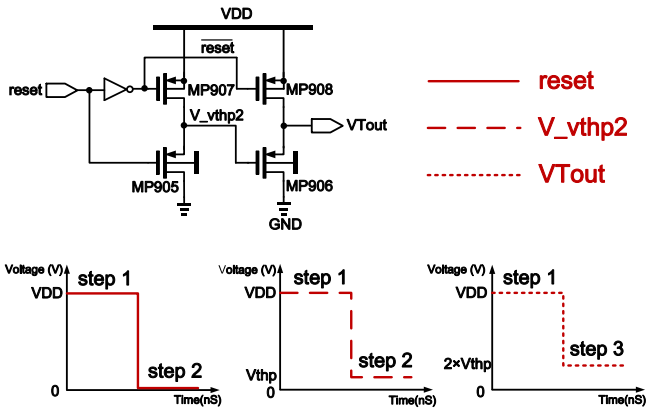

Fig. 6. Schematic of the voltage & temperature sensor.

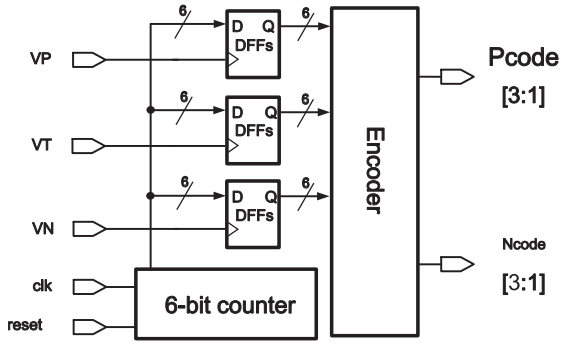

Fig. 7. Schematic of the digital circuits.

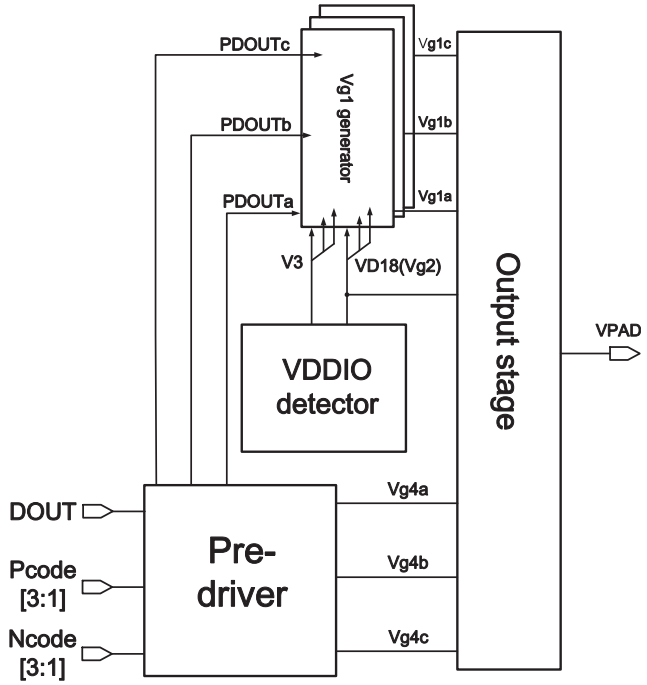

Fig. 8. Schematic of the 2×VDD mixed-voltage tolerant output buffer.

between bulk and source of MOS. In short, when supply voltage variation affects Vbs, Vbs also affects Vthp

$$Vthp = Vthp0 + \gamma_p\left(\sqrt{2|Vfn| + Vbs} - \sqrt{2|Vfn|}\right) \quad (1)$$

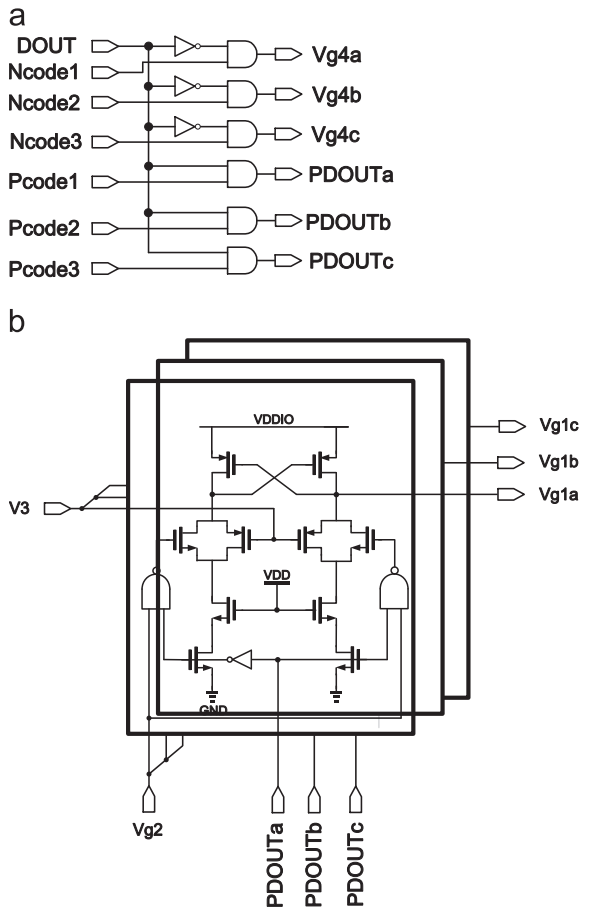

Fig. 9. Schematic of (a) the Pre-driver and (b) the Vg1 generator.

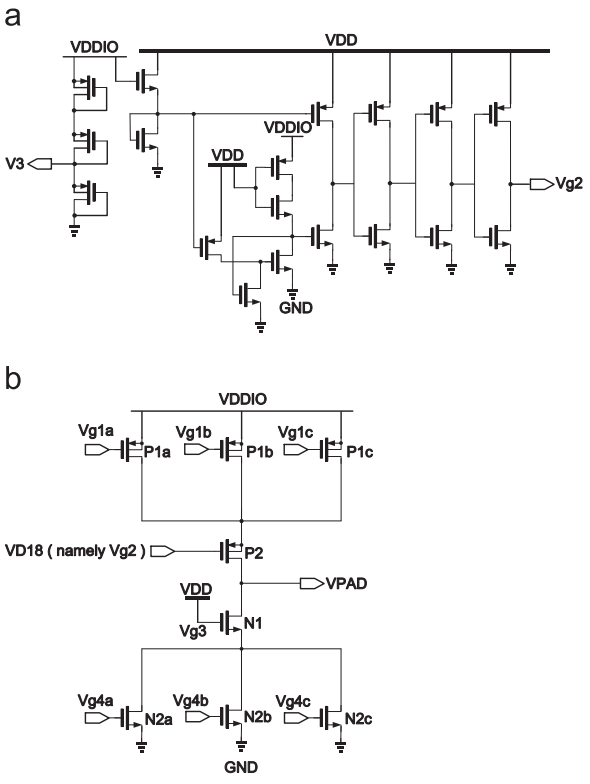

Fig. 10. Schematic of (a) the VDDIO detector and (b) the output stage.

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where γ_p can be written as $\gamma_p = \sqrt{2q\varepsilon_s N_A}/C_{ox}$, q is electronic charge, ε_s is silicon dielectric constant, N_A is doping concentration, and C_{ox} is oxide capacitance.

(2) The γ_p of the Vthp comprises temperature factors. Thus, the threshold voltage is affected as well. Notably, Vthp voltage has a negative temperature coefficient around −1 mV/°C

Thus, the 2 cascaded source followers generate 2×Vthp voltage, namely VTout, with VDD and temperature variation.

2.4. The PVT decider

Depending on the outputs of the mentioned three sensors, the PVT decider derives two digital codes, Pcode [3:1] and Ncode [3:1], to show the sensed PVT status. The PVT decider consists of a V_{Bias} generator, three comparators, and a digital circuit, as shown in Fig. 3. Fig. 7 shows the block diagram of the digital circuits composed of a 6-bit counter, an encoder, and D flip-flops. When pout, TVout, and nout reach the reference voltage VREFP and VREFN, respectively, comparators deliver, VP, VT, and VN, respectively, to latch D flip-flops (DFFs). According to the sensed corners, encoder will generate two codes, Pcode [3:1] and Ncode [3:1]. The codes indicate the required compensation status so as to control the output currents in the 2×VDD output buffer.

2.5. 2×VDD output buffer

Fig. 8 shows the 2×VDD output buffer composed of a Pre-driver, a Vg1 generator, a VDDIO detector, and an output stage. The Pre-driver generates six signals, PDOUTa–c, Vg4a–c, based on three received signals, DOUT, Pcode [3:1], and Ncode [3:1], so as to adjust output currents. The VDDIO detector and Vg1 generator will then generate appropriate gate drive voltages in different voltage modes without leakage currents and overstress problems [7].

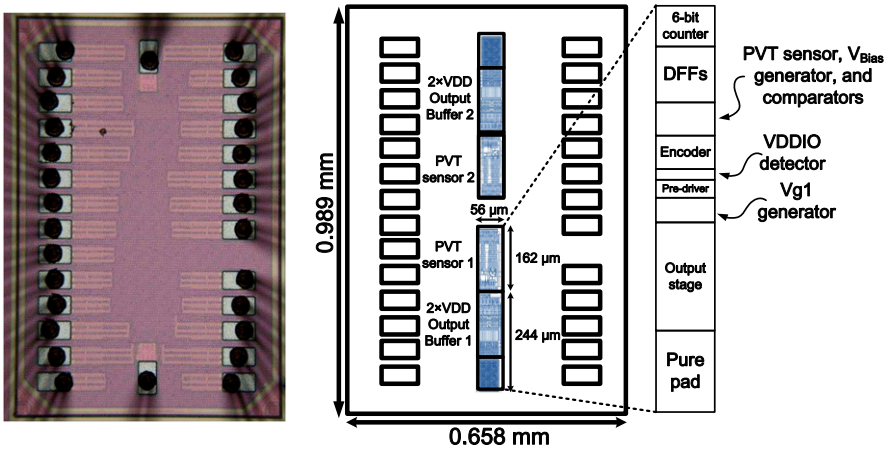

Fig. 11. Die photo of the proposed design.

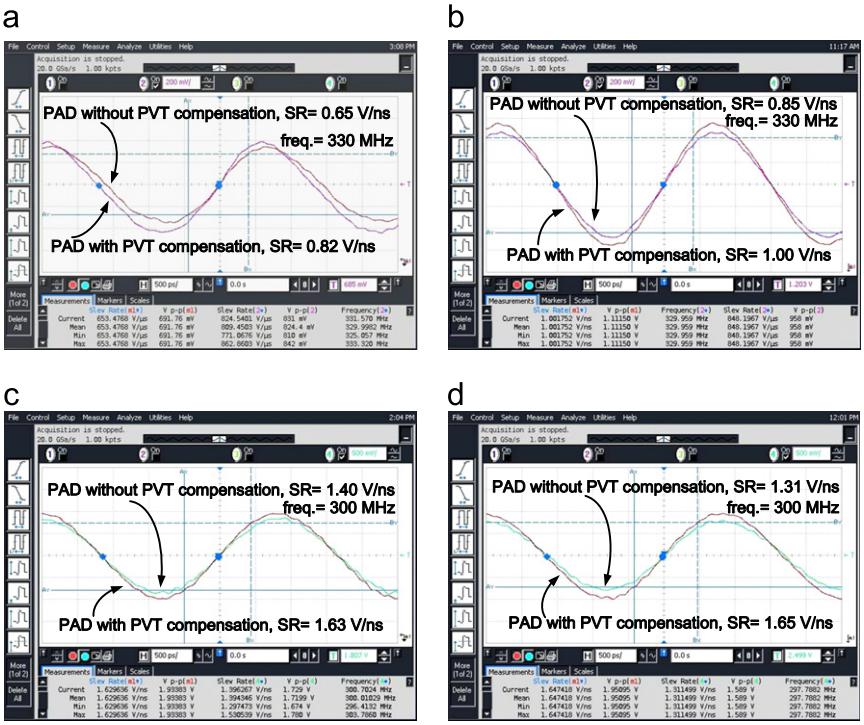

Fig. 12. Measured the uncompensated and compensated VPAD for different VDDIO voltages: (a) VDDIO = 0.9 V, (b) VDDIO = 1.2 V, (c) VDDIO = 1.8 V, and (d) VDDIO = 2.5 V.

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2.5.1. The Pre-driver

Fig. 9(a) shows the Pre-driver schematic, which is basically a decoder. It is composed of digital logic circuits, which accepts Pcode [3:1], and Ncode [3:1] signals from the three sensors. After decoding Pcode [3:1] and Ncode [3:1] signals, the current paths in the output buffer are selected.

2.5.2. The Vg1 generator

The Vg1 generator is composed of three voltage level converters, as shown in Fig. 9(b). The Vg1x, x=a, b, c, generators accept

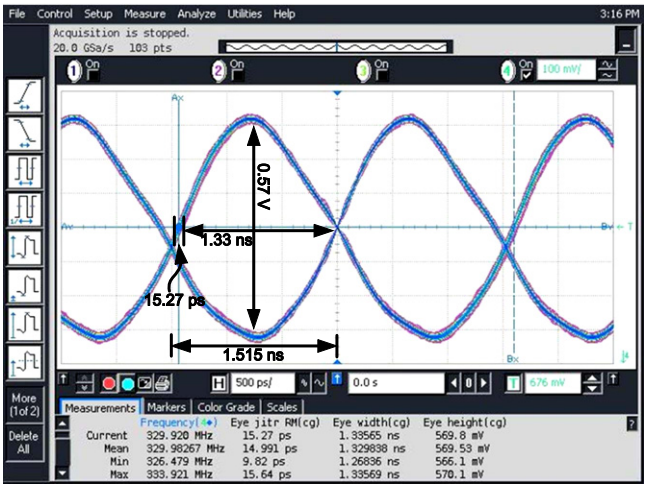

Fig. 13. The uncompensated eye diagram of VPAD with VDDIO=0.9 V in Tx mode.

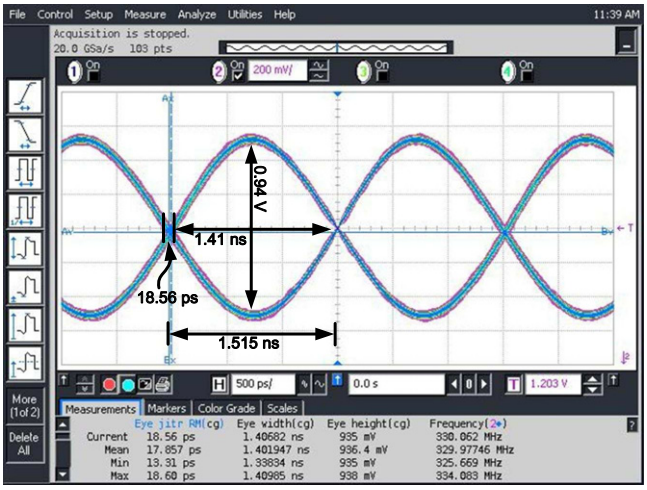

Fig. 14. The uncompensated eye diagram of VPAD with VDDIO=1.2 V in Tx mode.

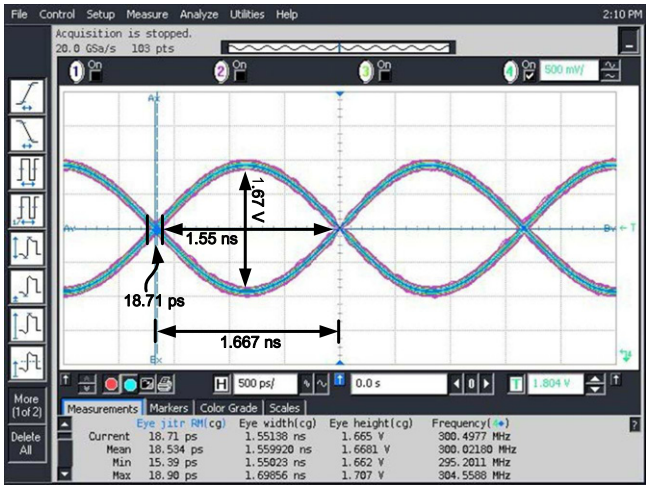

Fig. 15. The uncompensated eye diagram of VPAD with VDDIO=1.8 V in Tx mode.

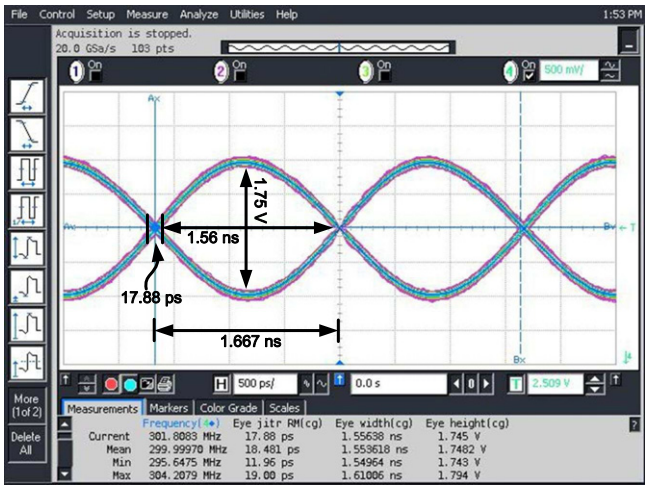

Fig. 16. The uncompensated eye diagram of VPAD with VDDIO=2.5 V in Tx mode.

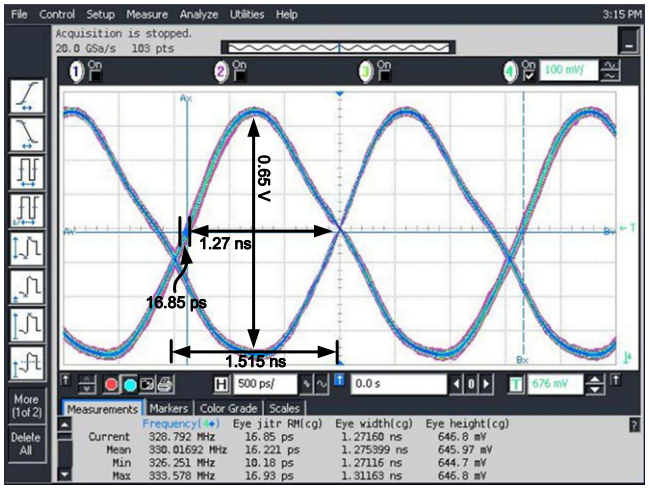

Fig. 17. The compensated eye diagram of VPAD with VDDIO=0.9 V in Tx mode.

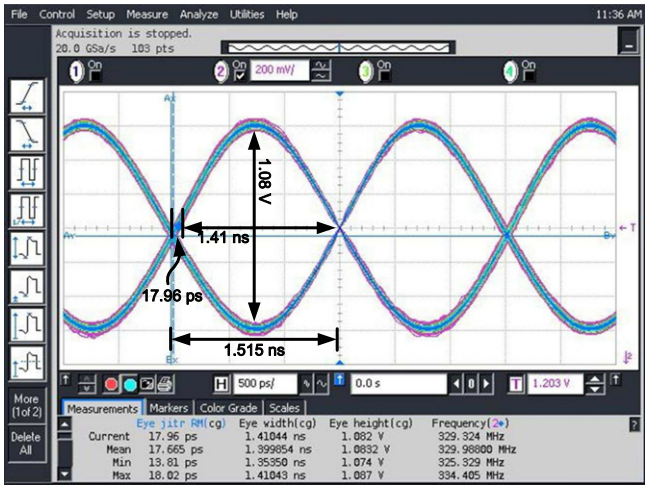

Fig. 18. The compensated eye diagram of VPAD with VDDIO=1.2 V in Tx mode.

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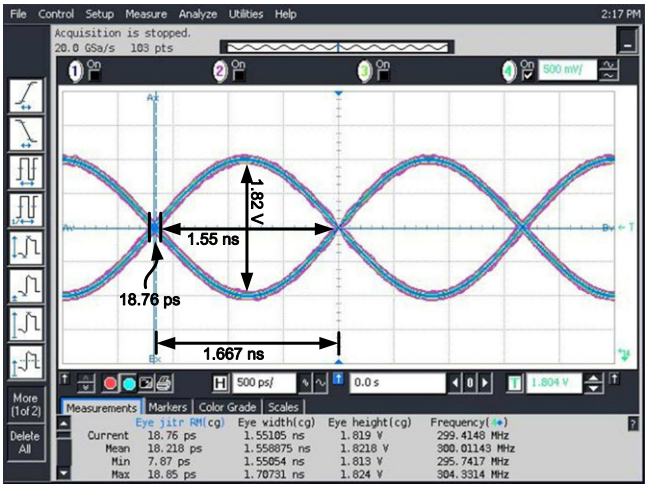

Fig. 19. The compensated eye diagram of VPAD with VDDIO = 1.8 V in Tx mode.

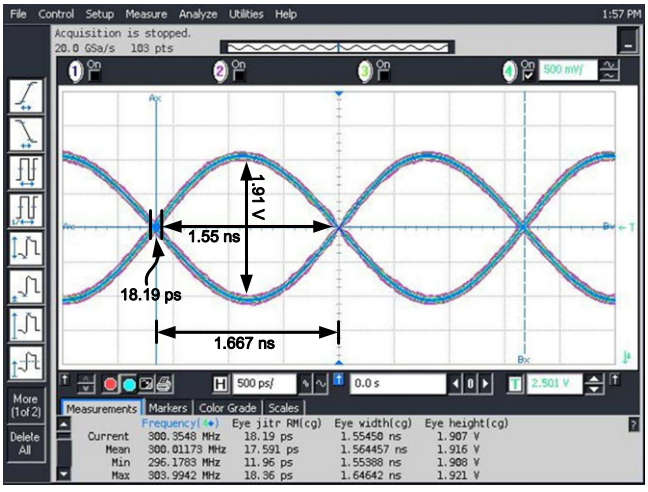

Fig. 20. The compensated eye diagram of VPAD with VDDIO = 2.5 V in Tx mode.

the Pre-driver signals (PDOUTx) and Vg2 from VDDIO detector to generate voltages, to prevent over-voltage hazards in the output stage.

2.5.3. The VDDIO detector

Fig. 10(a) shows the VDDIO detector of the proposed 2×VDD output buffer. The detector circuit provides a 1.2 V gate drive on P2 to prevent the stress problem of the transistor gate oxide when VDDIO = 1.8/2.5 V. On the other hand, the detector circuit will apply 0 V on P2 gate drive to prevent the stress problem of the transistor gate oxide when VDDIO = 1.2 V.

2.5.4. The output stage

Fig. 10(b) shows the output stage of the proposed 2×VDD output buffer circuit. The supply voltage (VDD) of the core circuits using 90 nm CMOS process is 1.2 V. Thus, the output stage must be realized using two groups of stacked PMOS and NMOS transistors, respectively, for transmitting 2×VDD (≈2.5 V) signals. PMOSs P1a–P1c are in parallel such that the slew rate of the output signal can be compensated by turning on or off the current paths flowing through P1a–P1c individually. According to the detected different process and temperature status, Pcode [3:1] and Ncode [3:1] will select the number of turned-on PMOSs of the output stage. The switching status of N1a–N1c are corresponding to PMOSs mentioned in the above. P1a–P1c and N1a–N1c are designed with different sizes to generate different currents to compensate the slew rate of the output signal.

3. Implementation and measurement results

This work is implemented using 90 nm CMOS technology without any thick-oxide device. Fig. 11 shows the die photo of this work, where the overall chip size is only 0.658×0.989 mm^2, the core size is 0.056×0.406 mm^2, and the compensation circuit is 0.056×0.162 mm^2. Thus, the area overhead is less than 40% for a single I/O buffer. The uncompensated and compensated VPAD signals given VDDIO = 0.9/1.2/1.8/2.5 V in Tx mode are shown in Fig. 12. The slew rate after compensation is enhanced to 0.82 (V/ns) from 0.65 (V/ns), which is 26% when VDDIO = 0.9 V.

Table 2
Compensation results at different VDDIOs.

VDDIO	0.9 V	1.2 V	1.8 V	2.5 V
Data rate (MHz)	330	330	300	300
Eye jitter (ps)	16.85	17.96	18.76	18.19
Eye width (ns)	1.27	1.41	1.55	1.55
Eye height (V)	0.65	1.08	1.82	1.91
Slew rate improvement (V/ns)	26% (0.65→0.82)	18% (0.85→1.00)	14% (1.40→1.63)	23% (1.31→1.65)

Table 3
Performance comparison of output buffer.

Specification	[2] *JSSC*	[8] *ECCTD*	[11] *TCAS-I*	[12] *TCAS-I*	[9] *TCAS-II*	This work
Year	2003	2007	2009	2010	2012	2012
Process (μm)	0.18	0.35	0.35	0.18	0.35	0.09
Supply voltage (V)	3.3	3.3	3.3	1.8	3	1.2
Transmitting voltage mode (V)	3.3	1.4	1.8/3.3/5.0	0.9/1.2/1.82.5/3.3/5.0	3	0.9/1.2/1.8/2.5
Results	Measured	Measured	Measured	Measured	Measured	Measured
Data rate (MHz)	N/A	N/A	80/120/84	10/40/50/2.5/3.3/5.0	N/A	330/330/300/300
Slew rate (V/ns)	0.40–0.99	0.37	Max. 0.71	NA	0.81	0.82/1/1.63/1.65
Process corners, detected	TT, FF, SS	N/A	N/A	N/A	N/A	TT, FF, SS, FS, SF
Slew rate improvement	32%	N/A	N/A	N/A	100%	26% /18% /14% /23%

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The maximum slew rate is 1.65 (V/ns) when VDDIO=2.5 V. The uncompensated and compensated eye diagrams of VPAD are shown in Figs. 13–16 and Figs. 17–20, respectively. The eye is widen by 14/15/9/9% when VDDIO=0.9/1.2/1.8/2.5 V, respectively. The best improvement occurs when VDDIO=0.9 V, and the fastest data rate is 330 MHz when VDDIO=0.9 V. This work attains the edge of all PVT corner detection, and the maximum slew rate. The performance of the proposed design is summarized in Table 2. Table 3 shows the comparison between this work and several recent works. This work is the only one to provide all-PVT-corner detection and slew rate compensation. Meanwhile, our design is also the only one to meet the slew rate specifications of ATA given VDDIO=1.2/1.8/2.5 V. Besides, our design is the only one to meet the data rate specifications of PCI-express.

4. Conclusion

In this work, the 2×VDD output buffer with PVT detector for slew rate compensation is implemented using a typical 90 nm CMOS process. The maximum slew rare improvement can be achieved over 26%. The maximum slew rare is 1.65 (V/ns) when VDDIO=2.5 V. Notably, since the PVT sensor and PVT decider are implemented on silicon, it is easy to carry out real-time detection of the PVT corners of PMOS and NMOS, respectively.

Acknowledgments

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