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A low power 48-dB/stage linear-in-dB variable gain amplifier for direct-conversion receivers

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ABSTRACT

In this paper, a low power Variable Gain Amplifier (VGA) circuit with an approximation to exponential gain characteristic is presented. It is achieved using current mirrors to generate appropriate current signals to bias the input stage of the VGA circuit working in triode region, and the output stage working in saturation region, respectively. The VGA circuit presented herein comes with a 549 μW maximum power consumption given a 1.8 V supply. Most important of all, it has a linear-in-dB 48-dB dynamic gain range per stage. The effect of the input trasconductance and the output resistance on the linearity of gain control is also discussed. This circuit is fabricated using a 0.18 μm standard CMOS process with a core area of 0.0045 mm^2.

1. Introduction

A wireless sensor network (WSN) is a network comprising autonomous sensors which are spatially distributed to cooperatively monitor physical or environmental conditions, e.g., temperature, sound, vibration, pressure, movement or pollutants [1]. In WSN and other modern communication systems, the received signals often undergo a wide range of variable attenuation in different channels. To accurately retrieve information from these waveforms, an automatic gain control (AGC) circuit must be included in the receivers to adjust the amplitude such that downstream circuits can operate in the desired manner [2]. To realize constant settling time AGC circuits that are independent of the amplitude of the incoming waveforms, the variable gain amplifier (VGA) utilized to amplify the incoming waveforms is required to adjust its gain linearly in decibels with a gain control voltage [3].

Unfortunately, with the absence of devices providing an exponential characteristic with a standard CMOS process, it is much more difficult to design such a VGA than with a process offering bipolar transistors. To overcome this problem, pseudo-exponential functions that attempt to approximate the real exponential function have been reported [3–7], and circuits with a pseudo-exponential function behavior have also been proposed [4–7]. In this paper, a novel VGA with a gain pseudo-exponentially controlled by the gain controlling voltage is presented. With design consideration that transceivers for WSN have relatively low data rates and power consumption, this VGA requires a maximum power no more than 549 μW and occupies merely 47 μm × 96 μm on silicon.

2. VGA Circuit Design

2.1. Approximation of exponential gain characteristics

By using Taylor series expansion, the exponential function can be expanded as:

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \cdots + \frac{a^n}{n!}x^n \tag{1}$$

The terms in Eq. (1) with $n > 3$ has negligible influence to the function. Thus, the function can be approximated as follows [3],

$$e^{ax} \approx 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 = \frac{1}{2} \times \left[1 + (1+ax)^2\right] \tag{2}$$

Note that $ax \ll 1$works well in the above equation. Fortunately, the decibel linear range can be improved by changing the constant 1 into a decimal number 0.12 and using the relation, $e^{2ax} = e^{ax}/e^{-ax}$, which results in the following equations [4].

$$e^{ax} \approx 0.12 + (1+ax)^2 \tag{3}$$

$$e^{2ax} = \frac{e^{ax}}{e^{-ax}} \approx \frac{0.12 + (1+ax)^2}{0.12 + (1-ax)^2} \tag{4}$$

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Nevertheless, the constant 0.12 cannot be easily implemented accurately with analog circuits. By contrast, the decimal 0.125 can be realized by using a current mirror with a ratio of 1:8.

It can be shown in Fig. 1 that the approximation using a constant of 0.125 is as good as using 0.12. Hence, the constant 0.125 is adopted in Eq. (5) of this design instead of 0.12. Thus, Eq. (4) is turned into the following equation.

$$e^{2ax}=\frac{e^{ax}}{e^{-ax}}\approx\frac{0.125+(1+ax)^2}{0.125+(1-ax)^2} \tag{5}$$

To obtain a circuit capable of carrying out a relationship dictated by Eq. (5), a current generator is built consisting of M_{N1}, M_{N2}, M_{P1}, M_{P2}, and 4 sets of current mirrors, as shown in Fig. 2. The current paths of this circuit can be expressed with as follows.

$$I_{D,M_{N1}}=\frac{1}{8}\times\beta\times\left(\tfrac{1}{2}\times V_{DD}-V_{thn}\right)^2 \tag{7}$$

$$I_{D,M_{P1}}=\frac{1}{8}\times\beta\times\left(V_{DD}-\tfrac{1}{2}\times V_{DD}-|V_{thp}|\right)^2 \tag{8}$$

$$I_{D,M_{N2}}=\beta\times\left[\left(\tfrac{1}{2}\times V_{DD}+\Delta V_{control}\right)-V_{thn}\right]^2 \tag{9}$$

$$I_{D,M_{P2}}=\beta\times\left[V_{DD}-\left(\tfrac{1}{2}\times V_{DD}+\Delta V_{control}\right)-|V_{thp}|\right]^2 \tag{10}$$

where β is selected such that $k_nC_{ox}(W/L)_{N1}=k_pC_{ox}(W/L)_{P1}$. This relationship also dictates the aspect ratio of transistors M_{N1}, M_{N2}, M_{P1}, and M_{P2}. From KCL, I_{C1} and I_{C2} are the sum of drain currents from M_{P1}, M_{P2} and M_{N1}, M_{N2}, respectively. With some algebraic manipulation, we attain:

$$\begin{aligned}I_{C1}&=\left\{\tfrac{1}{8}\times\beta\times\left(V_{DD}-\tfrac{1}{2}\times V_{DD}-|V_{thp}|\right)^2+\beta\right.\\&\quad\left.\times\left[V_{DD}-\left(\tfrac{1}{2}\times V_{DD}+\Delta V_{control}\right)-|V_{thp}|\right]^2\right\}\times A_{I1}\\&=\beta\times\left(V_{DD}-\tfrac{1}{2}\times V_{DD}-|V_{thp}|\right)^2\\&\quad\times\left[\tfrac{1}{8}+\left(\frac{V_{DD}-\left(\tfrac{1}{2}\times V_{DD}+\Delta V_{control}\right)-|V_{thp}|}{V_{DD}-\tfrac{1}{2}\times V_{DD}-|V_{thp}|}\right)^2\right]\times A_{I1}\\&=\beta\times\left(\tfrac{1}{2}\times V_{DD}-|V_{thp}|\right)^2\times\left[\tfrac{1}{8}+\left(1-\frac{\Delta V_{control}}{\tfrac{1}{2}\times V_{DD}-|V_{thp}|}\right)^2\right]\times A_{I1}\end{aligned} \tag{11}$$

and

$$\begin{aligned}I_{C2}&=\left\{\tfrac{1}{8}\times\beta\times\left(\tfrac{1}{2}\times V_{DD}-V_{thn}\right)^2+\beta\times\left[\left(\tfrac{1}{2}\right.\right.\right.\\&\quad\left.\left.\left.\times V_{DD}+\Delta V_{control}\right)-V_{thn}\right]^2\right\}\times A_{I2}\\&=\beta\times\left(\tfrac{1}{2}\times V_{DD}-V_{thn}\right)^2\\&\quad\times\left[\tfrac{1}{8}+\left(\frac{\left(\tfrac{1}{2}\times V_{DD}+\Delta V_{control}\right)-V_{thn}}{\tfrac{1}{2}\times V_{DD}-V_{thn}}\right)^2\right]\times A_{I2}\\&=\beta\times\left(\tfrac{1}{2}\times V_{DD}-V_{thn}\right)^2\times\left[\tfrac{1}{8}+\left(1+\frac{\Delta V_{control}}{\tfrac{1}{2}\times V_{DD}-V_{thn}}\right)^2\right]\times A_{I2}\end{aligned} \tag{12}$$

where A_{I1} and A_{I2} are the current gains of the respective current mirrors. Then, bydividing I_{C2} with I_{C1}, we attain:

$$\begin{aligned}\frac{I_{C2}}{I_{C1}}&=\frac{\beta\times\left(\tfrac{1}{2}\times V_{DD}-V_{thn}\right)^2\times A_{I2}}{\beta\times\left(\tfrac{1}{2}\times V_{DD}-|V_{thp}|\right)^2\times A_{I1}}\times\frac{\left[\tfrac{1}{8}+\left(1+\frac{\Delta V_{control}}{\tfrac{1}{2}\times V_{DD}-V_{thn}}\right)^2\right]}{\left[\tfrac{1}{8}+\left(1-\frac{\Delta V_{control}}{\tfrac{1}{2}\times V_{DD}-|V_{thp}|}\right)^2\right]}\\&=\frac{\left(\tfrac{1}{2}\times V_{DD}-V_{thn}\right)^2\times A_{I2}}{\left(\tfrac{1}{2}\times V_{DD}-|V_{thp}|\right)^2\times A_{I1}}\times\frac{\left[0.125+\left(1+\frac{\Delta V_{control}}{\tfrac{1}{2}\times V_{DD}-V_{thn}}\right)^2\right]}{\left[0.125+\left(1-\frac{\Delta V_{control}}{\tfrac{1}{2}\times V_{DD}-|V_{thp}|}\right)^2\right]}\end{aligned} \tag{13}$$

By approximating

$$a=\tfrac{1}{2}\times V_{DD}-V_{thn}\approx\tfrac{1}{2}\times V_{DD}-|V_{thp}| \tag{14}$$

Eq. (16) can be further simplified into:

$$\frac{I_{C2}}{I_{C1}}=\kappa\times\left[\frac{0.125+(1+ax)^2}{0.125+(1-ax)^2}\right]\approx\kappa\times e^{ax} \tag{15}$$

where

$$x=\Delta V_{control} \tag{16}$$

and

$$\kappa=\frac{\left(\tfrac{1}{2}\times V_{DD}-V_{thn}\right)^2\times A_{I2}}{\left(\tfrac{1}{2}\times V_{DD}-|V_{thp}|\right)^2\times A_{I1}} \tag{17}$$

Apparently, if the gain of an amplifier is a linear function of Eq. (13), the particular amplifier will provide pseudo-exponential gain characteristics and linear-in-dB characteristics.

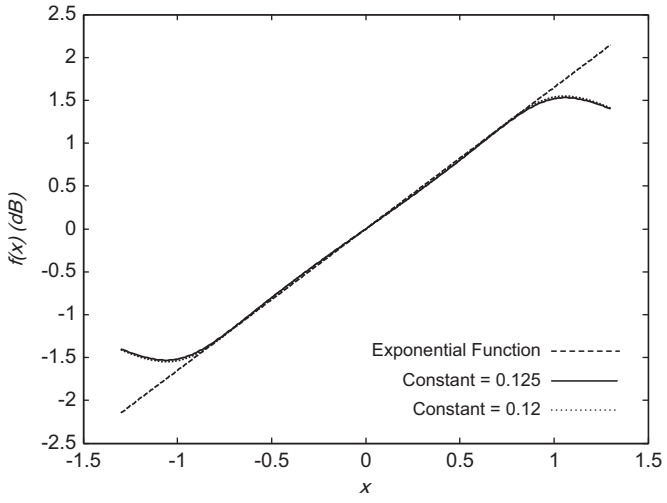

Fig. 1. Approximation of the exponential function.

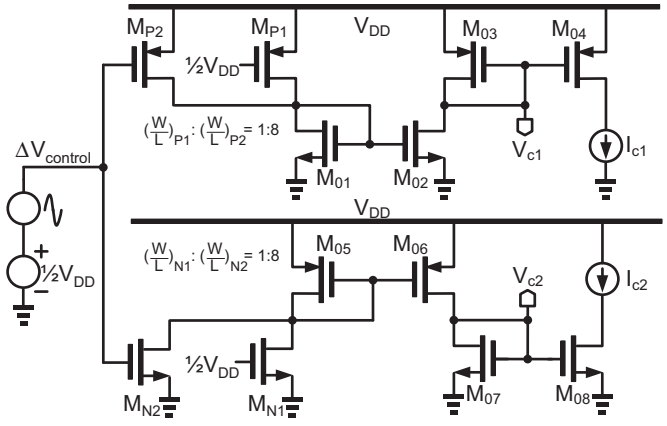

Fig. 2. I_{C1} and I_{C2} current generator.

2.2. VGA circuit with exponential gain characteristics

To realize an amplifier with the required pseudo-exponential gain characteristics, a system topology shown in Fig. 3 is used. A current generator is used as a V-to-I circuit, which converts the

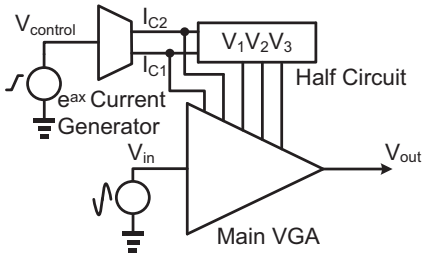

Fig. 3. The block diagram of the proposed VGA.

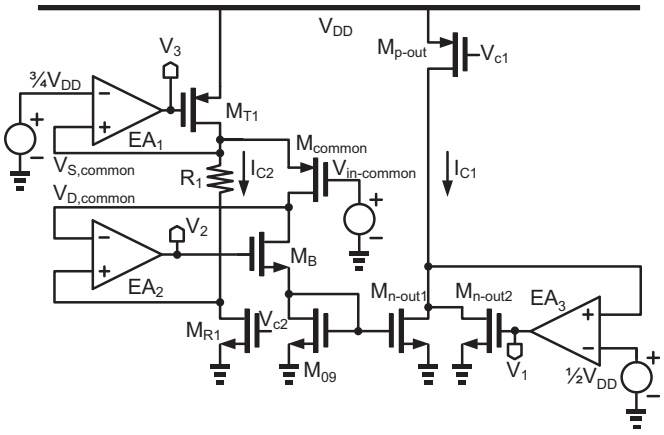

Fig. 4. The half circuit.

control voltage $V_{control}$ into I_{C1} and I_{C2}, as shown in Fig. 2. The current I_{C1} and I_{C2} will be mirrored to both main VGA and half circuit. The half circuit is in charge of generating additional bias voltages, V_1, V_2, and V_3, which are supplied to main VGA as functions of I_{C1} and I_{C2}. With the appropriate bias currents and bias voltages from the current generator and the half circuit, the main VGA amplifies the incoming voltage, V_{in}, by an amplitude according to the control voltage $V_{control}$. Notably, V_{in} and V_{out} are fully differential in physical implementation.

As shown in the half circuit Fig. 4, I_{C2} is mirrored to M_{R1} through V_{C2}, which flows through R_1 to generate a voltage $I_{C2} \times R_1$. Recall that the transconductance of a MOS transistor operating in triode region is expressed as follows.

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \frac{\partial\left\{\mu_p C_{ox}\left(\frac{W}{L}\right)\left[(V_{gs}-V_{th})V_{ds}-\frac{1}{2}{V_{ds}}^2\right]\right\}}{\partial V_{gs}} = \mu_p C_{ox}\left(\frac{W}{L}\right)V_{ds} \tag{18}$$

If we bias M_{common} in triode region and ensure that the voltage across the transistor is equivalent to the voltage across R_1, the transconductance of M_{common} becomes:

$$g_m = \mu_p C_{ox}\left(\frac{W}{L}\right)I_{C2}R_1 \tag{19}$$

To ensure that the drain node voltage of M_{T1} remains constant regardless of I_{C2}, an error amplifier EA_1 is used to regulate the drain of M_{T1} to V_{bias} by adjusting the gate of M_{T1} with V_3. EA_2 senses the drain node of M_{R1} and regulate the drain of M_{common} to be consistent by adjusting the gate of M_B with V_2. In this way, both the source and drain node voltages of transistor M_{common} are well-defined:

$$V_{S,common} = V_{bias} \tag{20}$$

$$V_{D,common} = V_{bias} - I_{C2}R_1 \tag{21}$$

Both V_2 and V_3 are used to bias the main VGA, forcing both the input transistors M_{in1} and M_{in2} into triode region such that their transconductance will be governed by Eq. (19).

The output resistance of an amplifier is determined by:

$$r_o = \frac{1}{\lambda I_D} = (\lambda_p I_{D,M_{p\text{-}out}} + \lambda_n I_{D,M_{n\text{-}out1}} + \lambda_n I_{D,M_{n\text{-}out2}})^{-1} \tag{22}$$

which is denoted as the shunted output resistance of $M_{p\text{-}out}$, $M_{n\text{-}out1}$ and $M_{n\text{-}out2}$. Since $I_{D,M_{p\text{-}out}} = I_{D,M_{n\text{-}out1}} + I_{D,M_{n\text{-}out2}}$ and let $I_{D,M_{p\text{-}out}} = I_{C1}$, we have:

$$r_o = \frac{1}{\lambda_p I_{C1} + \lambda_n I_{C1}} = \frac{1}{(\lambda_p + \lambda_n)I_{C1}} \tag{23}$$

By multiplying Eq. (19) with Eq. (23), we attain an expression of the overall gain:

$$A_{vVGA} = \frac{A_{I3}\mu_p C_{ox}\left(\frac{W}{L}\right)I_{C2}2R_2}{(\lambda_p + \lambda_n)I_{C1}}$$

$$= \frac{A_{I3}\mu_p C_{ox}\left(\frac{W}{L}\right)2R_2}{(\lambda_p + \lambda_n)} \times \kappa \times \left[\frac{0.125+(1+ax)^2}{0.125+(1\text{-}ax)^2}\right] \approx B \times e^{ax} \tag{24}$$

where A_{I3} is the current gain of the drain current of $M_{n\text{-}out2+}$ or $M_{n\text{-}out2-}$ compared to the drain current of M_{B1} or M_{B2} of Fig. 5.

By Eq. (24), we obtain a VGA circuit shown in Fig. 5 that provides a gain linearly in decibels with respect to gain controlling voltage, which is realized using transconductors given the MOS operating in triode region and output resistance given the MOS operating in saturation region.

Current balancing is achieved using EA_3, $M_{n\text{-}out1+}$, $M_{n\text{-}out2-}$, and $M_{n\text{-}out2}$. Referring to Fig. 4, EA_3 can be interpreted as a linear regulator, which attempts to regulate the drain nodes of $M_{p\text{-}out}$ in Fig. 4, $M_{n\text{-}out1}$ and $M_{n\text{-}out2}$ in Fig. 5 to a predefined voltage, $V_{out,common}$. As EA_3 controls the gate voltage of $M_{n\text{-}out2}$, $M_{n\text{-}out1+}$ and $M_{n\text{-}out2-}$ are simultaneously controlled as well. Hence, the DC level of the output nodes of both main VGA and the half circuit will be kept at $V_{out,common}$ regardless of the gain control voltage, $V_{control}$. In this design, $V_{out,common}$ is chosen to be $\frac{1}{2}V_{DD}$. This is important because we need to ensure $M_{p\text{-}out}$, $M_{n\text{-}out1}$, $M_{n\text{-}out2}$, $M_{p\text{-}out+}$, $M_{n\text{-}out1+}$, $M_{n\text{-}out2+}$, $M_{p\text{-}out-}$, $M_{n\text{-}out1-}$, and $M_{n\text{-}out2-}$, all working in saturation such that the VGA operates in a manner dictated by Eq. (24). Furthermore, it is important for the outputs of the VGA to $1/2V_{DD}$ to attain the maximum voltage swing. However, if the input stage of the cascaded circuit requires a DC bias other than $1/2V_{DD}$, $V_{out,common}$ can be adjusted to a demanded corresponding value.

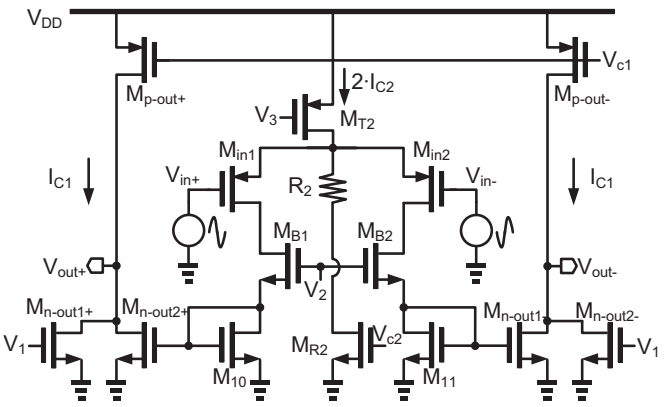

Fig. 5. The main VGA.

3. Measurement results of the VGA

This design has been implemented using TSMC 0.18 μm standard CMOS process. Simulation results show that the VGA has a minimum bandwidth of 3 MHz with no RC load, and 5 kHz with 50 pF loading on both outputs. The measurement was conducted with PC-controlled Audio Precision Sys-2712, which has approximately 50 pF capacitive load on both probes. ABM

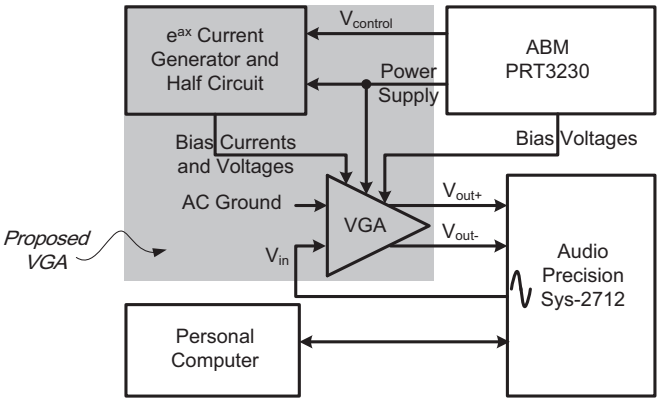

Fig. 6. The measurement setup for the proposed VGA.

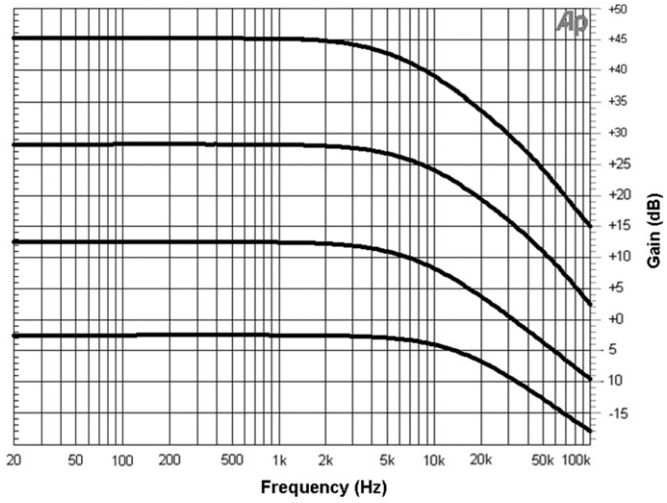

Fig. 7. The measured Bode plot.

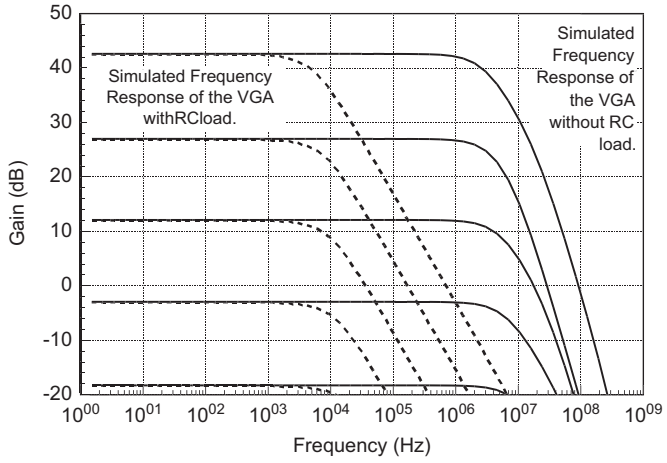

Fig. 8. The simulated Bode plot.

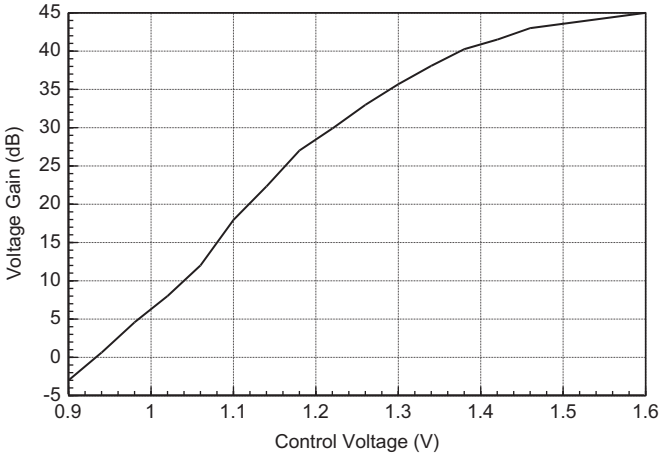

Fig. 9. Measured gain with respect to $V_{control}$.

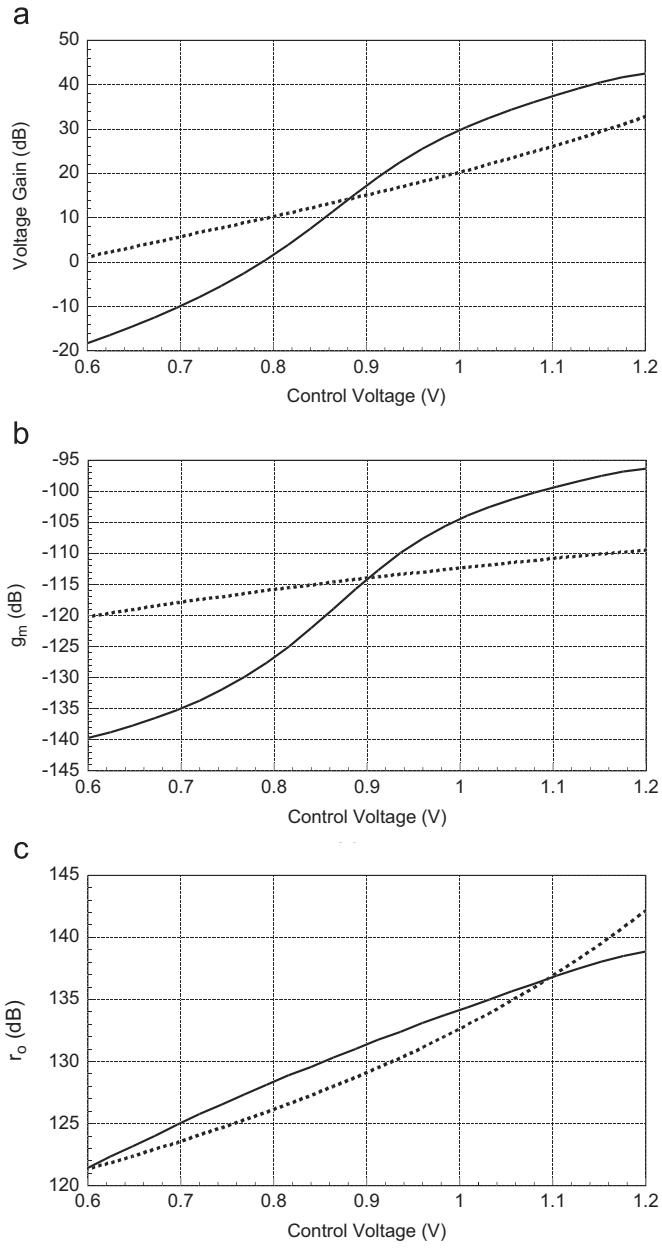

Fig. 10. Simulated (solid line) vs, theoretical (dotted line) on (a) gain, (b) g_m, (c) r_o with respect to $V_{control}$.

PRT3230 was used to supply power, provide bias voltages, and generate the gain control voltage. The measurement setup is shown in Fig. 6, and the measured and simulated Bode plots are given in Fig. 7 and Fig. 8, respectively.

Measurement results plotted in Fig. 9 also show that current I_{C1} and I_{C2} are capable of adjusting the forward gain from −3 dB to 45 dB, which is 12 dB narrower than the simulated result of −18 dB to 42 dB shown in Fig. 10(a). Nevertheless, the gain tuning range of two such cascaded VGAs is still more than enough for most wireless receivers [2].

To address the nonlinearity characteristic exhibited in the measurement and simulation results, we have to separate the transconductance, g_m, and output resistance, r_o, and plot their values as shown in Figs. 10(b) and 10(c), respectively, against the gain control voltage, $V_{control}$. Apparently, r_o closely follows Eq. (23), and the gain linearly in decibels with the gain control voltage is achieved. However, the tunable range of r_o should not be large to prevent an excessive difference in the bandwidth of VGA with respect to different gain. On the other hand, g_m has a large tuning range, yet showing nonlinear characteristics against $V_{control}$, which deviates from Eq. (18). The major reason of this problem lies in the usage of square-law modeling of MOS transistors. Since Eq. (18) is attained by differentiating the square-law drain current equation of a MOS transistor working in triode region, linearity is limited to very small range where the square-law model is accurate. The same phenomenon also applies to MOS transistors working in saturation, which has been reported in prior works [4,7]. VGAs demonstrated in these literatures use MOS transistors working in saturation as the input transconductor and diode-connected loads as active loads such

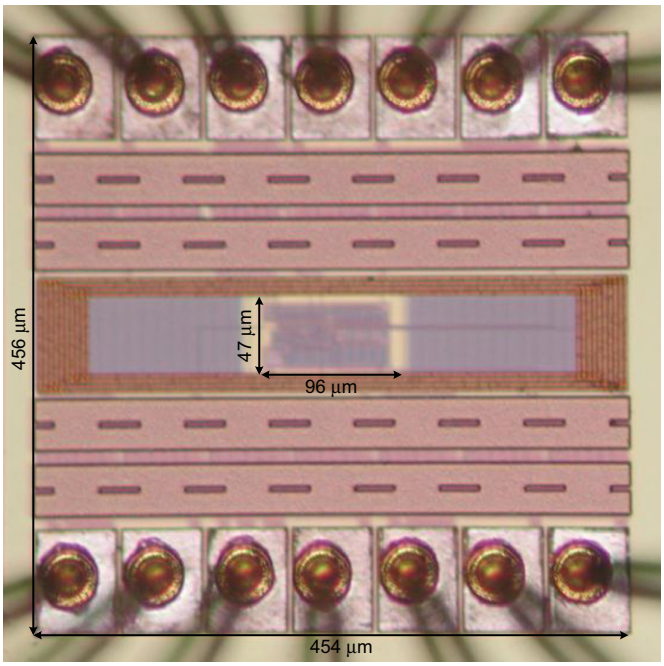

Fig. 11. Die micrograph.

Table 2
Overall performance.

Gain: −3 dB to 45 dB	Input voltage swing: 0.1 V
Bandwidth: 3 MHz Min.	Output voltage swing: 1 V
THD: −42 dB	CMRR: 10 dB to 13 dB
Core area: 0.0045 mm^2	PSRR: −60 dB to −46 dB
Supply voltage: 1.8 V	Slew rate: 0.2 V/ns
Power: 0.433 mW to 0.549 mW	Noise: $2.5\mu V\sqrt{Hz}$

Table 1
Transistor sizes.

I_{C1} and I_{C2} current generator						
M_{P1}		M_{P2}		M_1/M_2		M_3/M_4
$\frac{0.88\ \mu m}{1.8\ \mu m}$		$\frac{7.04\ \mu m}{1.8\ \mu m}$		$\frac{0.22\ \mu m}{1.8\ \mu m}$		$\frac{0.22\ \mu m}{1.8\ \mu m}$
M_{N1}		M_{N2}		M_5/M_6		M_7/M_8
$\frac{0.88\ \mu m}{1.8\ \mu m}$		$\frac{1.76\ \mu m}{1.8\ \mu m}$		$\frac{0.88\ \mu m}{1.8\ \mu m}$		$\frac{0.22\ \mu m}{1.8\ \mu m}$
The half circuit						
M_{T1}		$M_{p\text{-}out}$		M_{common}		M_B
$\frac{22\ \mu m}{1.8\ \mu m}$		$\frac{6.6\ \mu m}{1.8\ \mu m}$		$\frac{6.6\ \mu m}{1.8\ \mu m}$		$\frac{8.8\ \mu m}{1.8\ \mu m}$
M_{R1}		M_{09}		$M_{n\text{-}out1}$		$M_{n\text{-}out2}$
$\frac{5.28\ \mu m}{1.8\ \mu m}$		$\frac{3.3\ \mu m}{1.8\ \mu m}$		$\frac{2.42\ \mu m}{1.8\ \mu m}$		$\frac{0.88\ \mu m}{1.8\ \mu m}$
The main VGA						
$M_{p\text{-}out+}$	$M_{p\text{-}out-}$	M_{T2}	M_{in1}	M_{in2}	M_{B1}	M_{B2}
$\frac{6.6\ \mu m}{1.8\ \mu m}$	$\frac{6.6\ \mu m}{1.8\ \mu m}$	$\frac{44\ \mu m}{1.8\ \mu m}$	$\frac{6.6\ \mu m}{1.8\ \mu m}$	$\frac{6.6\ \mu m}{1.8\ \mu m}$	$\frac{8.8\ \mu m}{1.8\ \mu m}$	$\frac{8.8\ \mu m}{1.8\ \mu m}$
M_{10}	M_{11}	$M_{n\text{-}out1+}$	$M_{n\text{-}out1-}$	$M_{n\text{-}out2+}$	$M_{n\text{-}out2-}$	M_{R2}
$\frac{3.3\ \mu m}{1.8\ \mu m}$	$\frac{3.3\ \mu m}{1.8\ \mu m}$	$\frac{0.88\ \mu m}{1.8\ \mu m}$	$\frac{2.42\ \mu m}{1.8\ \mu m}$	$\frac{2.42\ \mu m}{1.8\ \mu m}$	$\frac{0.88\ \mu m}{1.8\ \mu m}$	$\frac{10.56\ \mu m}{1.8\ \mu m}$

Table 3
Comparison with prior works.

	Proposed	[4]	[6]	[7]	[8]
Gain (dB)	−3 to 45	0 to 95	−10 to 17	−5 to 10	5 to 53
Stages	1	3[a]	2	1	2
Bandwidth	3 MHz Min.	32 MHz	1.25 GHz	150 MHz	15 MHz
Supply voltage	1.8 V	1.8 V	1.8 V	3.3 V	3 V
Power (mW)	0.433–0.549	6.48	43.2	2.5	2.8
Process (μm)	0.18	0.18	0.18	0.5	1.2
Core area	0.0045 mm^2	0.4 mm^2	0.0887 mm^2	0.15 mm^2	N/A
Year	2010	2006	2008	1998	2000
FOM	58287.8	1172.84	8807.779	6000	257.14/Area

[a] Variable gain stage+1 constant gain stage.

that their gain can be described as follows,

$$A_{v,\mathrm{VGA}} = \frac{g_{m,\mathrm{transconductor}}}{g_{m,\mathrm{diode\text{-}load}}} \alpha \sqrt{\frac{I_{\mathrm{transconductor}}}{I_{\mathrm{diode\text{-}load}}}} \quad (25)$$

where $g_{\mathrm{m,transconductor}}$ and $g_{\mathrm{m,diode\text{-}load}}$ represents the input transconductor and the diode-connected load, $I_{\mathrm{transconductor}}$ and $I_{\mathrm{diode\text{-}load}}$ represents their bias currents, respectively. Apparently, the gain of such VGAs exhibits a square-root relationship with their gain control current, $I_{\mathrm{transconductor}}$ and $I_{\mathrm{diode\text{-}load}}$, whereas the VGA described in this work is directly proportional to its gain control current, I_{C1} and I_{C2}. In other words, the difference in bias current flowing through the proposed VGA can be made half for the same gain tuning range in comparison with the prior works. Hence, the variation in the bandwidth of the VGA is also reduced. By contrast, the tunable gain range is doubled for the same change in gain control current. If gain linearity is stringent, certain circuits can be added to the current mirror shown in Fig. 2 to prevent the system from adjusting the VGA into regions where Eq. (14) is no longer valid, and still retain an acceptable gain tuning range. Comparing Fig. 9 with Fig. 10(a), it is apparent that the gain tuning range measured is deviated from the simulation. When V_{control} is lower than 0.9 V, the currents flowing through $M_{\mathrm{p\text{-}out}}$, $M_{\mathrm{p\text{-}out+}}$, and $M_{\mathrm{p\text{-}out-}}$ become larger than what is anticipated by simulations. The widths of $M_{\mathrm{n\text{-}out2}}$, $M_{\mathrm{p\text{-}out-}}$, and $M_{\mathrm{p\text{-}out2-}}$ are not sufficiently large to handle such a current. Hence, EA_3 can no longer regulate the DC level of the VGA output to $V_{\mathrm{out\text{-}common}}$ to make the VGA function properly (Table 1).

The proposed VGAs have a simulated power consumption ranging from 433 μW to 549 μW depending on its gain. Limited by the current resolution given by ABM PRT3230, we can only verify that the current consumed by three of these identical VGAs is less than 1 mA, and that of other seven identical VGAs is less than 2 mA, all at maximum gain, respectively. This implies that the overall power consumption is below 0.514 mW at the maximum gain. Seven of these VGAs consume more than 2 mA, and three of these VGAs consume less than 1 mA, indicating a single VGA consumes power around the range of 0.5 mW to 0.6 mW at the minimum gain. The micrograph of this VGA is shown in Fig. 11.

Dimensions of the transistors used in this VGA are given in Table 1, whereas a tabulated comparison of this VGA along with other prior works is shown in Table 2. Besides the advantages in terms of power dissipation and area, the proposed VGA also out performs other prior works in the following figure of merit (FOM) comparison Table 3:

$$\mathrm{FOM} = \frac{\text{tunable gain} \times \text{bandwidth}}{\text{power consumption} \times \text{area}} (\mathrm{dB\ MHz\ mW^{-1}\ mm^{-2}}) \quad (26)$$

4. Conclusion

In this study, a VGA with linear-in-dB gain characteristics is presented. The approximation to the exponential gain characteristic is derived, and a feasible realization is proposed. The power consumption of this VGA is below 0.549 mW, with a dynamic range of 48 dB per stage. Hence, dynamic range specifications of a wireless sensor network are easily met, making this VGA practical in many applications.

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