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A high-efficiency DC–DC buck converter for sub-2 × VDD power supply

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ABSTRACT

This paper presents a DC–DC step-down converter, which can accommodate the range of power supply voltage from VDD to sub-2 × VDD. By utilizing stacked power MOSFETs, a voltage level converter, a detector and a controller, the proposed design is realized by a typical 1P6M 0.18 μm CMOS process without using any high voltage process to resolve gate-oxide reliability and leakage current problems. The core area of the proposed design is less than 0.184 mm^2, while the power supply range is up to 5 V. Since the internal reference voltage is 1.0 V, it can increase the output regulation range. The proposed design attains very high conversion efficiency to prolong the life time of battery-based power supply. Therefore, it can be integrated in a SOC (system-on-chip) to provide multiple supply voltage sources.

1. Introduction

Thanks to the fast evolution of semiconductor technology, transistors are downsized constantly and rapidly. The operation voltage of transistors is also dropped from 5 V to 3.3, 1.8 V, or even less. Nevertheless, the operation voltage of prior or existing systems might be still 12 or 5 V, particulary car electronics. Therefore, we need a voltage converter to supply lower operation voltage for transistors fabricated by advanced processes. The function of a voltage converter is to convert an input voltage into a regulable output voltage. Moreover, the output voltage should be independent with the variation of input voltage and output load. Nowadays, there are two popular types of voltage converters, the "Low Drop-Out Linear Regulator (LDO)" and the "Switching Mode Power Supply (SMPS)" [1]. Table 1 shows the comparison between these two types of voltage converters.

Fig. 1 shows a typical structure of the low drop-out linear regulator [2]. Its major advantages include a small resolution step, if properly implemented, and low cost. However, if heat sinks are required, the cost will be increased. Additionally, LDOs do not generate any switching noise. The simplicity is another advantage for LDOs. On the other hand, one of the main disadvantages of LDOs is poor efficiency, since the power, which is not delivered to the load, will be dissipated as heat in the pass element. Therefore, engineers usually choose this structure as a power system solution when the output voltage is very close to the input voltage.

The switching mode power supply (SMPS) is usually applied to high efficiency voltage converters instead of linear regulators, especially when the voltage difference between the input and the output of the voltage converter is large [3,4]. In addition to the previous advantage, the output voltage of the SMPS can be boosted, dropped, or even converted into a negative voltage. Therefore, its application scope is larger than that of the linear regulators. However, the disadvantage of the switching mode power supply is that ripples will be coupled with the output voltage. The reason is that the switching mode power supply compares the divided voltage of the output with an internal reference voltage to generate digital control signals which then turn-on/off the power MOS transistors. There are two common methods to implement the controller mechanism therein, "Pulse-Width Modulator (PWM)" and "Pulse-Frequency Modulator (PFM)" [5]. A general structure of the buck converter circuit is illustrated in Fig. 2.

In this paper, we propose a high-efficiency DC–DC buck converter for sub-2 × VDD power supply by using stacked output stage. In Section 1, the comparison between LDO and DC–DC buck converter is introduced. Besides, the overview of the entire work is briefed. In Section 2, we analyze basic DC–DC buck converter to show the efficiency and regulation indexes. In Section 3, the proposed DC–DC buck converter is disclosed. The analysis of the proposed design is described in great detail. In Section 4, the simulation and measurement result are shown to justify the correctness of our design. Finally, we compare the measurement results with those of prior works. A short conclusion is given in Section 5.

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Table 1
Comparison between LDO and SMPS.

	LDO	SMPS
Efficiency	Low (30%–50%)	High (> 70%)
Structure	Simple	Complex
Output ripple	Small	Big
Weight & Volume	Big	Small
Input range	Small	Big

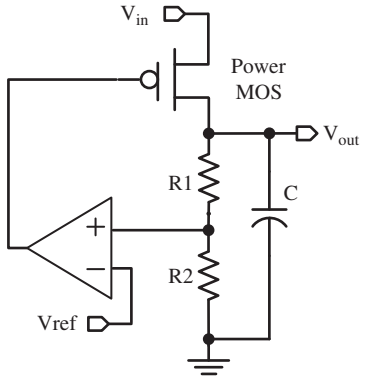

Fig. 1. Typical structure of a low drop-out linear regulator.

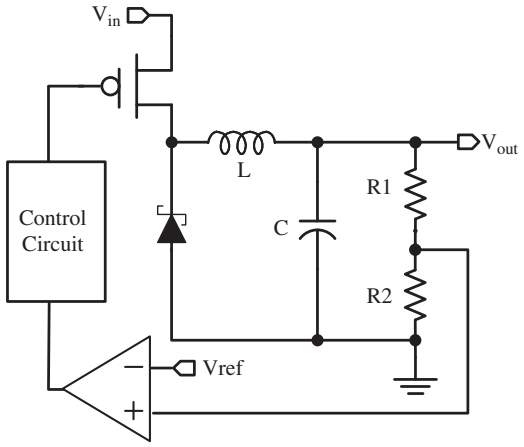

Fig. 2. General structure of the buck converter circuit.

2. Performance indexes of DC–DC buck converter

2.1. Definition of performance indexes

As an ideal DC–DC converter, high-efficiency, good load regulation and line regulation are required. Efficiency, as shown in Eq. (1), is the ratio of output power and input power. The difference between input power and output power is the power consumption of internal control circuits and power MOSs. Therefore, when the DC–DC converter is overloaded given a large output current, the efficiency is relatively high. On the contrary, in the light load scenario, the proportion of the internal current consumption becomes large such that the efficiency will become low. Line regulation is expressed as ratio of variation in the output voltage relative to that in the input voltage, while the load regulation is expressed as variation in the steady state output voltage when the load current changes. Eqs. (2) and (3) show the definition for line regulation and load regulation, respectively.

$$\text{Efficiency} = \frac{P_{out}}{P_{loss}+P_{out}} \times 100\% \tag{1}$$

$$\text{Line regulation} = \frac{\Delta V_{\text{out}}/V_{\text{out}}}{\Delta V_{\text{in}}} \times 100\% \tag{2}$$

$$\text{Load regulation} = \frac{V_{\text{out}}/V_{\text{out}}}{\Delta I_{out}} \times 100\% \tag{3}$$

2.2. Efficiency analysis

Assume the power loss of those discrete components besides transistors is negligible. Eq. (4) is attained by dividing the numerator and denominator with the same output current. Referring to Eq. (4), when the resistance is equal to the load resistance, the efficiency is close to 50%. If the efficiency is expected to be greater than 90%, the turn-on resistance (R_{on}) must be at least one-tenth of the load resistance (R_{load}). Thus, to get a better efficiency, the first thing to carry out is to reduce the turn-on resistance. Besides, in the light load scenario, we need to consider the power consumption caused by dynamic switching and the static current. The dynamic power consumption of CMOS logic is proportional to the number of transitions, i.e., $P \propto C \cdot V^2 \cdot f$, where C is the load, V denotes the voltage swing, and f is the frequency of switches. Therefore, reducing operation frequency by the control circuit will provide a better efficiency in the light load scenario. Prior methods for such a design purpose include the PFM control circuit [6], Pulse Skip [7], and Burst Mode [8]. However, though all the above methods were proved to reduce the frequency of switching and the static current, large ripples were also generated on the output voltage.

$$\text{Efficiency} = \frac{R_{load}}{R_{load}+R_{on}} = \frac{1}{1+R_{on}/R_{load}} \tag{4}$$

3. The high-efficiency DC–DC buck converter design

Fig. 3 shows the proposed buck converter, where a Pulse-Width Modulator is used to realize the feedback control. This structure includes a low drop-out linear regulator (LDO) as a voltage source to supply a 3.3 V, VDD33, for the internal circuity. A reference voltage, VREF = 1.0 V, generated by Bandgap, is compared with a feedback voltage which is the output voltage, Vout, divided by R1 and R2. EA (error amplifier) is used to amplify the difference between VREF and $R1/(R1+R2) \cdot Vout$. The output of EA, VEA, is compared with Vramp to generate a digital signal, Q. Dead-time circuit generates two non-overlapping signals, QP and QN. Voltage Level Converter [19] shifts the voltage level of QP and sends a VC to be the gate drive of the power transistor (PMOS1).

3.1. Gate-oxide reliability

Since the largest voltage input is 5 V, which is much higher than the usual core supply voltage, 3.3 V, in a typical 0.18 μm CMOS process. Therefore, we should resolve the gate-oxide reliability and leakage current problems. In this work, we propose two stacked MOSs in the output stage as shown in Fig. 4. To cut off the PMOS1 completely and prevent any leakage current, the gate drive of PMOS1 should be boosted by 1.7 V. Therefore, a Voltage Level Converter is needed, which is shown in Fig. 5. QP and QP_Bar are a pair of out-of-phase differential voltages. When QP is "1", MN03 is turned on and the voltage of VC_Bar is dropped. Therefore, VC is boosted as MP02 is turned on and MP01 is cut off. A positive feedback loop composed of MP01 and MP02 can enhance the voltage transition speed. Finally, Vin = 5 V is passed through VC, while the output voltage at VC_Bar becomes

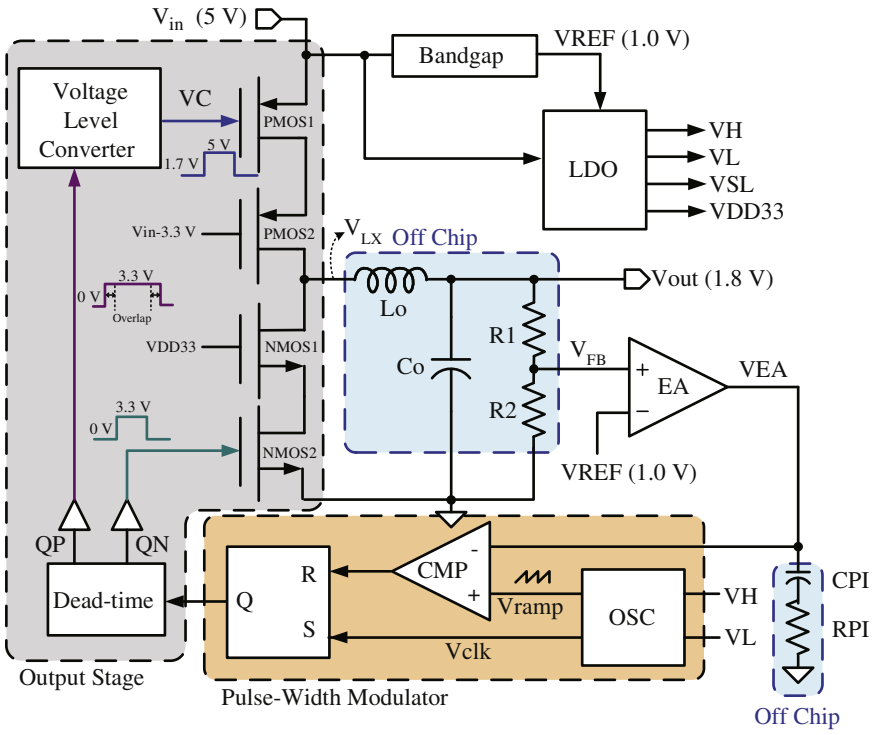

Fig. 3. The proposed DC–DC buck converter structure.

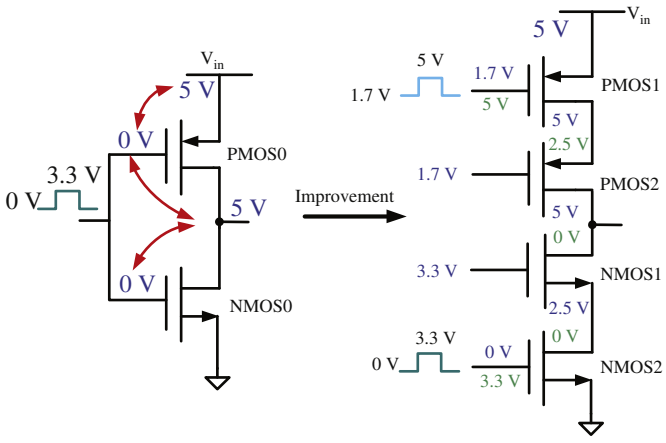

Fig. 4. Stacked output stage.

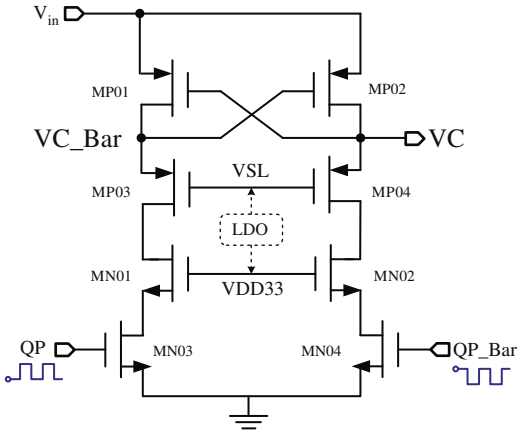

Fig. 5. Schematic of Voltage Level Converter.

the summation of VSL and the threshold voltage of MP03, which is close to VSL.

3.2. Pulse-width modulator

The Pulse-Width Modulator compares the voltage VEA and a triangular voltage, Vramp. It generates a pulse train of which the duty cycle is determined by the difference between VEA and Vramp. The Pulse-Width Modulator is composed of a voltage comparator, a clock and ramp signal generator, and a latch, as shown in Fig. 3.

The voltage comparator circuit, i.e., CMP in Fig. 3, mainly consists of three blocks: Pre-amplification, Decision circuit, and Output buffer as shown in Fig. 6 [9]. A differential pair and active loads are used to achieve the Pre-amplification function. The Decision circuit needs to distinguish the difference in a few mV level between the input voltages to have a high precision. We use a positive feedback network to increase the gain of the Decision circuit. The output buffer stage is used to slice the output signal of the Decision circuit into digital signals.

The schematic of clock and ramp signal generator is shown in Fig. 7. VH and VL are two reference voltages, and VH is always larger than VL. When Vclk is "0", then MN7 is cut off such that I1 and Icg are identical. In the meantime, Ct is charged by Icg, and Vramp is rising. As soon as Vramp is larger than VH, CMP_H turns "0" and CMP_L turns "1". Meanwhile, Vclk turns high and MN7 is turned on. After MN7 is turned on, Vramp is discharged through MN7 until Vramp is smaller than VL. By repeating the above operation, we can get a clock signal at Vclk and a ramp signal at Vramp.

The peak-to-peak value of Vramp is determined by VH and VL as illustrated in Fig. 8. A buck converter operated in the continuous-conduction mode (CCM) has the conversion relationship given by Eq. (5) [10], where VH and VL are upper and lower bounds of the ramp signal, D_{ramp} is the duty cycle pulse ratio of

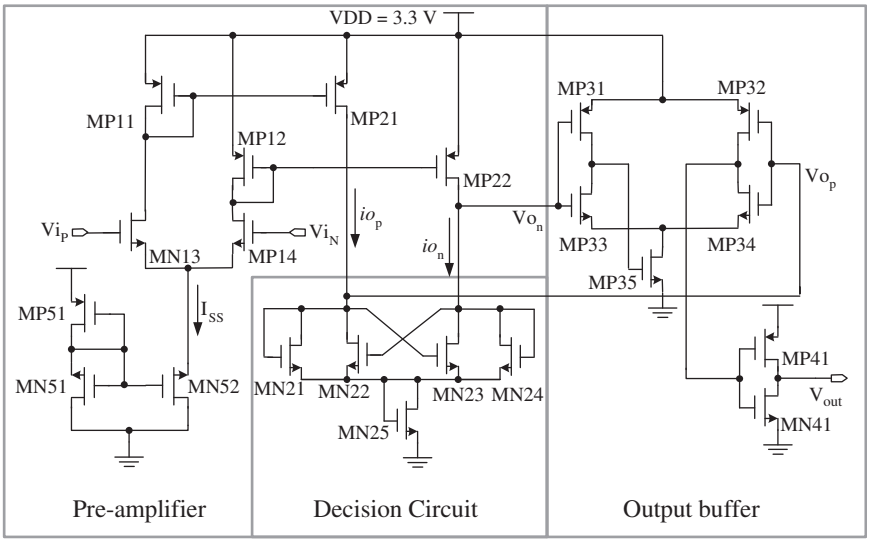

Fig. 6. The schematic of the voltage comparator (CMP).

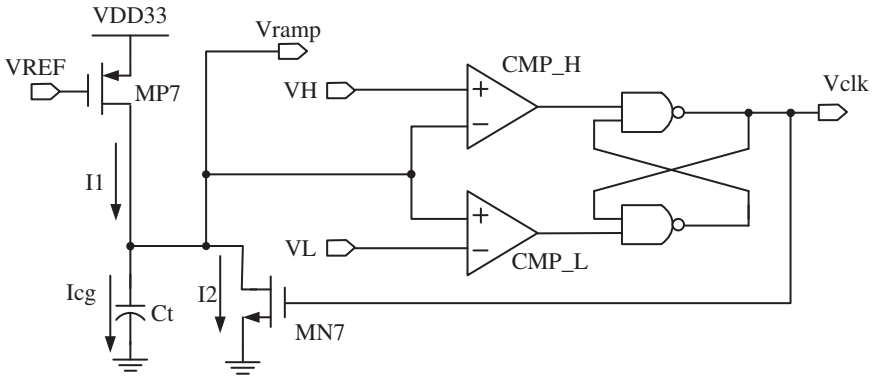

Fig. 7. The schematic of the clock and ramp signal generator.

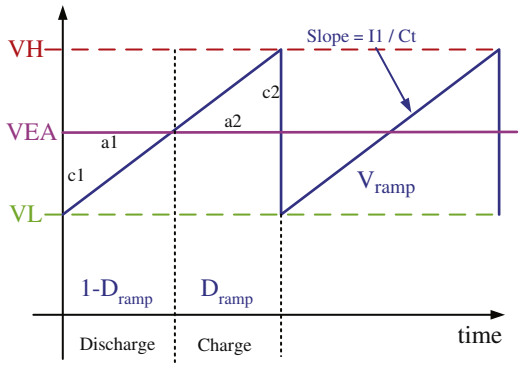

Fig. 8. Triangle voltage waveform of Vramp.

signal Q in Fig. 3. The transition frequency of the ramp signal, f_{ramp}, is calculated by Eq. (6).

$$D_{\text{ramp}} = \frac{\text{VH}-\text{VEA}}{\text{VH}-\text{VL}} = \frac{\text{Vout}}{\text{Vin}} \tag{5}$$

$$f_{ramp} \cong \frac{\text{I1}}{(\text{VH}-\text{VL})\cdot \text{Ct}} \tag{6}$$

Dead-time circuit in Fig. 3 generates a pair of non-overlapping control signals which can prevent any short-circuit current to improve the efficiency. Fig. 9 shows the schematic of Dead-time circuit design. When the input signal Q is "1", Q_Bar is "0". In the meantime, XOR_N equals to QP_Bar or the previous state, logic "0". Then, XOR_P is flipped to "1", because QN is "1", and QP_Bar is changed to "1" by the C2 delay path. Therefore, QP leads QN given a rising edge of input signal Q. By contrast, QN leads QP given a falling edge of input signal Q. Consequently, QN and QP become a pair of non-overlapping control signals for the power transistors.

3.3. Reference voltage

Reference voltage circuitry is critical to any analog circuit design, especially in the voltage converter design. Fig. 10 shows the schematic of Bandgap and LDO design in Fig. 3. Left side of Fig. 10 is a bandgap bias circuit [11]. It generates a PVT-independent (note: PVT=process, supply voltage, temperature) reference voltage, VREF. In this work, the reference voltage, VREF, is 1.0 V, which is also a reference voltage to the LDO circuit. The LDO circuit generates all of the required biases and a 3.3 V supply voltage for the internal circuits. The series resistors, RO0 and RO1, monitor the output voltage by a simple voltage division. A feedback voltage, Vf, is fed back and compared with VREF of Bandgap circuit by an error amplifier. The error amplifier then generates a control gate drive to the pass transistor, MPL11, to regulate the output voltage according to the difference between feedback voltage, Vf, and output voltage of Bandgap circuit.

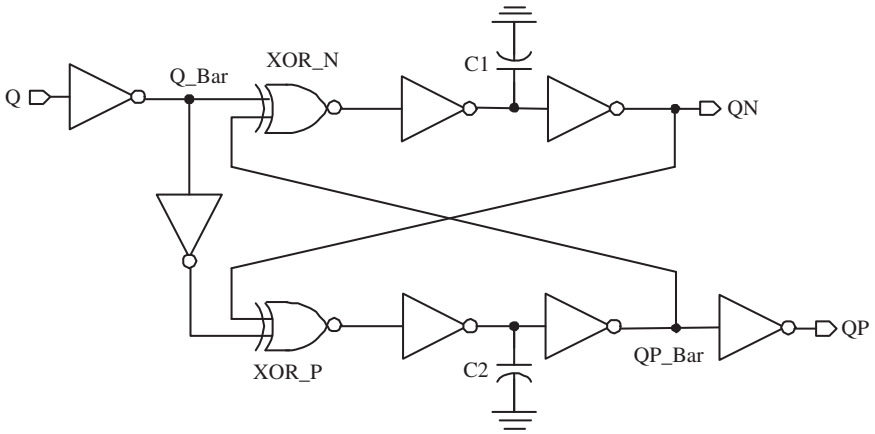

Fig. 9. Dead-time circuit.

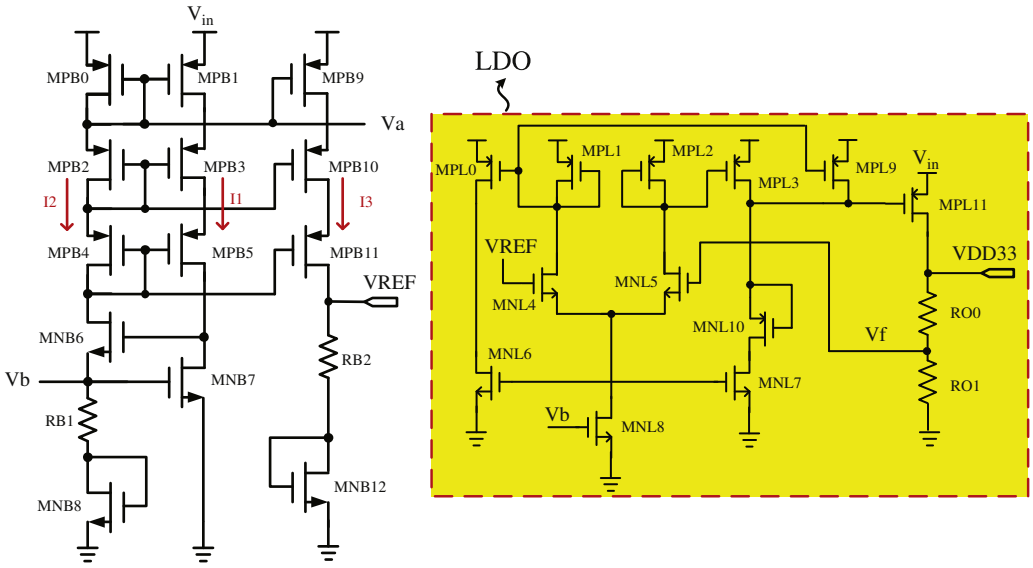

Fig. 10. Schematic of Bandgap and LDO.

A faster speed of the feedback loop comes along with a more stable output voltage.

3.4. Selection Lo and Co of off-chip passive components

Traditionally, inductors and capacitors are essential components in DC–DC buck converter designs. Besides, generating a DC voltage, they are used as a low-pass filter to reduce the ripple coupled with the output voltage. Large inductors and capacitors can reduce the ripple amplitude at the expense of high cost. We will explain how to select the appropriate Lo and Co in Fig. 3.

The load current, input and output voltages and operation frequency are the main parameters for the inductor selection. Referring to Fig. 11, t_{on} and $t_{\overline{on}}$ are the turn-on and turn-off time of power MOSs, respectively. T is the period of switching. D_{LC} denotes the ratio of t_{on} vs. T. The voltage on the inductor, Lo, can be denoted as $V_{LX}-\mathrm{Vout}$ where $V_{LX}-\mathrm{Vout}=\mathrm{Lo}(di_{Lo}/dt)$. Notably, V_{LX} is approaching to Vin, when the power MOSs are operated in saturation region. Then, Eq. (7) is attained by simple inductance formula. However, I_O, in Fig. 11, is the average value of i_{Lo}, which should be greater than zero, when the DC–DC buck converter operates in the continuous mode. Therefore, I_O should be greater than $\frac{1}{2}\Delta i_{Lo}$. Finally, the inductor selection can be derived in Eq. (9), where f is the reciprocal of period T.

$$\Delta i_{Lo}=\frac{V_{LX}-\mathrm{Vout}}{\mathrm{Lo}}\cdot D_{LC}\cdot T \tag{7}$$

$$\Delta i_{Lo}\simeq\frac{\mathrm{Vin}-\mathrm{Vout}}{\mathrm{Lo}}\cdot D_{LC}\cdot T \tag{8}$$

$$\mathrm{Lo}\geq\frac{\mathrm{Vout}\cdot(1-D_{LC})}{2\cdot \mathrm{I}_O\cdot f} \tag{9}$$

The current waveform of the capacitor is shown in the bottom of Fig. 11. The average current of the capacitor is zero, and the peak-to-peak current is Δi_{Lo}. When the current of the capacitor is larger than zero, the accumulated charge is denoted as ΔQ as shown in the gray region. Therefore, the voltage variation on the capacitor, Co, can be denoted as $\Delta\mathrm{Vout}=\Delta Q/\mathrm{Co}$. In addition, $\Delta Q=(1/2\times T/2\times 1/2)\Delta i_{Lo}=\Delta i_{Lo}/8f$. Referring to Eq. (8), the capacitor selection is derived in Eq. (10), where the ratio of output voltage variation usually must be less than 1%.

$$\mathrm{Co}=\frac{\mathrm{Vout}}{\frac{\Delta\mathrm{Vout}}{8\cdot \mathrm{Lo}\cdot f^2}(1-D_{LC})},\ \frac{\Delta\mathrm{Vout}}{\mathrm{Vout}}<1\% \tag{10}$$

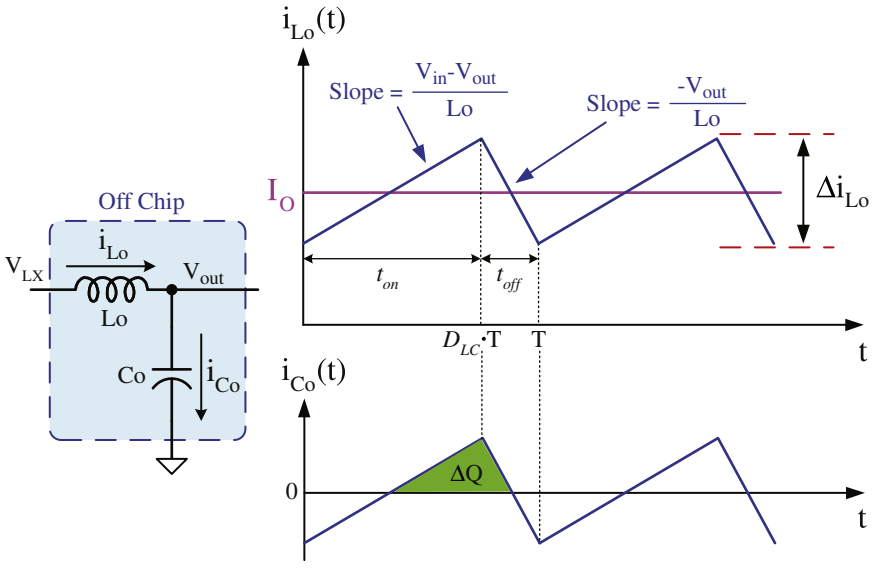

Fig. 11. Current waveforms on the inductor and capacitor.

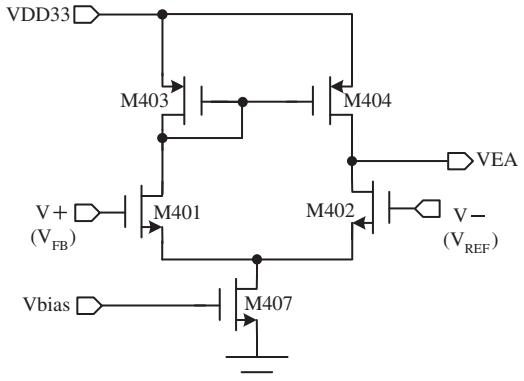

Fig. 12. Schematic of the error amplifier.

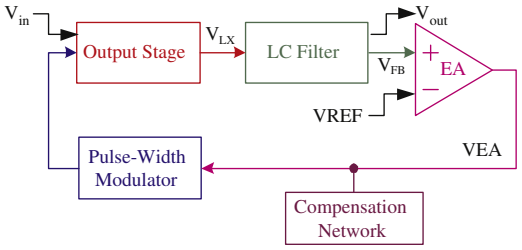

Fig. 13. Simplified system loop of the proposed buck converter.

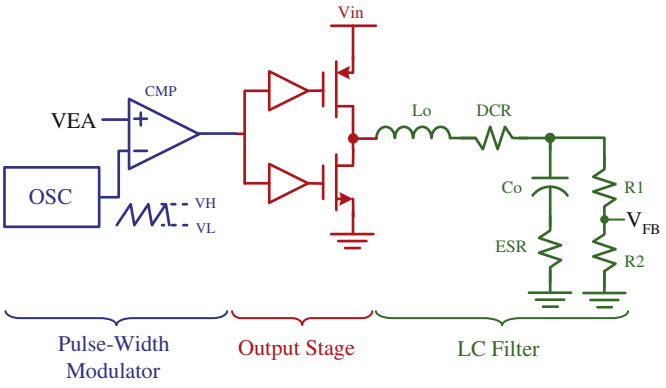

Fig. 14. Analysis of the open loop.

3.5. Design of error amplifier

The error amplifier is used to magnify the difference between reference voltage (VREF) and the feedback voltage, i.e., Vout divided by R1 and R2. The error amplifier can improve the performance of transient response. Typically, a high frequency signal will be coupled with the output voltage in SMPS designs. We should provide an appropriate low frequency gain for this kind of designs and filter out the unwanted high frequency signals. In general, an amplifier with 1 MHz bandwidth is more than enough to cope with the frequency, f_{switch}, in an SMPS design. Nevertheless, amplifiers with higher bandwidth will amplify the unwanted control signal in high frequency range to cause the system loop unstable [12,13,20]. Therefore, in this work, we employ a one-stage differential amplifier to carry out the low-bandwidth error amplifier, as shown in Fig. 12.

3.6. Stability analysis

As shown in Fig. 13, the system feedback loop in Fig. 3 can be simplified to be composed of an error amplifier (EA), a Pulse-Width Modulator, an Output Stage, an LC Filter (off-chip Lo, Co) and a Compensation Network (CPI, RPI). According to the sampling theorem, the bandwidth of this system should be smaller than half of the operation frequency, f_{switch}. In general, industrial requirements will choose one-fourth to one-fifth of the operation frequency. Besides, according to Barkhausen stability criterion, the phase margin must be designed greater than 45° [14].

Referring to Fig. 14, we start with the analysis of the open loop path, including the Pulse-Width Modulator, Output Stage and LC Filter. The frequency response of Pulse-Width Modulator is a voltage gain, Vin/(VH−VL), which is independent of frequency. LC Filter will provide a two-stage pole, LC_pole, and a zero, LC_zero, which is generated by ESR (equivalent serial resistance) of Co. Therefore, the open loop gain is denoted by Eq. (11), where DCR is the DC resistance of Lo. Fig. 15 illustrates the corresponding Bode Plot. The DC gain is generated by Pulse-Width Modulator, Output Stage, and LC Filter. Then we need to find out the gain of the system bandwidth, MidGAIN, which should be compensated by

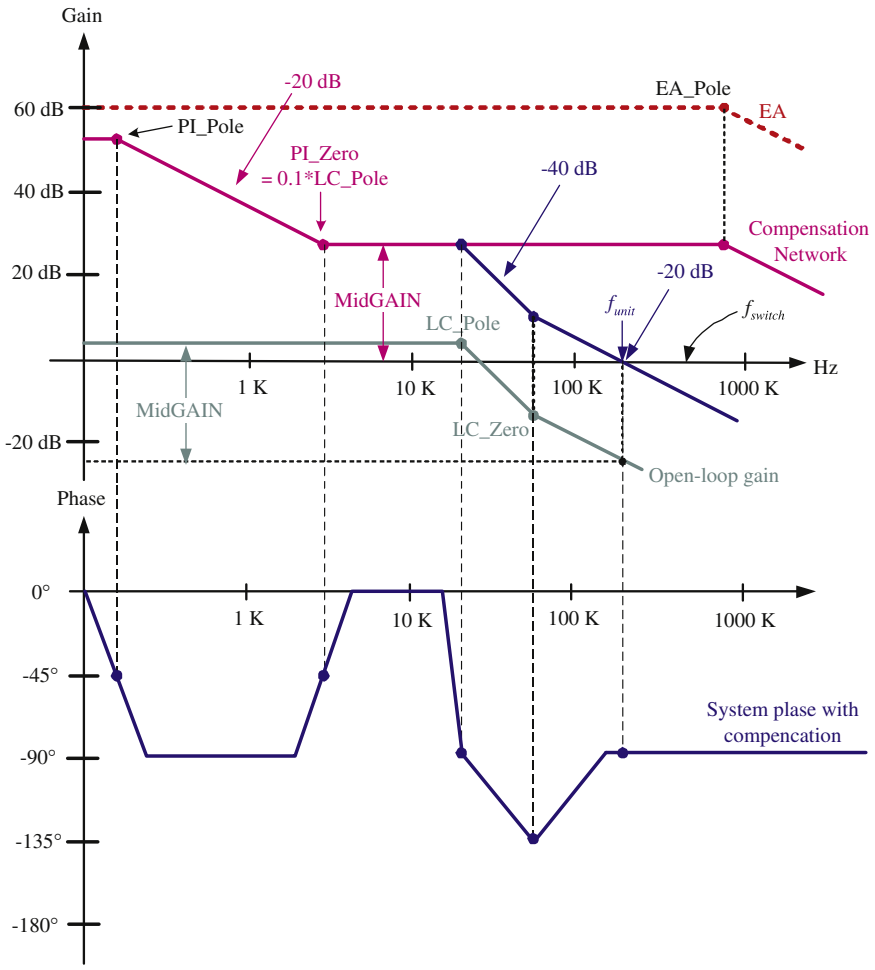

Fig. 15. The Bode Plot of the proposed design.

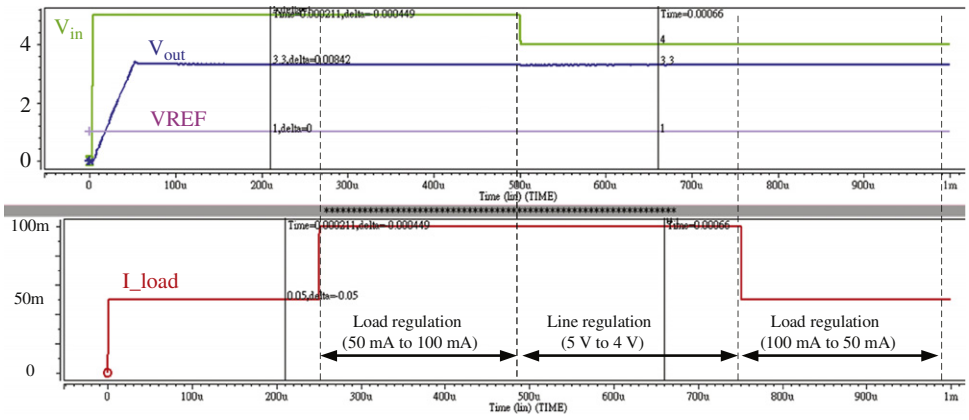

Fig. 16. Simulation waveform of line regulation and load regulation.

the Compensation Network.

$$Gain_{open\text{-}loop} = \frac{\text{Vin}}{\text{VH}-\text{VL}} \cdot \frac{1+s\cdot \text{ESR}\cdot \text{Co}}{1+s\cdot(\text{ESR}+\text{DCR})\cdot +s^2\cdot \text{Lo}\cdot \text{Co}} \tag{11}$$

Traditionally, there are two common compensation methods, Type-II and Type-III, which depend on the location of LC_zero in the system frequency response [15]. Type-II compensation net is a one zero–one pole compensation net and Type-III compensation net is a two zero–two pole compensation net. When the location of LC_zero is smaller than the system bandwidth, Type-II compensation method is good enough to compensate the system. In this work, the half operation frequency is 300 KHz, and LC_zero is located around 80 KHz. Therefore, we choose Type-II to compensate the proposed design, where the compensation components, RPI and CPI in Fig. 3, are coupled to VEA node. After the compensation, the zero, PI_Zero, is located at one-tenth of original zero pole, LC_zero, which can compensate the phase margin. The first pole of the system, PI_Pole, is used to reduce the gain in high frequency response and make sure the phase margin larger than 45°, because the slope of gain is equal to -20 dB when frequency is f_{unit}.

4. Implementation and measurement

The proposed design is implemented by a typical TSMC 0.18 μm CMOS process. The external inductor (Lo) and capacitor (Co) are 10 μH and 22 μF, respectively. The equivalent series resistance (ESR) of the capacitor is 0.1 Ω. The compensation resistor (RPI) and capacitor (CPI) is 100 KΩ and 1 nF, respectively. Fig. 16 shows the simulation waveform of line regulation and load regulation. The input voltage, Vin, varies from 5 to 4 V, and the output current varies from 100 to 50 mA. VREF is a 1.0 V. Figs. 17 and 18 show the measurement waveform of line regulation and load regulation, respectively. According to the measurement results, when the ripple voltage of Vin is 200 mV, the ripple voltage of Vout is 300 mV. The variation of Vout is roughly 34 mV even if the input voltage or the output current jumps drastically from 0 to 100 mA. Fig. 19 shows the scenario with temperature variation from −40 to +125 °C, where the internal reference voltages, i.e., VDD33, VSL, and VREF, show very tiny variation. In other words, the output voltage in this work can resist the variation of input voltage, output current, and temperature. Fig. 20 shows the efficiency comparison between simulation and measurement. The discrepancy between simulation and measurement results is about 3.5%, when the output current is larger than

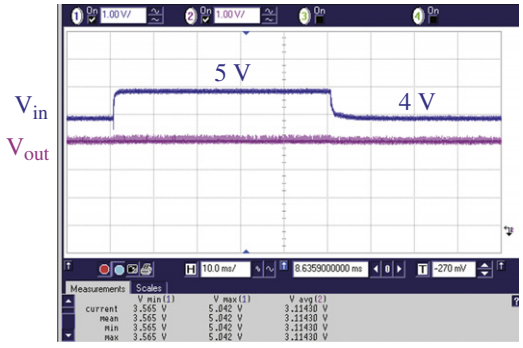

Fig. 17. Measurement waveform of line regulation.

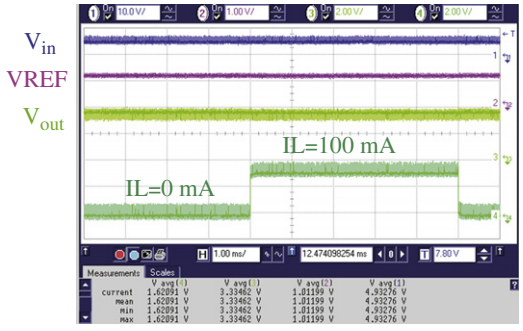

Fig. 18. Measurement waveform of load regulation.

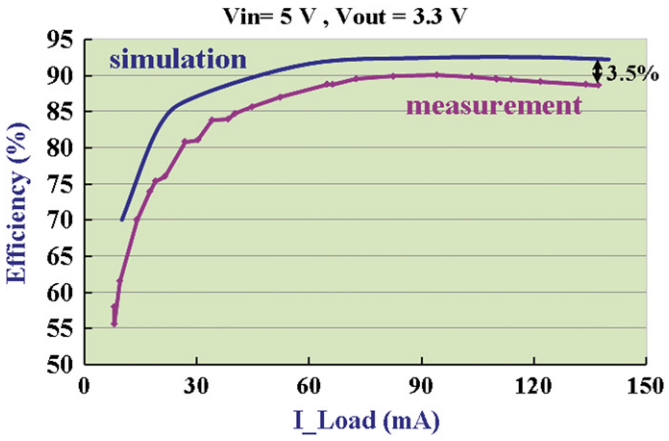

Fig. 20. Efficiency comparison between simulation and measurement.

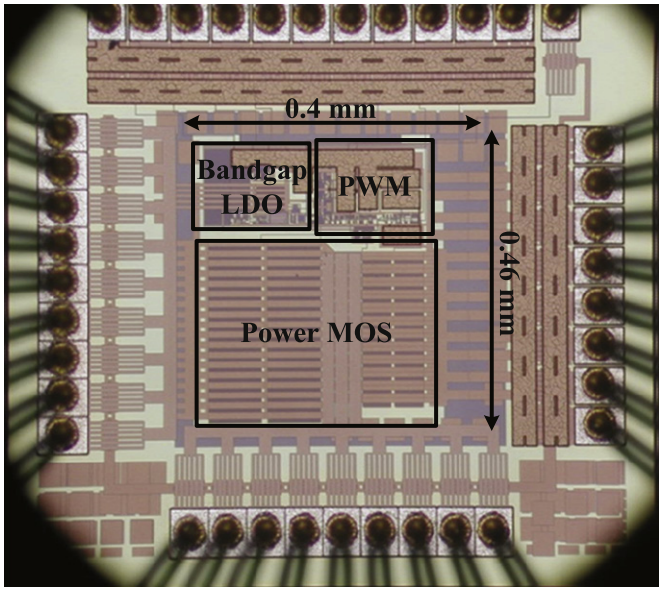

Fig. 21. Die photo of the DC–DC buck converter.

Table 2
Simulation result of line regulation and load regulation.

	Line regulation	Load regulation
Vout = 3.3 V	0.038%/V	0.343%/V
Vout = 1.8 V	0.055%/V	0.346%/V

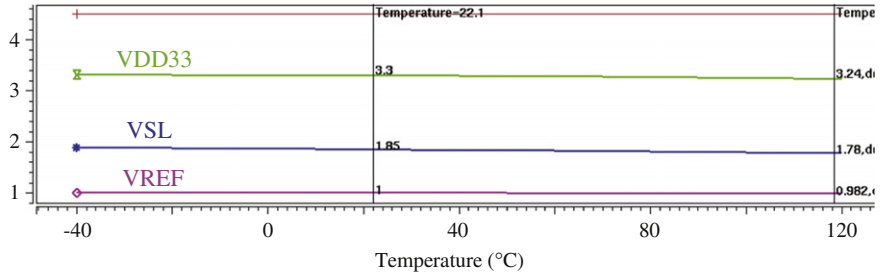

Fig. 19. Scenario with temperature variation.

Table 3
Comparison between prior works and ours.

	[16]	[17]	[18]	[20]	Ours
Year	2007	2008	2010	2010	2010
Technology (μm)	0.6	0.35	0.25	0.35	0.18
Area (mm^2)	1.353	3.57	3.57	3.14	0.184
Vin (V)	2.2−6	2.7−5	2.7−4.5	1.6−3.3	3−5
Vout (V)	0.6− Vin−0.2	1 (min)	3.3	0.9−3.0	1− Vin−0.2
Efficiency range (%)	88.5−96.7	95	96	50−96.5	89.97−90.1
Temperature (°C)	0−75	N/A	N/A	N/A	−40−125
Load current range (mA)	0.9−800	460	50−500	45−90	60−140
Maximum switching frequency (KHz)	1100	180	700	N/A	300

60 mA. Fig. 21 shows the die photo of the DC–DC buck converter. The core area is less than 0.184 mm^2. The performance of the proposed design is tabulated in Table 2.Table 3 shows a comparison between our work and prior works. The chip area, efficiency, and temperature tolerant of our design outperforms the prior works.

5. Conclusion

This paper presents a high-efficiency DC–DC step-down converter. The input voltage range can reach almost 2 times of VDD voltage through the proposed stacked power transistors without any thick-oxide device to resolve the gate-oxide reliability and leakage current problems. The maximum efficiency is 90% at Vin=4.84 V, I_{load}=94.12 mA, and temperature=25 °C. The temperature tolerance is wide enough to be used in a rugged environment, likes car electronics.

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