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A Signed Array Multiplier with Bypassing Logic

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Abstract A low power digital signed array multiplier based on a 2-dimensional (2-D) bypassing technique is proposed in this work. When the horizontally (row) or the vertically (column) operand is zero, the corresponding bypassing cells skip redundant signal transitions to avoid unnecessary calculation to reduce power dissipation. An 8×8 signed multiplier using the 2-D bypassing technique is implemented on silicon using a standard 0.18 μm CMOS process to verify power reduction performance. The power-delay product of the proposed 8×8 signed array multiplier is measured to be 31.74 pJ at 166 MHz, which is significantly reduced in comparison with prior works.

Keywords Domino effect · 2-dimensional bypassing · Partial product · Array multiplier · Bypassing logic

1 Introduction

Due to the rapid expanding of commercially portable devices, high energy-efficient demand for battery operated multimedia devices is a popular research topic. Particularly, digital multipliers are deemed as the most critical arithmetic unit in digital signal processors (DSP), which can be used to execute complicated computations, e.g., Fast Fourier Transform (FFT), inverse Fast Fourier Transform (IFFT), digital cosine transform, digital filtering, etc. [1]. Referring to prior studies, many digital multipliers have been reported to provide high speed operations, e.g., [2, 3]. Unfortunately, these digital multipliers causing high power consumption are not welcomed in portable devices. To reduce low power consumption, many prior digital multipliers have been focused on switching reduction methods. In [4], the partial computations are skipped caused by the sign extension bits. A bypassing multiplier was proposed in [5], which utilized a bypassing technique to disable the unnecessary operations of adding cells when the partial product of a row is equal to 0. However, all the above prior works are based on the 1-dimensional (1-D) bypassing technique to skip or disable the unnecessary adding cells.

Though [10] reported a 2-dimensional (2-D) bypassing multiplier to resolve the above problems of 1-D bypassing multiplier, it was only limited to unsigned multiplication. This paper proposes a signed 2-D bypassing technique, which can simultaneously detect the nullity of the partial product and multiplicand to determine whether the adding cells are skipped or not. An 8×8 signed 2-D bypassing multiplier is designed and carried out by a typical 0.18 μm 1P6M CMOS process to verify the functionality and performance on silicon. The overall performance of the proposed design is better than that of the prior designs.

2 Signed 2-Dimensional Bypassing Array Multiplier

To reduce the power dissipation, a basic conception of a digital multiplier is to avoid unwanted switching or transiting activities. This paper proposes an signed array multiplier with 2-D bypassing units, which can detect the bitwise nullity of the multiplicand in the vertical

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direction and the partial product in the horizontal direction to skip the redundant operations. The descriptions of the proposed signed 2-D bypassing array multiplier are explained in detail in following sub-sections.

2.1 Baugh–Wooley Algorithm

A signed multiplier namely, e.g., Baugh–Wooley multiplier, [6] is based on the following equations.

$$X = X_{n-1}.....X_0 = -X_{n-1}2^{n-1} + \sum_{i=0}^{n-2} X_i 2^i \tag{1}$$

$$Y = Y_{n-1}.....Y_0 = -Y_{n-1}2^{n-1} + \sum_{j=0}^{n-2} Y_j 2^j \tag{2}$$

$$\begin{aligned} P = XY = {} & X_{n-1}Y_{n-1}2^{2n-2} + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} X_i Y_j 2^{i+j} \\ & - X_{n-1}\sum_{j=0}^{n-2} Y_j 2^{n+j-1} - Y_{n-1}\sum_{i=0}^{n-2} X_i 2^{n+i-1} \end{aligned} \tag{3}$$

$$\begin{aligned} \because - X_{n-1}\sum_{j=0}^{n-2} Y_j 2^{n+j-1} \\ = X_{n-1}\left(-2^{2n-2} + 2^{n-1} + \sum_{i=0}^{n-2} \overline{X_i} 2^{n+i-1}\right) \end{aligned} \tag{4}$$

$$\begin{aligned} - Y_{n-1}\sum_{i=0}^{n-2} X_i 2^{n+i-1} \\ = Y_{n-1}\left(-2^{2n-2} + 2^{n-1} + \sum_{j=0}^{n-2} \overline{Y_j} 2^{n+j-1}\right) \end{aligned} \tag{5}$$

$$\begin{aligned} \therefore P = {} & -2^{2n-1} + \left(\overline{X_{n-1}} + \overline{Y_{n-1}} + X_{n-1}Y_{n-1}\right)2^{2n-2} \\ & + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} X_i Y_j 2^{i+j} + (X_{n-1} + Y_{n-1})2^{2n-1} \\ & - \sum_{i=0}^{n-2}\left(X_{n-1}\overline{Y_i} + Y_{n-1}\overline{X_i}\right)2^{2n-1} \end{aligned} \tag{6}$$

where X, Y, and P are the multiplier, the multiplicand, and the product, respectively. X_i, $i = n-1, ..., 0$, and Y_j, $j = n-1, ..., 0$, are, respectively, the bit representations of the multiplier and the multiplicand, and n is the length of the operands. P_k, $k = 2n-1, ..., 0$, denotes the partial products. A mathematical calculation of a Baugh–Wooley 4×4 multiplier is shown in Fig. 1.

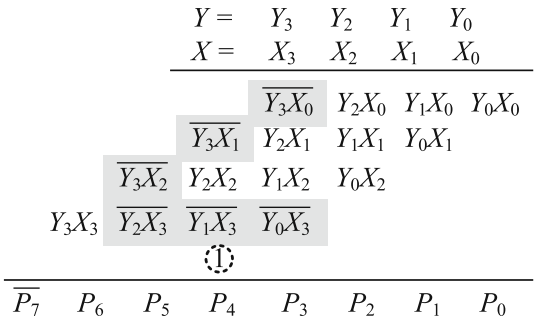

Figure 1 Mathematical calculation of the 4×4 Baugh–Wooley multiplier.

Comparing with typical unsigned multipliers, the major differences between unsigned and signed multipliers are that the partial products in the gray area of the Baugh–Wooley multiplier should be inverted and added with a "1" in the dotted circle. This is the key reason why [10] can not used for signed multiplication.

2.2 Signed 2-Dimensional Bypassing Design

In this paper, we propose a signed multiplier with a 2-dimensional bypassing technique which detects the bitwise nullity of the multiplicand bits, Y_j's, as well as the state of the multiplier, X_i's. Besides row bypassing, as soon as the Y_j is found to be zero, the results from the adding cells residing in the previous column are automatically passed to the corresponding adding cells in the next column.

2.2.1 An Adding Cell with Bypassing Logic

An adding cell with the bypassing logic is revealed in Fig. 2a. On the other hand, the adding cells without bypassing capability are shown as the one in Fig. 2b.

The product of multiplier will be wrong, if $X_{i+1} \neq$ "0" and Y_j = "1" cause the loss of the carry in signal, $C_{i-1,j}$, of AC_{ij}. According to the above illustrative example, a simple rule is introduced: if and only if X_{i+1} is not equal to "0" and the carry in of $AC_{i-1,j}$ is "1", then the adding cell, AC_{ij}, can not be bypassed. The equation of such a bypassing control signal based on the above rule is derived to $X_{i+1}\cdot(Y_j + C_{i-1,j})$.

2.2.2 Domino Effect in Long Multipliers

It is obvious that not every adding cell needs the additional bypassing logic. It will be very area-efficient if we can identify which adding cells require the bypassing logic to produce a correct multiplication result. Given

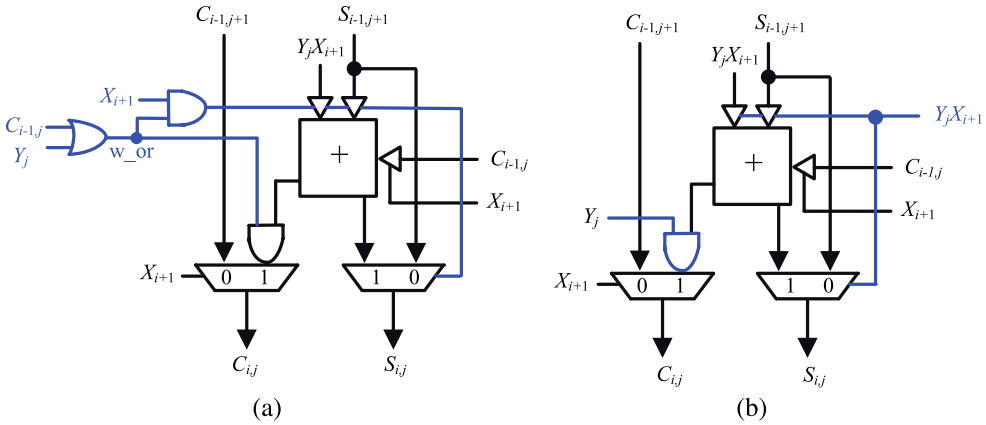

Figure 2 **a** Adding cell with bypassing logic **b** Adding cell without bypassing logic.

$n = 4$, it can be easily concluded that AC_{22} is the only unit with the necessity of a bypassing logic. If $n = 5$ and the same array structure is used, then AC_{31}, AC_{32}, AC_{33}, AC_{23} need the bypassing logic to attain correct results. By a similar induction, for any $n \times n$ multipliers, where $n \geqq 5$, all of the adding cells, AC_{ij} where $n-2 \geqq i \geqq 3, n-2 \geqq j \geqq 1$, and AC_{ij} where $i = 2$, $j = n-2$, must contain the bypassing logic to execute the correct multiplication. In other words, if $n = 8$, a total of $(8-4) \times (8-2)+1 = 25$ adding cells with bypassing logic are required, as shown in Fig. 3. Therefore, the following rule is concluded: A total of $(n-4)\times\ (n-2)+1$ adding cells with bypass logic are required to constitute a signed 2-dimensional bypassing multiplier, $\forall n > 3$.

A phenomenon of the bypassing multipliers is that if an adding cell is activated (not bypassed), then all of the other adding cells in the same column must be activated. For example, if A_{22} is activated, AC_{32} must

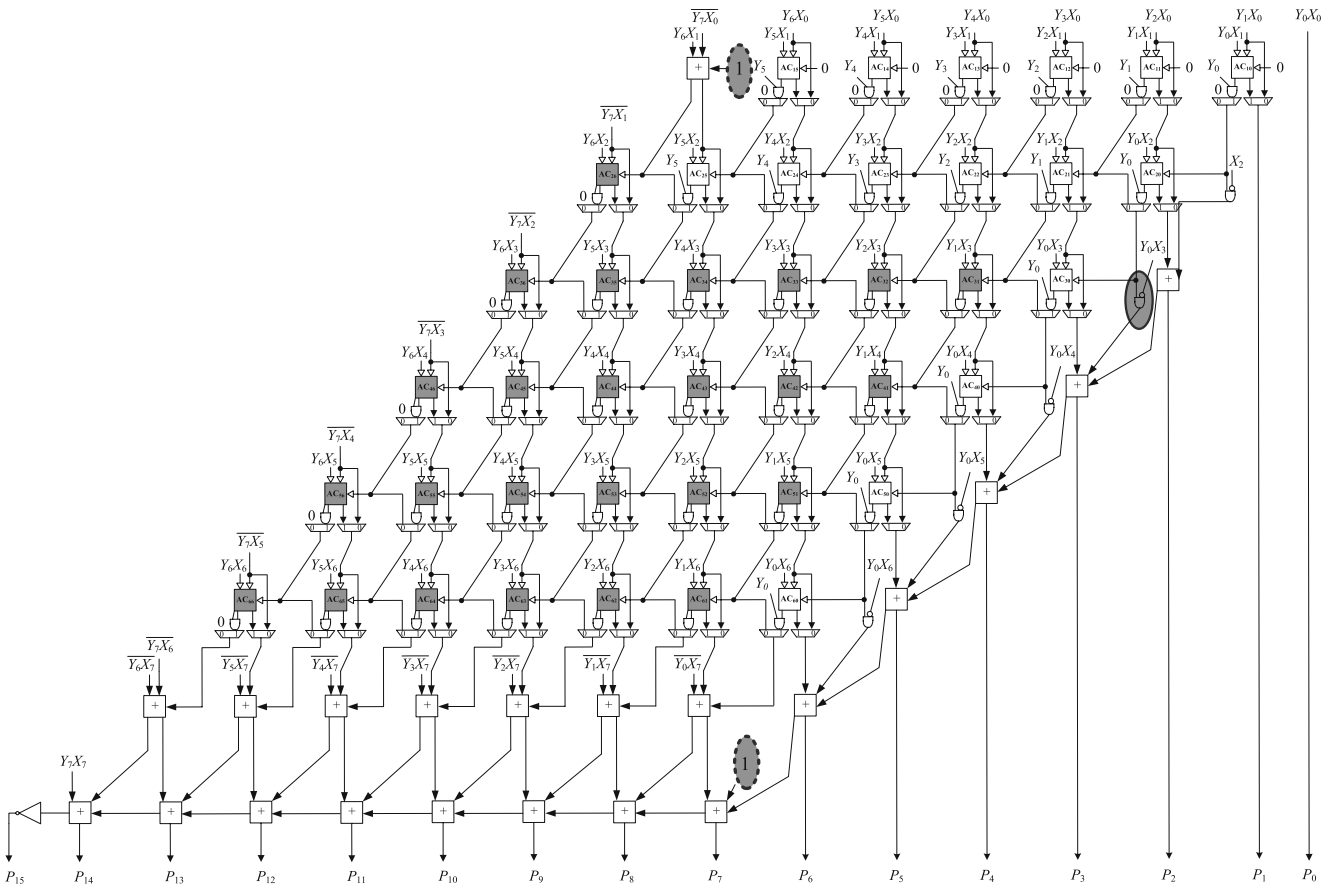

Figure 3 An 8×8 signed 2-D bypassing multiplier.

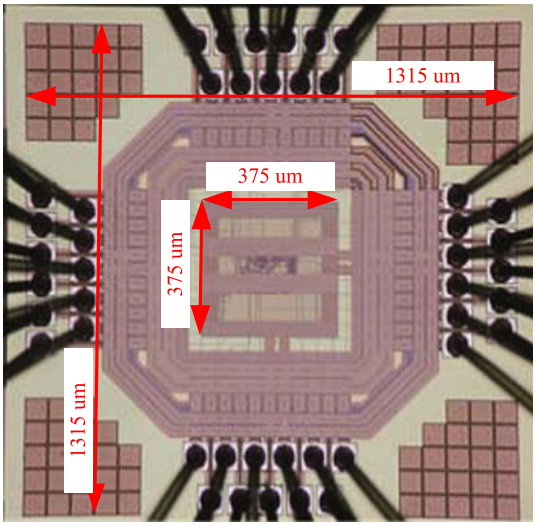

Figure 4 Die photo of the proposed 8×8 signed 2-dimensional bypassing multiplier.

be activated to deliver the carry signal to the following adding cells to ensure the correctness of carry propagation and logical operation. This phenomenon is named "domino effect" of the 2-D bypassing multipliers.

3 Implementation and Measurement

TSMC (Taiwan Semiconductor Manufacturing Company) standard 0.18 μm 1P6M CMOS technology is used to carry out the proposed 8×8 signed 2-dimensional bypassing multiplier. The functional simulations of the proposed design have been simulated at all PVT (process, voltage, temperature) corners. The power consumption of the proposed design is 1.1912 mW at a 166 MHz clock.

Figure 4 shows the die photo of the proposed 8×8 signed 2-D bypassing multiplier. The core area of the chip is 375×375 μm^2. In the on-silicon measurement, the testing vectors are generated by the pattern generator of Agilent 16702B Logic Analysis System using a PRSG (pseudo-random number sequence generator) to generate 10,000 random numbers. Figure 5 shows parts of the testing vectors. The output waveforms of the physical measurement on silicon is given in Fig. 6.

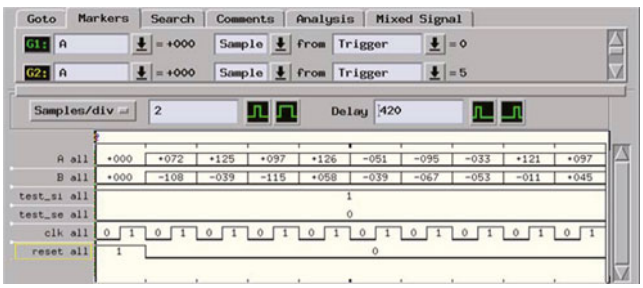

Figure 5 Testing vectors for the proposed 8×8 signed 2-D bypassing multiplier.

Figure 6 Output waveforms of the proposed 8×8 signed 2-D bypassing multiplier.

Table 1 Comparison with prior works.

	Proposed	[7]	[8]	[9]
Process (μm)	0.18	0.6	0.18	0.35
Supply voltage (V)	1.8	3.3	1.8	3.3
Frequency (MHz)	166	20	28.6	500
Delay (ns)	6	5.47	34.97	2
Power (mW)	5.27	7.895	N/A	67.38
PDP (pJ)	31.74	43.19	N/A	134.76
Latency	1	1	1	1
Year	2010	2009	2008	2008

Table 1 shows the comparison of the proposed design with several prior works. As shown in Table 1, the proposed signed array multiplier attains the second best PDP and the lowest power dissipation.

4 Conclusion

A digital signed array multiplier taking advantage of a 2-dimensional bypassing method to achieve power-saving is proposed in this paper. A 8×8 signed multiplier composed of adding cells with bypassing logics is implemented to verify the functionality and low power performance. By on-silicon measurement, the power consumption of the proposed design is 5.27 mW at a 166 MHz clock. Compared with several prior works, the proposed design attains appealing power consumption performance and the lowest number of latency.

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