

A ROM-less DDFS Based on a Parabolic Polynomial Interpolation Method with an Offset

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Abstract A novel direct digital frequency synthesizer (DDFS) based on a parabolic polynomial with an offset is proposed in this paper. A 16-segment parabolic polynomial interpolation is adopted to replace the traditional ROM-based phase-to-amplitude conversion methods. Besides, the proposed parabolic polynomial interpolation is realized in a multiplier-less structure such that the speed can be significantly improved. This work is manufactured by a standard 0.13 μm CMOS cell-based technology. The maximum clock rate is 161 MHz, the core area is 0.33 mm^2 , and the spurious free dynamic range (SDRF) is 117 dBc by physical measurements on silicon.

Keywords Direct digital frequency synthesizer (DDFS) · Interpolation · Spurious free dynamic range (SFDR)

1 Introduction

The frequency synthesizer is an important component of communication systems. Conventionally, phase-lock loops (PLLs) [1, 2] are usually adopted to synthesize sinusoid waves. However, the PLL-based frequency synthesizers can not provide fast frequency switching and high spectral purity sine outputs at the same time [3]. This deficiency makes PLLs inadequate for modern wireless communication systems demanding fast

frequency switching. The direct digital frequency synthesizer (DDFS) has been considered as a better alternative rather than PLL-based frequency synthesizers. The reason is that DDFS can provide fast frequency switching and excellent spectral purity.

A conventional DDFS architecture is shown in Fig. 1. The digital phase is converted into samples of sine amplitude by a ROM look-up table. Then, the sample values are converted into analog signals by a Digital-to-Analog Converter (DAC). However, this architecture has an intrinsic difficulty: it demands a very large ROM as the storage of the sinusoid amplitudes. Thus, it suffers from the inherent drawbacks of large power dissipation, large chip area, and slow speed. Although the ROM size can be significantly reduced by truncating the output of the phase accumulator, the added spurious noise will degrade the spectral purity.

On the other hand, many researches have been reported on the designs of ROM-less DDFS, e.g., [4–8]. The ROM-less DDFSs utilized different algorithms instead of ROM tables to realize the phase-to-sine mapper. Many prior ROM-less DDFS works demanded complicated polynomials to carry out the phase-to-sine mapper. However, any method based on high-order polynomials will be hard to meet the high speed requirement of modern wireless communication applications due to the intrinsic massive computation complexity. Considering the feasibility of hardware realization, any polynomial whose order is larger than three may be inefficient to be implemented. By contrast, lately reported DDFSs based on 2nd-order polynomials can not achieve high performance without sacrificing the speed. This paper proposes a DDFS based on a 2nd-order parabolic polynomial with an offset to resolve all of the mentioned difficulties. The

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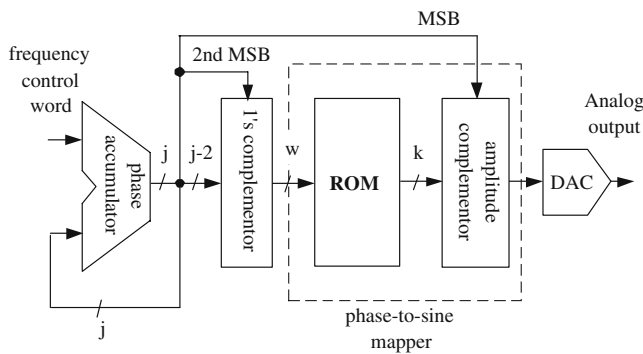


Figure 1 The conventional DDS structure.

proposed DDS can simultaneously achieve an exceptional spectral purity and a satisfactory speed.

2 The Proposed DDS Architecture

2.1 Prior Parabolic Polynomial Interpolation Methods

To implement the phase-to-sine mapping function by a 2nd-order polynomial, the parabolic polynomial could be the most convenient choice. The first quadrant of the cosine signal ($\cos \theta, 0 \leq \theta < \pi/2$) can be divided into $M = 2^m$ segments, and each segment can be approximated by the parabolic polynomial, which is expressed as follows:

$$y(x) = a_i x^2 + c_i, \quad i = 1 \sim M. \quad (1)$$

where the parameter a_i and c_i can be derived by the least square method. Although the SFDR of this DDS

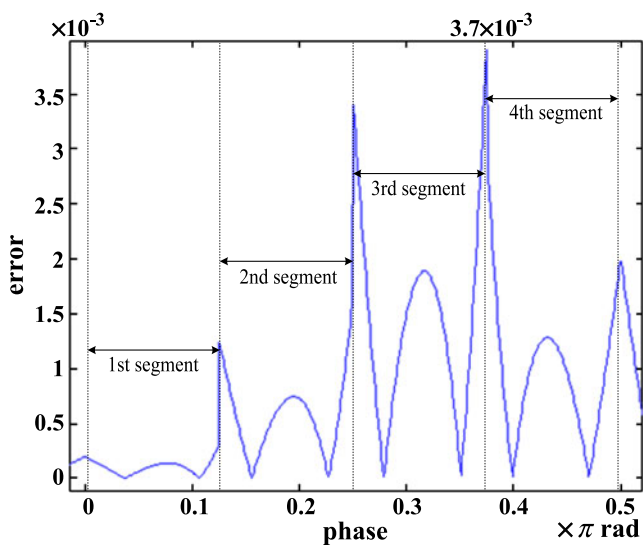


Figure 2 The error between the ideal cosine function and the QLIP method ($M = 4$).

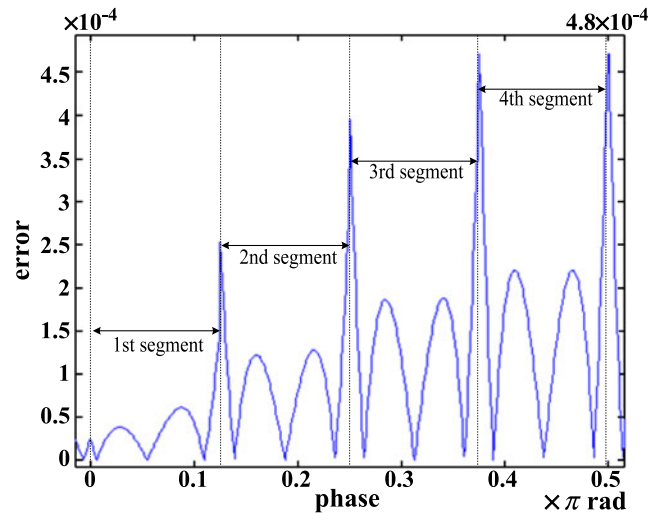


Figure 3 The error between the ideal cosine function and the proposed method ($M = 4$).

will be increased as the increase of M , large M will lead to divergence when performing the least square method.

Ashrafi and Adhami [4] proposed a quasi-linear interpolation method (QLIP) to improve the performance of the DDS based on the parabolic polynomial. It was based on the observation that a cosine signal is close to a parabola at the vicinity of $\theta = 0$. Meanwhile, it is more like a straight line around $\theta = \pi/2$. The QLIP method can be expressed as follows:

$$y(x) = \begin{cases} a_i x^2 + c_i, & 1 \leq i \leq 3M/4 \\ a_i x + c_i, & 3M/4 + 1 < i \leq M. \end{cases} \quad (2)$$

According to [4], the QLIP method attained a 6 dBc improvement over the parabolic polynomial method.

Both the QLIP and the parabolic polynomial method have the same difficulty in fitting the curvature of the sinusoid. The curvature of a given curve $y = f(x)$ can be expressed as follows:

$$k(x) = \frac{y''}{(1 + y'^2)^{3/2}}, \quad (3)$$

Table 1 The SFDR of the QLIP method and the proposed method under different M .

	QLIP method [4]	Proposed method
$M = 4$	65 dBc	81.3 dBc
$M = 8$	78 dBc	99 dBc
$M = 16$	90 dBc	117.3 dBc

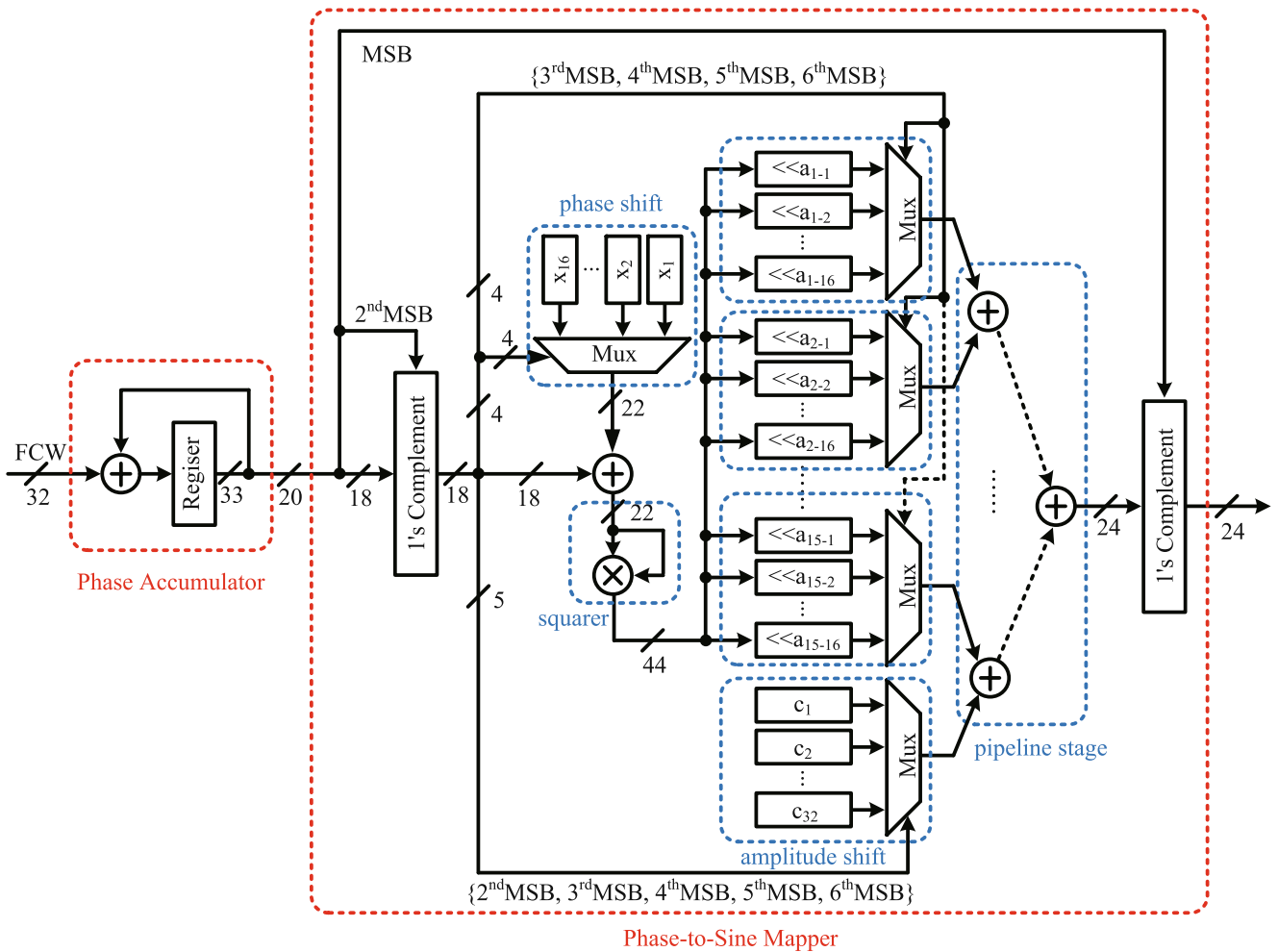


Figure 4 The block diagram of the proposed DDS.

where $k(x)$ is the curvature at x . If the parabolic polynomial is used, its 1st-order derivative ($y' = 2a_i x$) is proportional to the 2nd-derivative ($y'' = 2a_i$). Thus, if

only one parameter a_i is used to determine both the slope and the curvature of the curve, the fitting will be hard.

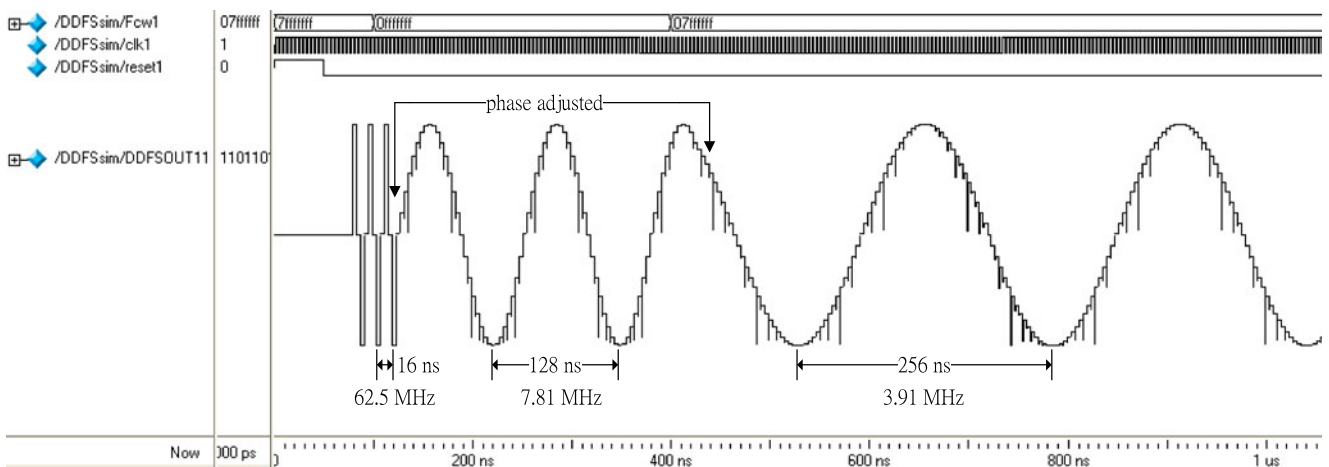


Figure 5 Post-layout simulation result without coupled to a DAC.

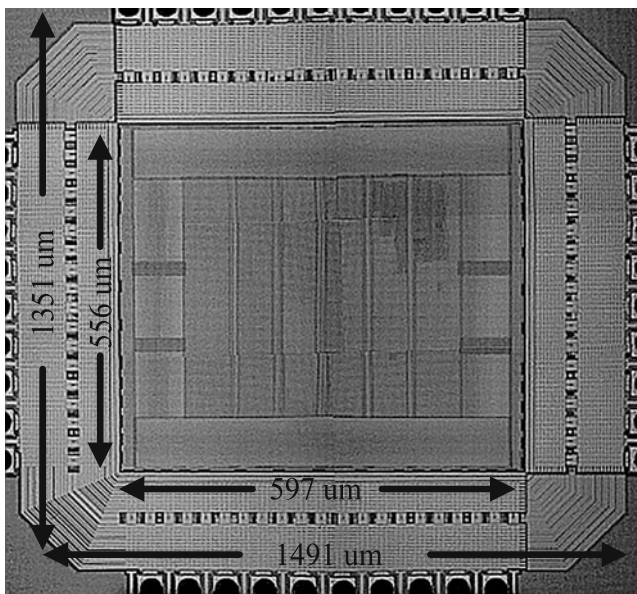


Figure 6 The die photo of the proposed DDFS.

2.2 Proposed Parabolic Polynomial Interpolation

Therefore, to enhance the adjustability of the parabolic polynomial, we introduce a 1st-order term, which is called the “offset”, into Eq. 1,

$$y(x) = a_i(x + x_i)^2 + c_i, \quad i = 1 \sim M \quad (4)$$

where x_i is the displacement factor, i.e., “offset”, for segment i . The coefficient “ x_i ” is derived by the variation between a ideal sine wave and the generated sine wave. When Eq. 3 is used to carry out the phase-to-sine mapping function, there are two parameters that can be used to adjust the characteristics of the curve in each segment.

2.3 Iterative Derivation of Offsets

We start with an initial value 0 for factor x_i , and then use the least square method to derive a_i and c_i , respectively. Equation 4 can be expanded to M segments and re-formulated to be Eq. 5. After multiplying the

transpose of the first matrix at the righthand side of Eq. 5, we attain Eq. 6. Thus, the coefficients a_i and c_i can be derived, which is expressed as Eq. 7. Finally, the approximated sine wave amplitude in Eq. 5 can be rewritten as Eq. 8.

According to Eq. 8, we can derive the coefficient x_i to find the least square error. Then, back-substitute x_i into Eq. 7 such that a_i and c_i are derived, respectively.

2.4 Performance Evaluation

To evaluate the performance of the proposed parabolic polynomial, we carry out different DDFSs based on these three methods, Eqs. 1, 2, ours in Eq. 4, and compare their performance. The coefficients of these DDFSs are derived by the least square method of MATLAB, where the output of these DDFSs are not quantized. Figures 2 and 3 show the computed error of the QLIP method and the proposed method, where the maximum error is 3.77×10^{-3} and 4.8×10^{-4} , respectively. It is obvious that the proposed method is superior in terms of accuracy.

Then, we try to distinguish our method from QLIP in terms of SFDR. Table 1 shows the SFDR comparison between the QLIP method and the proposed method with different numbers of segments. The SFDR of the proposed method for $M = 16$ has almost 27 dBc improvement over that reported in [4]. Regarding the computation complexity, Eq. 4 needs only one more addition/subtraction than Eq. 2. However, this overhead is acceptable compared to the significant improvement of the spectral purity. Since 100 dBc SFDR meets the requirement of many modern wireless communication applications, we adopt the 16-segment parabolic polynomial with an offset method to realize the proposed DDFS.

$$\begin{bmatrix} y_1 \\ y_2 \\ y_2 \\ \vdots \\ y_M \end{bmatrix} = \begin{bmatrix} (x + x_1)^2 & 1 \\ (x + x_2)^2 & 1 \\ (x + x_3)^2 & 1 \\ \vdots & \vdots \\ (x + x_M)^2 & 1 \end{bmatrix} \begin{bmatrix} a_i \end{bmatrix} \quad (5)$$

Figure 7 The measurement of the proposed DDFS.

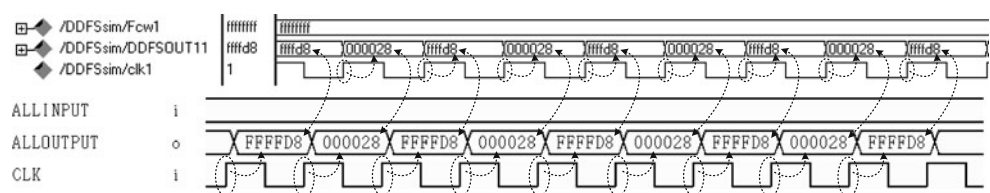
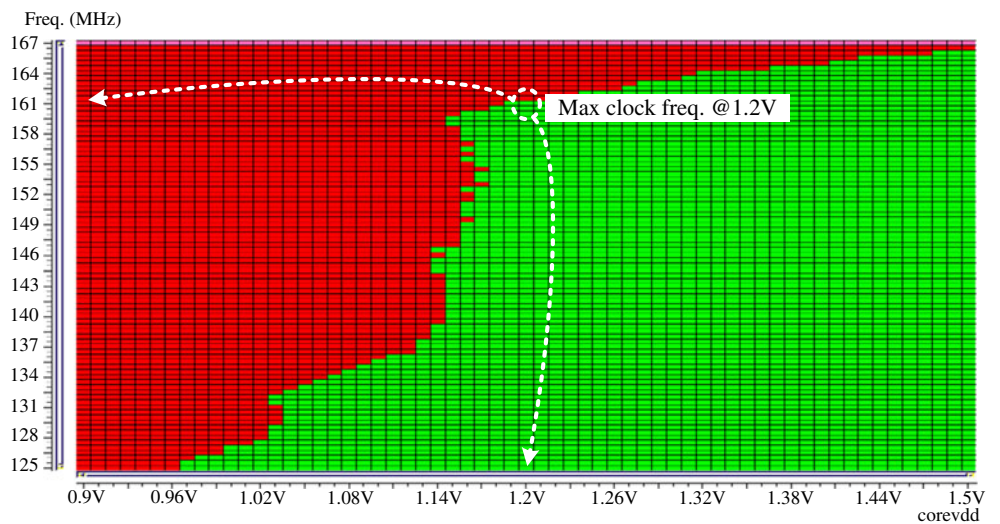


Figure 8 The SHMOO diagram.



$$\begin{bmatrix} (x+x_1)^2 & 1 \\ (x+x_2)^2 & 1 \\ (x+x_3)^2 & 1 \\ \vdots & \vdots \\ (x+x_M)^2 & 1 \end{bmatrix}^T \begin{bmatrix} y_1 \\ y_2 \\ y_3 \\ \vdots \\ y_M \end{bmatrix} = \begin{bmatrix} (x+x_1)^2 & 1 \\ (x+x_2)^2 & 1 \\ (x+x_3)^2 & 1 \\ \vdots & \vdots \\ (x+x_M)^2 & 1 \end{bmatrix} \begin{bmatrix} a_i \\ c_i \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} a_i \\ c_i \end{bmatrix} = \left(\begin{bmatrix} (x+x_1)^2 & 1 \\ (x+x_2)^2 & 1 \\ (x+x_3)^2 & 1 \\ \vdots & \vdots \\ (x+x_M)^2 & 1 \end{bmatrix}^T \begin{bmatrix} (x+x_1)^2 & 1 \\ (x+x_2)^2 & 1 \\ (x+x_3)^2 & 1 \\ \vdots & \vdots \\ (x+x_M)^2 & 1 \end{bmatrix} \right)^{-1} \times \begin{bmatrix} (x+x_1)^2 & 1 \\ (x+x_2)^2 & 1 \\ (x+x_3)^2 & 1 \\ \vdots & \vdots \\ (x+x_M)^2 & 1 \end{bmatrix}^T \begin{bmatrix} y_1 \\ y_2 \\ y_3 \\ \vdots \\ y_M \end{bmatrix} \quad (7)$$

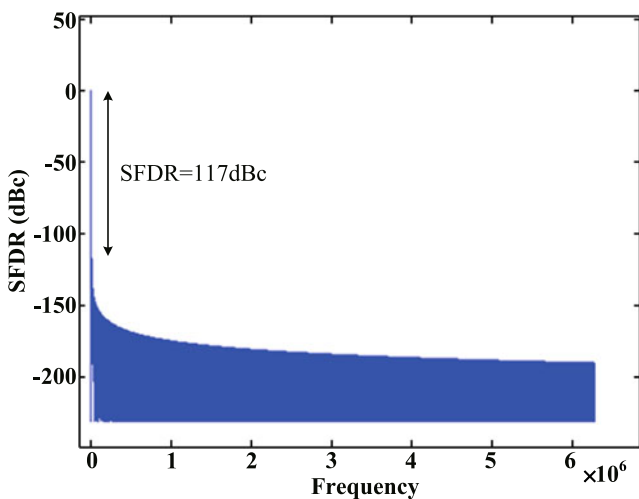


Figure 9 Spurious performance of the proposed DDFS.

$$\begin{bmatrix} y'_1 \\ y'_2 \\ y'_3 \\ \vdots \\ y'_M \end{bmatrix} = \begin{bmatrix} (x+x_1)^2 & 1 \\ (x+x_2)^2 & 1 \\ (x+x_3)^2 & 1 \\ \vdots & \vdots \\ (x+x_M)^2 & 1 \end{bmatrix} \times \left(\begin{bmatrix} (x+x_1)^2 & 1 \\ (x+x_2)^2 & 1 \\ (x+x_3)^2 & 1 \\ \vdots & \vdots \\ (x+x_M)^2 & 1 \end{bmatrix}^T \begin{bmatrix} (x+x_1)^2 & 1 \\ (x+x_2)^2 & 1 \\ (x+x_3)^2 & 1 \\ \vdots & \vdots \\ (x+x_M)^2 & 1 \end{bmatrix} \right)^{-1} \cdot \begin{bmatrix} (x+x_1)^2 & 1 \\ (x+x_2)^2 & 1 \\ (x+x_3)^2 & 1 \\ \vdots & \vdots \\ (x+x_M)^2 & 1 \end{bmatrix}^T \begin{bmatrix} y_1 \\ y_2 \\ y_3 \\ \vdots \\ y_M \end{bmatrix} \quad (8)$$

Table 2 Specifications of the proposed DDFS.

Technology	0.13 μm CMOS process
Power supply	1.2 V
Frequency control word (FCW)	32 bits
Phase word	20 bits
Frequency tuning range	0.053 Hz
SFDR	117.3 dBc
Output resolution	24 bits
Max. clock rate	161 MHz
Gate count	17,767
Power dissipation	3.56 mW @ 161 MHz (core) 69.83 mW @ 161 MHz (PAD)
Area	2.015 mm^2 (whole chip) 0.33 mm^2 (core area)

2.5 Hardware Implementation

Considering the hardware implementation feasibility of the DDFS based by the proposed parabolic polynomial, we must choose a suitable length of the phase word. The reason is that the phase word-length determines the performance and the complexity of the phase-to-sine mapper. According to [9], the worst case SFDR for a DDFS with a perfect phase-to-sine mapper (unquantized output) can be expressed as Eq. 9:

$$\text{SFDR} < 20 \cdot \log 2^W \quad (9)$$

where W is the phase word-length. Since the simulation result shows the SFDR of the proposed methods for $M = 16$ is 117.3 dBc, the phase word-length is chosen to be 20 bits.

Given the phase word-length of 20 bits, the hardware complexity is certainly increased to slow down the operation speed. To enhance the speed, the multiplication in Eq. 4 should be removed to reduce the complexity. In our implementation, coefficient a_i is manipulated as a 15-bit binary sequence, and therefore the multiplication can be replaced by the shift-and-add operation (Ex: $0.75 \cdot x = 2^{-1} \cdot x + 2^{-2} \cdot x$). Figure 4 shows the entire hardware block diagram of the proposed DDFS. The

frequency control word (FCW) is 32 bits to obtain a fine frequency tuning range. The output of the squarer is shifted and selected by multiplexers. The symbol a_{i-j} in Fig. 4 represents the j -th bit of the sequence for the i -th segment. The summation of the total 16 multiplexer's outputs is realized by a 4-level adder tree. To reduce the latency caused by the adder tree, the summation is implemented by a 4-stage pipeline structure.

3 Implementation and Measurement

The proposed DDFS prototype is carried out by a standard 0.13 μm CMOS technology to verify the performance. All of the PVT (pressure, voltage, and temperature): $[0^\circ\text{C}, +100^\circ\text{C}]$, $\text{VDD} \pm 10\%$, and (SS, SF, TT, FS, FF) models, are simulated. The frequency transition from 62.5 MHz to 3.91 MHz sine output given the worst condition (SS Model, 0°C , $f_{\text{clock}} = 227$ MHz) is shown in Fig. 5, where f_{clock} means the operation frequency. The die photo of the proposed DDFS is shown in Fig. 6.

The proposed prototype is verified by the Agilent 93000 SOC test system, which shows that the measured data exactly match the expected results. Figure 7 shows the measurement result. The output values (ALLOUT-PUT) match the simulation results (DDFSOUT11). Figure 8 exhibits the SHMOO diagram, which shows that the maximum clock range at 1.2 V power supply is 161 MHz.

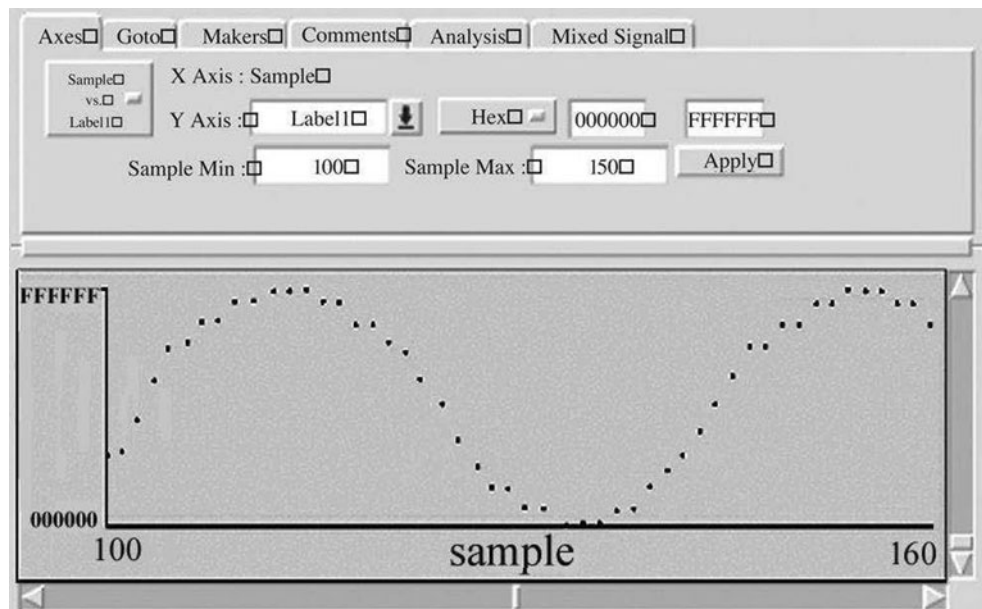
Figure 9 shows the spurious performance of the proposed method is as high as 117.2 dBc. The specifications of the proposed prototype is summarized in Table 2. Table 3 presents the comparison between the proposed DDFS and several recent ROM-less DDFS designs. The comparison shows that the proposed DDFS has the largest SFDR while maintaining the satisfactory speed and energy efficiency. The waveform of the synthesized sine wave derived from the measured samples by the Agilent 16702B logic analyzer is shown in Fig. 10.

Table 3 Comparison of DDFS designs.

	[6]	[7]	[10]	[11]	[12]	[13]	[14]	Ours
Process (μm)	0.5	0.25	0.35	0.35	*	*	*	0.13
Type	sine	quad	sine	quad	quad	quad	quad	sine
SFDR (dBc)	91.51	80	35	80	95.11	50.89	69.3	117.3
Phase accumulator bits	16	24	8	18	12	15	7	20
Output resolution (bits)	14	12	8	16	10	14	n/a	24
Power (mW/MHz)	0.56	0.127	410	0.81	2.18	1,044.35	2.4	0.35
Max. clock (MHz)	106	600	2,000	100	221	11.25	201	161
Area (core) mm^2	2.489	n/a	n/a	n/a	n/a	n/a	n/a	0.33
Area (with pad) mm^2	n/a	0.09	3.99	n/a	n/a	n/a	n/a	2.015
Year	2005	2005	2005	2006	2007	2008	2008	2009

*The DDFS design was implemented by FPGA (Field Programmable Gate Array).

Figure 10 Waveform samples of the synthesized sine wave.



4 Conclusion

A parabolic polynomial with an offset to realize the phase-to-sine mapping function of a DDFS is presented in this paper. The proposed method can achieve a significant improvement in SFDR compared to the QLIP method [4]. A 16-segment parabolic polynomial is employed to implement a ROM-less DDFS. The logic operation of the proposed DDFS is manipulated to achieve a multiplier-less design. The pipeline design is adopted to further reduce the latency in signal processing. The proposed DDFS achieves a SFDR of 117 dBc, and the maximum frequency of the synthesis sine wave is 161 MHz.

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