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Energy-Efficient Double-Edge Triggered Flip-Flop

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Abstract This paper presents a novel design for a double-edge triggered flip-flop (DETFF). A detailed analysis of the transistors used in the DETFF is carried out to determine the critical path. Therefore, the proposed DETFF employs low-V_{th} transistors at critical paths such that the power-delay product as well as the large area consumption caused by the low-V_{th} transistors can be resolved simultaneously. Therefore, the proposed DETFF fully utilizes the multi-V_{th} scheme provided by advanced CMOS processes without suffering from a large area penalty, slow clock frequency, and poor noise immunity. The proposed design is implemented using a typical 0.18-μm 1P6M CMOS process. The measurement results reveal that the proposed DETFF reduce the power-delay product by at lease 25% (i.e., dissipated energy).

Keywords Double-edge triggered · Flip-flop · Low power · Multiple V_{th} · Clocking

1 Introduction

A double-edge triggered flip-flop (DETFF) can latch digital data signal switches at both the rising and the falling edges. In other words, DETFFs allow system designers to use a slower frequency clock while maintaining the same data throughput. In addition, the power dissipation is expected to be reduced by half without any significant negative impact. DETFF can thus be used in many VLSI signal processing applications, especially in register and latch intensive SOC (system-on-chip) applications [12–14]. Double-edge triggering or latching is also widely used in pipelining designs, e.g., [1, 2], to reduce the sequencing overhead. Many DETFF-related researches have been reported thus for, including [3–10]. Lu and Ercegovac [6] is probably one of the earliest works to resolve the demands of double-edge triggering. The states of the cross-coupled pairs in the two latches do not flip easily, which in turn decreases the operating frequency. The solution reported in [3] mainly focused on the speed rather than the power consideration. Johnson and Kourtev [4] successfully integrated a PTL (pass transistor logic)-based XOR gate with a pair of back-to-back inverter pairs such that the number of transistors was reduced. The DETFF in [8] was designed specifically for TSPC (true-single-phase-clocking) logic.

With the increasing developments in CMOS technologies, multiple V_{th} (threshold voltage) transistors can be fabricated on a single die. Such rapid developments have led to increased emphasis on realizing further improvements in the performance of DETFF designs by using deep sub-micron CMOS processes. For instance, [5] proposed the use of a low-swing scheme to resolve the power dissipation problem. Low-V_{th} NMOS transistors are driven by the clock and the inverted clock. However, a total of three back-to-back inverter pairs are required. Sung et al. [7] reported a full-low-V_{th} DETFF that actually replaces all of the transistors in the DETFF described in [4] with low-V_{th} transistors. Obviously, the power consumption is reduced in such a design. However, methods using multi-V_{th} suffer from

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the problem that low-V_{th} transistors occupy a larger area than normal transistors. Moreover, several side effects are caused. First, the subthreshold current is increased, which is undesirable in the standby mode. Second, the noise immunity worsens because of the reduction in the threshold voltage. Therefore, it is necessary to determine the critical path in a DETFF and determine which transistors can be suitably replaced by low-V_{th} MOS.

2 Low-Energy DETFF Design

With the rapid developments in CMOS technology, multiple threshold voltage transistors have now become available. In this study, dual threshold voltage transistors manufactured by a typical 0.18-μm 1P6M CMOS process are used to construct a DETFF.

2.1 Current Analysis of Dual-V_{th} Transistors

The drain current in the saturation region of a MOSFET transistor is given by

$$I_D = \frac{k_p}{2}\frac{W_{\text{eff}}}{L_{\text{eff}}}(V_{GS} - V_{\text{th}})^2, \tag{1}$$

where k_p is the process parameter and W_{eff} and L_{eff} are the effective width and length of the transistor, respectively. According to Eq. 1, a lower threshold voltage transistor can produce a larger drain current. Furthermore, if we consider $\frac{W_{\text{eff}}}{L_{\text{eff}}}$ to be constant, then Eq. 1 can be derived as $I_D \propto (V_{GS} - V_{\text{th}})^2$.

Consider a TSMC 0.18-μm 1P6M CMOS process as an illustrative example. The threshold voltages of normal (high) NMOS/PMOS and medium (low) NMOS/PMOS are listed in Table 1. For the NMOS, V_{GS} = VDD = 1.8 V, the high threshold voltage $V_{\text{th}-n}$ = 0.48 V, and the low threshold voltage $V_{\text{th}-m}$ = 0.23 V. Therefore, we can calculate the ratio of $\frac{I_{DH}}{I_{DL}}$ as

$$\frac{I_{DH}}{I_{DL}} = \frac{(V_{GS} - V_{\text{th}-n})^2}{(V_{GS} - V_{\text{th}-m})^2} = \frac{(1.8 - 0.48)^2}{(1.8 - 0.23)^2}, \tag{2}$$

Table 1 Characteristics of MOS transistors in a 0.18-μm CMOS process.

	Normal N	Medium N	Normal P	Medium P
V_{th} (V)	0.48	0.23 V	−0.49	−0.28
W/L (nm/nm)	220/180	220/300	220/180	220/250
Area (μm^2)	0.92×1.5	0.92×1.78	1.08×2	1.6×2.59
Area penalty	0	+18.67%	0	+91.85%

W/L denotes the feature size of the MOS transistors.

where I_{DH} and I_{DL} are the drain currents of the high and the low threshold voltage transistor, respectively. Therefore, the current increases by approximately 40%.

On the other hand, with the decrease in the transistor operating voltage, the threshold voltage decreases as well. The subthreshold current is calculated as

$$I_{\text{DSUB}} = \frac{W_{\text{eff}}}{W_o} \cdot I_o \cdot 10^{(V_{GS} - V_{\text{th}})/S}, \tag{3}$$

where W_o and I_o are the gate width and drain current, respectively. S is the subthreshold swing parameter, and it can be calculated as

$$S \approx 2.3 V_T \left[1 + \frac{C_d}{C_{ox}}\right], \tag{4}$$

where V_T is the thermal voltage and C_d, the junction capacitance between the source and the drain. The leakage current can be obtained by replacing V_{GS} with 0 as

$$I_{\text{leak}} = \frac{W_{\text{eff}}}{W_o} \cdot I_o \cdot 10^{-V_{\text{th}}/S}. \tag{5}$$

If W_o remains unchanged, then I_{DSUB} as well as I_{leak} will increase with I_o. Therefore, the subthreshold current becomes a positive factor for driving wires. In other words, a transistor with low-V_{th} is more suitable for driving wires than for storing data. In contrast, high-V_{th} transistors are suitable for storing data.

2.2 Side Effects of Low-V_{th}

In addition to the increased leakage current when low-V_{th} transistors are used, other side effects are also produced.

Temperature Coefficient The reduction in the threshold voltage leads to an increase in the temperature coefficient according to the following equation.

$$TCV_{\text{th}} = \frac{1}{V_{\text{th}}} \cdot \frac{\partial V_{\text{th}}}{\partial T}, \tag{6}$$

where TCV_{th} is the temperature coefficient and T, the temperature.

Output Impedance of Drain The impedance looking into the drain of an MOS is given by the following equation.

$$r_o^{-1} = \frac{\partial i_D}{\partial v_{DS}} \propto (V_{GS} - V_{\text{th}})^2 \cdot \lambda, \tag{7}$$

where r_o is the output impedance, i_D and v_{DS} are the AC portions of the signals of the drain current and the voltage drop across the channel, respectively, and λ is the channel modulation factor. Therefore, the reduction in the threshold voltage leads to an increase

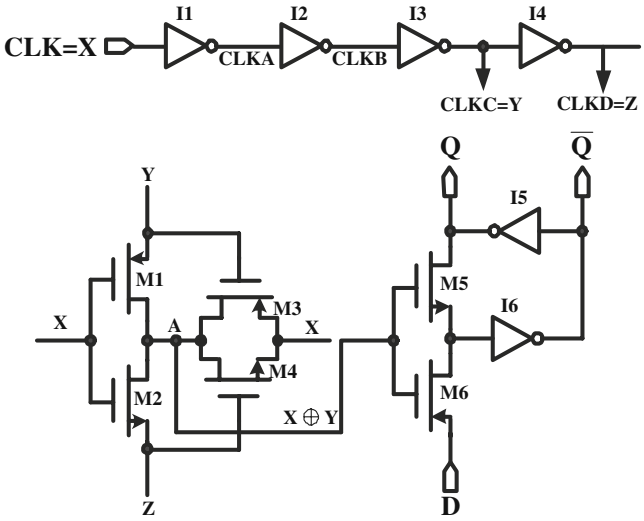

Figure 1 Single-latch DETFF described in [4].

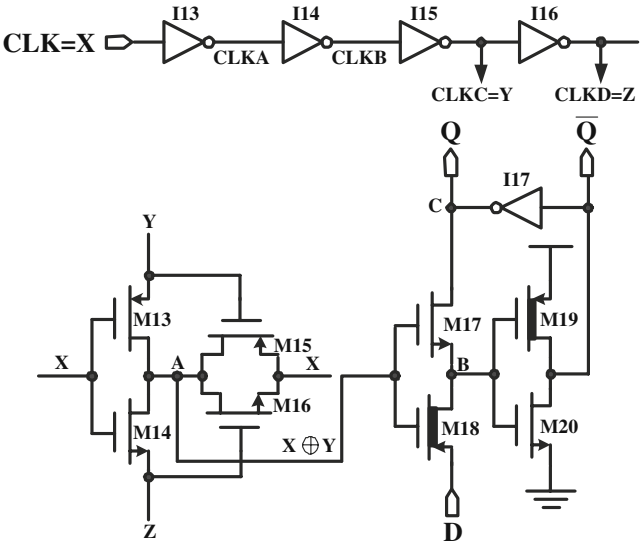

Figure 3 Proposed energy-efficient DETFF.

in the output impedance at the drain. In other words, it is difficult to flip the state at the drain.

2.3 Schematic of Proposed DETFF

Figure 1 shows the single-latch DETFF described in [4], and Fig. 2 shows the modified version of the single-latch DETFF proposed in [7]. The only difference between the two is that in the latter, all of the transistors are replaced with low-V_{th} transistors except for the two inverters on the right-hand side. Although the simulation results reported in [7] showed that there was an improvement in terms of power dissipation, the area penalty is very high. According to the characteristics listed in Table 1, the area overhead will be roughly 55.26%, which is impractical. In addition, the increased output impedance at these output nodes makes it difficult for the back-to-back inverter pairs to flip states if necessary, according to the analysis in the previous section. Consequently, the operating speed will be reduced.

A simple method to improve the single-latch DETFF is shown in Fig. 3. M13 to M16 are XOR gates that are used to detect the edge transitions generated in the inverters I13 to I16. Therefore, this combination acts as an edge detector and generator, which is not critical to the state transitions at D and Q. It is not necessary to suffer the large area penalty and high leakage current by using low-V_{th} transistors to construct such an XOR gate.

Selection of M18 Notably, the input, D, is present at the source of PMOS M18, while we expect that the

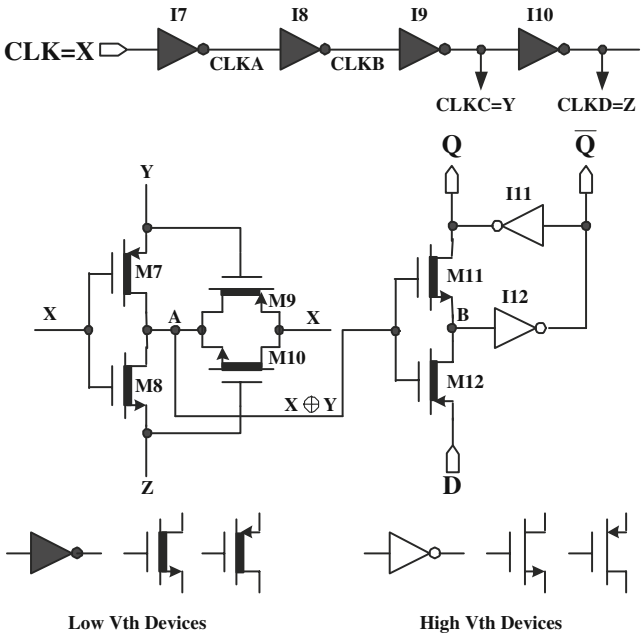

Figure 2 Single-latch DETFF described in [7].

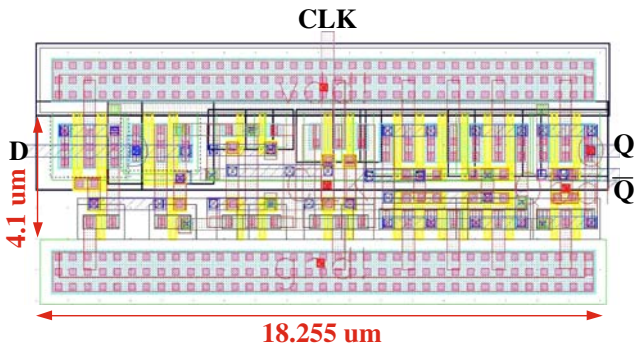

Figure 4 Layout of proposed DETFF cell.

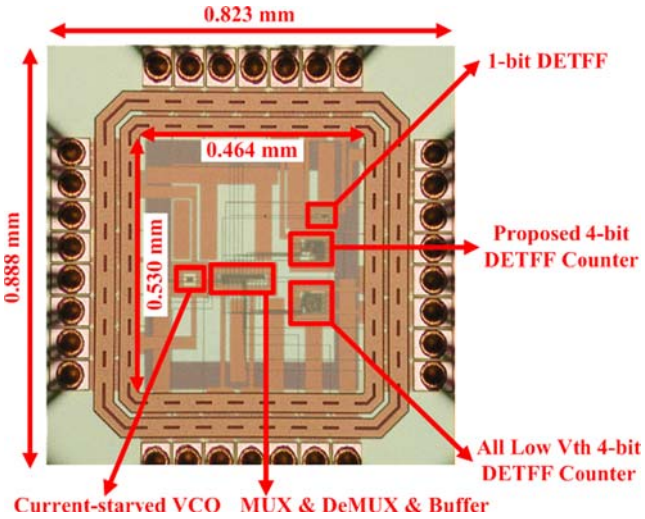

Figure 5 Die photo of prototypical chip using proposed DETFF.

state of node B will follow the input D given the fact that the XOR result at the gate drive of M18 is pulled low. Because D is at the source of M18 and B is at M18's drain, M18 is physically a common-gate amplifier formation whose gain is proportional to gm_{M18}, the transconductance of M18. gm_{M18} is directly proportional to $(V_{GS} - V_{\text{th}})$. Therefore, a low-V_{th} transistor is a better solution to obtain speed and power at the expense of area.

Selection of M17 The output, Q, resides at the drain of M17. In order to make it easy for I17 to flip the state of Q, its load should be small. Therefore, using a low-V_{th} transistor will be a bad solution based upon the conclusion given by Eq. 7. Therefore, we propose the use of a normal NMOS transistor rather than a low-V_{th} one.

Selection of M19 and M20 Basically, M19 and M20 constitute an inverter to drive I17. However, the input of this inverter, i.e., node B, is the output of another

Figure 6 One DETFF operates with 10 MHz clock.

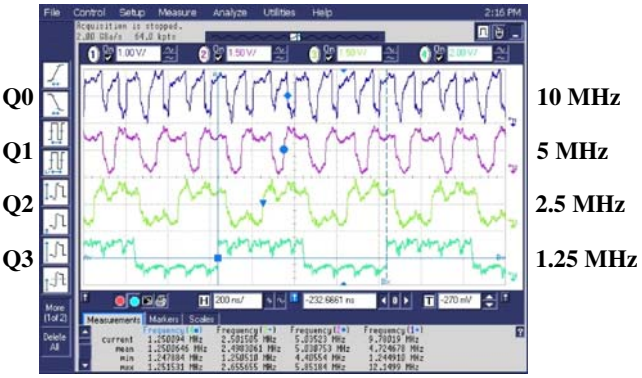

Figure 7 4-bit DETFF counter operates with a 10 MHz clock.

inverter composed of M17 and M18. Notably, the inverter composed of M17 and M18 is a "floating" inverter where there is no path to either VDD or GND. Therefore, node B becomes a "weak" output to drive the inverter composed of M19 and M20, where M19 is the current source and M20 is the current sink. If M19 is a high-V_{th} transistor, it will suffer from the problem of having to supply a large current to drive I17 in addition to the fact that the "weak" node B cannot easily switch it on. As a consequence, the slew rate (SR = $\frac{\partial V}{\partial t} = \frac{I}{C_L}$) at $\overline{Q}$ deteriorates. Hence, M19 should be a low-V_{th} transistor.

In other words, the proposed DETFF only utilizes two low-V_{th} transistors at M18 and M19. The overall area penalty is then reduced to merely 11% at most [15].

3 Implementation and Measurement

TSMC (Taiwan Semiconductor Manufacturing Company) 0.18-μm 1P6M CMOS process is adopted to design the proposed DETFF. The layout of the proposed DETFF cell is shown in Fig. 4; the cell has an area of 4.1 × 18.255 μm^2. A photo of the die photo of a prototypical chip design is shown in Fig. 5. It has an area of 823 × 888 μm^2 and it includes pads, two 4-bit registers composed of the proposed DETFFs, a build-in current-starved VCO, a loadable up/down

Table 2 Performance comparison with previous works.

	[4]	[8]	[7]	[11]	Ours
Rise delay (ps)	503	381	410	169	375
Fall delay (ps)	765	430	420	170	345
Power (μW)	66.3	90.9	47.8	154	31.7
P×D (fJ)	50.5	39.0	19.6	260.3	11.9
Years	2001	1997	2004	2007	2009

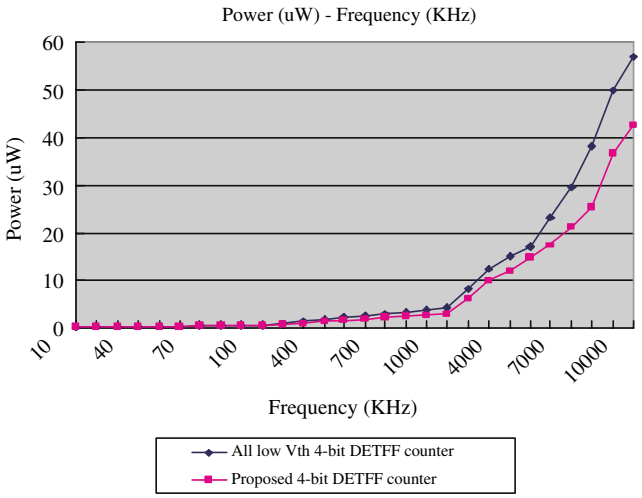

Figure 8 Comparison with proposed design and previous work [7].

counter also composed of the proposed DETFFs, and a MUX. Figure 6 shows the 1-bit DETFF operating with a 10 MHz clock. Figure 7 shows the proposed 4-bit DETFF counter operating with a 10 MHz clock to justify that the DETFF-based registers are operating correctly. A performance comparison of the proposed design with several previous DETFFs is summarized in Table 2. Although the proposed design has a chip area that is increased 11%, it dissipates the least energy and consumes the least power. Our design saves at least 33% power and 39% energy. Figure 8 shows the comparison with the proposed 4-bit DETFF counter and all low-V_{th} 4-bit DETFF counter [7]. It is observed that our design can save more power when the clock rate increases further.

4 Conclusion

In this work, we have proposed an energy-efficient DETFF design to realize low power consumption. A detailed circuit analysis help determine which transistors should be replaced with low-V_{th} ones and which transistors should be replaced with normal ones. The measurement results justify our analysis.

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