0.9 V to 5 V Bidirectional Mixed-Voltage I/O Buffer with an ESD Protection Output Stage

Chua-Chin Wang†, *Senior Member, IEEE*, Ron-Chi Kuo, and Jen-Wei Liu

***Abstract*—A 0.9 V to 5 V (0.9/1.2/1.8/2.5/3.3/5 V) mixed-voltage I/O buffer with NMOS clamping technique is proposed. By using a dynamic gate bias generator to provide appropriate gate drive voltages for the output stage, the I/O buffer can transmit sub-3×VDD voltage level signal without gate-oxide overstress hazard. Besides, the leakage current is eliminated by adopting a floating N-well circuit. The maximum data rate are all measured to 66 MHz for 5/3.3/2.5/1.8/1.2/0.9 V with an equivalent probe capacitive load of 10 pF.**

***Index Terms*—mixed-voltage-tolerant, I/O buffer, floating N-well circuit, gate-oxide reliability**

I. Introduction

With the fast development of CMOS technology, the supply voltage of integrated circuits (IC) is drastically scaled down to reduce power consumption [1]. When chips using different processes and supply voltages are integrated in a PCB-based system, such as in a PCI interface, conventional I/O buffers are not adequate to communicate due to the problems of gate-oxide reliability, hot carrier degradation, and the undesired leakage current path [2]. In past years, many mixed-voltage I/O buffers were reported to deal with the chip interface problems of different voltage levels [1]−[4], [6]. However, most of them can only transmit and receive the signal with the voltage from VDD to 2×VDD [1]-[4]. The compatibility with more advanced processes has been ignored. Therefore, a wide range I/O buffer able to simultaneously transmit and receive signal from $\frac{1}{2}$×VDD to sub-3×VDD is deemed as a total solution for these scenarios. To communicate the signal at sub-3×VDD, triple stacked transistors are used in the output stage to avoid the gate-oxide overstress. Notably, traditional gate-tracking circuit and floating N-well circuit can not be used directly due to the high voltage signal which is very close to 3×VDD [2], [4]. A protection voltage equal to VDDH−VDD (3.2 V) is required to ensure the gate-oxide reliability. The NMOS clamping technique without any power-consuming DC current path is employed to generate this protection voltage. Besides, the current drive capability with ESD protection is also proposed in this work.

II. 0.9 V to 5 V Mixed-Voltage I/O Buffer

Fig. 1 shows the block diagram of the proposed I/O buffer consisting a Pre-driver, an Input stage, an Output Stage, a Dynamic Gate Bias Generator, a Floating N-well Circuit, and a V_{PAD} Detector.

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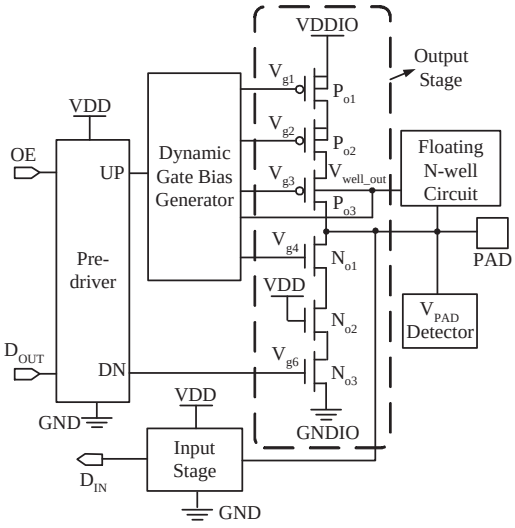


Fig. 1. Block diagram of the proposed mixed-voltage I/O buffer.

A. Output Stage

Since the supply voltage (VDD) of the core circuits is 1.8 V in 0.18 μm CMOS process, the output stage must be realized with three stacked PMOS and NMOS transistors, respectively, for 2×VDD<5 V<3×VDD, as depicted in Fig. 1. Besides, appropriate gate voltages are needed for P_{o1}∼P_{o3} and N_{o1}∼N_{o3} to ensure the gate-oxide reliability and correct functions. The detailed operation of output stage is tabulated in Table I.

B. Pre-driver

The Pre-driver is a simple logic circuit to decode and pre-drive. When the voltage of control signal OE is at 1.8 V, the I/O buffer operates in the transmitting (TX) mode. The logic state of V_{PAD} is determined by D_{OUT}. On the other hand, when the I/O buffer is in the receiving (RX) mode, OE is 0 V.

C. Input Stage

As shown in Fig. 2, MN604 and MN605 are added to prevent MP602 and MN601 from gate-oxide overstress. MP605 is used to clamp V_{i1} at 1.8 V when logic 1 is received. MP601 and MN602 are turned off as well as MP604 is turned on to reduce power dissipation in the TX mode.

D. Dynamic Gate Bias Generator

The dynamic gate bias generator is composed of a VDDIO Detector, V_{g1}, V_{g2}, V_{g3}, and V_{g4} generators. The details of each subcircuit will be analyzed in the following text.

TABLE I
GATE VOLTAGES OF THE OUTPUT STAGE

	VDDIO (V)	V_{g1} (V)	V_{g2} (V)	V_{g3} (V)	V_{g4} (V)
RX	5	5	>3.2	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
	3.3	3.3	3.3	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
	2.5	2.5	2.5	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
	1.8	1.8	1.8	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
	1.2	1.2	1.8	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
	0.9	0.9	1.8	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
TX	5	>3.2/5	>3.2	>3.2/1.8	>3.2/1.8
	3.3	>1.5/3.3	>1.5	>1.5	1.8
	2.5	>0.7/2.5	>0.7	>0.7	1.8
	1.8	0/1.8	0	0	1.8
	1.2	0/1.2	0	0	1.8
	0.9	0/0.9	0	0	1.8

[a] Only when $V_{PAD} = 5$ V, $V_{g3} = V_{PAD}$.
[b] Only when $V_{PAD} = 5$ V, $V_{g4} > 3.2$ V.
[c] In RX or TX, V_{well_out} =$1.8/V_{PAD}$, and V_{g5} =1.8 V
[d] In RX, V_{g6} =0 V; in TX, V_{g6} =0/1.8 V.

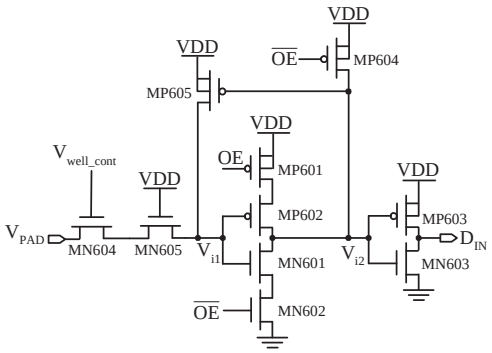


Fig. 2. Input stage circuit.

1) Bias Circuit and V_{PAD} Detector: Referring to Fig. 3, the bias circuit and V_{PAD} Detector are both realized with a string of diode-connected PMOS transistors. The summation of the threshold voltages of the PMOS must be larger than VDDIO and V_{PAD}, respectively, such that the transistors would be operated in the sub-threshold region to reduce the static current.

2) VDDIO Detector: VDDIO Detector is implemented with a string of diode-connected PMOS transistors, four detection circuits, (TR0, TR1, TR2, and TR3), and a thermometer code to one-hot code decoder, as illustrated in Fig. 3. As mentioned previously, the summation of the threshold voltages are larger than VDDIO such that the DC current in the PMOS string is very small. The DC voltages VX1∼VX11 generated by the PMOS string devices are all proportional to VDDIO. VX4, VX5, VX7, VX8, VX10 are fed into TR0∼TR3 for VDDIO detection. Since VX4 and VX5 would be larger than 1.8 V for VDDIO at VDDH, a protection transistor NMOS should be inserted at the gate of PMOS in TR0 and TR1. Through simple glue logic gates, the thermometer code VD0∼VD3 could be easily converted into the one-hot code VD50, VD33, VD25, and VD18. The thermometer code VD0∼VD3 can be obtained according to various VDDIOs.

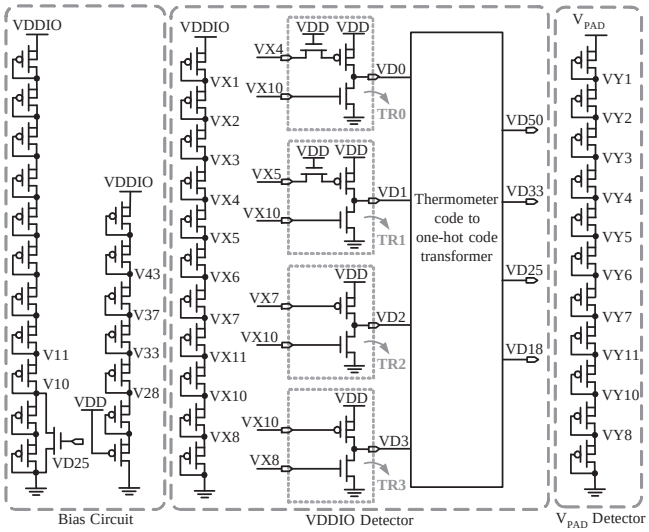


Fig. 3. Bias circuit, VDDIO Detector and V_{PAD} Detector.

3) V_{g1} Generator: In Fig. 4, V_{g1} generator comprises a cross-coupled latch and a voltage level converter, which outputs a pair of opposite signals, Q and QB. It is basically composed of two cross-coupled transistors PMOS with two NMOS transistors in series as discharging paths. V_{g1} generator contains three pairs of discharging paths which are respectively controlled by the signals UP50, UPL, UP18, and their complementary signals. When VDDIO is fed with 5 V and MN105 is turned on, QB is discharged to 3.3 V through the first pair of discharging paths (MP103, MN101, MP105, MN103, and MN105) while Q is pulled up to VDDIO. When VDDIO is fed with 3.3/2.5 V, the second pair of discharging paths (MN107∼MN110, MP107, and MP108) is activated, which is controlled by UPL and $\overline{\text{UPL}}$. When VDDIO is fed with 1.8/1.2/0.9 V, the third discharging path (MN111∼MN116) is on. Referring to the logic equations in Fig. 4, any input voltage will appear in only one pair of discharging paths.

4) V_{g2} and V_{g4} Generator: Fig. 5 (a) shows the schematic of V_{g2} generator. MN201 is a clamping NMOS, which can only pass the signal smaller than VX2$-V_{thn}$, where V_{thn} is the threshold voltage of NMOS. When VDDIO is 5 V, OE18 and OE50 are both biased at 1.8 V such that V_{g2} can be biased at 3.2 V (VX2-V_{thn}) through MN202 and MP201 without gate-oxide overstress. MP202 is turned off provided that VX2 is higher than 3.2 V. If VDDIO is lower than 1.8 V in the receiving mode, OE18 and OE50 are all biased at 1.8 V such that MN202 and MP201 are turned off. V_{g2} can be operated at 1.8 V through MP203 and MP203, when VX2 is lower than 1.8 V. Besides, the undesired leakage current caused by the parasitic diodes of MP202 and MP203 can be eliminated by connecting their N-well to a floating N-well circuit comprising MN203, MP204, and MP206.

V_{g4} generator is shown in Fig. 5 (b). It pulls V_{g4} to 3.2 V when V_{PAD} is 5 V and keeps V_{g4} at 1.8 V for $V_{PAD} = 3.3$ V. When V_{PAD} is 5 V, V_{g4} is biased at 3.2 V (VY4 $-V_{thn}$) by the clamping NMOS MN401. When V_{PAD} is biased at 3.3/2.5/1.8/1.2/0.9/0 V, VY4 -V_{thn} is smaller than 1.8 V and blocked by MP401. V_{g4} is then biased at 1.8 V by MP402,

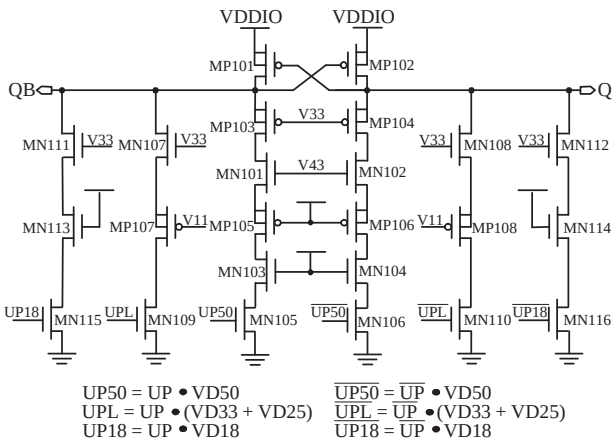


Fig. 4. V_{g1} generator.

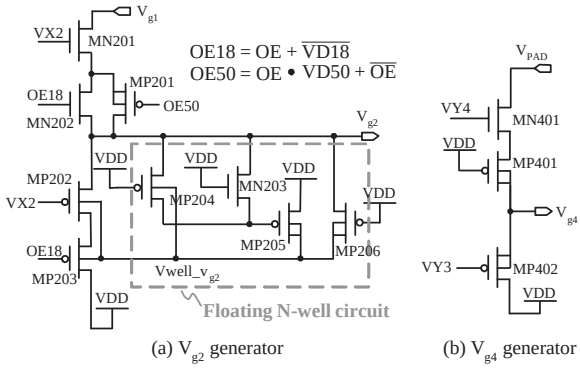


Fig. 5. V_{g2} generator and V_{g4} generator.

because VY3 is lower than 1.8 V.

5) V_{g3} Generator: The proposed V_{g3} generator is depicted in Fig. 6 (a). It can be observed that both $\mathrm{V_{PAD}}$ and V_{g2} are fed into V_{g3} generator. By detecting two signals, VDDIO and OE, a corresponding V_{g3} will be generated. To reduce the power consumption, V_{g3} generator combines the voltage-generating function with the gate-tracking capability in this work. In the receiving mode, when VDDIO is fed with $1.8/1.2/0.9$ V and $\mathrm{V_{PAD}}$ is biased at 5 V, the voltage of V_{neta} and V_{netb} are clamped at 3.2 V for passing $\mathrm{V_{PAD}}$ to V_{g3} to avoid the leakage current problem. Besides, MN301 is turned off by floating N-well circuit $\mathrm{F_2}$ when the voltage of V_{net_bias} is lower than 1.8V. When $\mathrm{V_{PAD}}$ is 0 V, an Edge Detector is adopted to prevent transistor $\mathrm{P_{o3}}$ from gate-oxide overstress. When $\mathrm{V_{PAD}}$ is at 2.5/3.3 V, V_{netb} is generated at 1.8 V by floating N-well circuit F1. Then, $\mathrm{V_{PAD}}$ is passed to MP318 to turn off the output stage $\mathrm{P_{o3}}$. In the transmitting mode, when VDDIO is operated at 5 V, a negative pulse, which is triggered at the negative edge of $\mathrm{D_{OUT}}$, would pulled V_{g3} down to 1.8 V. Thus, the gate-oxide overstress can be avoided. When VDDIO is operated at 1.8/1.2/0.9 V, V_{g2} is biased at 1.8/1.2/0.9 V and MN304 is turned off to protect V_{g3} from any leakage current.

E. Floating N-well Circuit

To avoid the undesired leakage current path through the parasitic diode of $\mathrm{P_{o3}}$, V_{well_out} is varied with different $\mathrm{V_{PAD}}$ by the floating N-well circuit. The proposed floating N-well circuit is composed of two traditional floating N-well cells, FN51 and FN52, as shown in Fig. 6 (b). With the clamping NMOS MN503, FN52 can output the signal V_{well_cont} at max(VY2$-\mathrm{V_{thn}}$, 1.8 V). When $\mathrm{V_{PAD}}$ is operated at 3.3 V, V_{well_cont} is biased at 1.8 V. When $\mathrm{V_{PAD}}$ is 5 V, V_{well_cont} at 3.2 V ($=$ VY2 $-\mathrm{V_{thn}}$) is used as the protection voltage for MP503. On the other hand, FN51 can generate the output signal V_{well_out} = max($\mathrm{V_{PAD}}$, V_{well_cont}).

F. ESD Protection Consideration

In traditional I/O buffers, the parasitic diode of the PMOS in the output stage can provide a discharge path for the ESD current. However, the parasitic diode connected to the I/O PAD and VDDIO does not exist due to the floating n-well circuit in the mixed-voltage-tolerant I/O buffer. Thus, the ESD capability of the mixed-voltage-tolerant I/O buffer is worse than that of traditional I/O buffers given the same size. In order to retain enough ESD capability, the penalty is the large area of NMOS and PMOS in Output stage. From the measurement results of several previous works [1]-[4], the ESD strength of the stacked output stage with their current driving ability higher than 25 mA can be equalized to 2 kV for HBM (human body model) and 200 V for MM (machine model) [5], [6]. Fig. 7 shows the simplified circuit with ESD consideration through discharging path and charging path. $\mathrm{V_{DS,NMOS}}$ and $\mathrm{V_{DS,PMOS}}$ can be derived as follows,

$$\mathrm{V_{DS,PMOS}} = \frac{\mathrm{V_{IL}} - \mathrm{V_{SS}}}{2} \tag{1}$$

$$\mathrm{V_{DS,NMOS}} = \frac{\mathrm{V_{IH}} - \mathrm{V_{SS}}}{2} \tag{2}$$

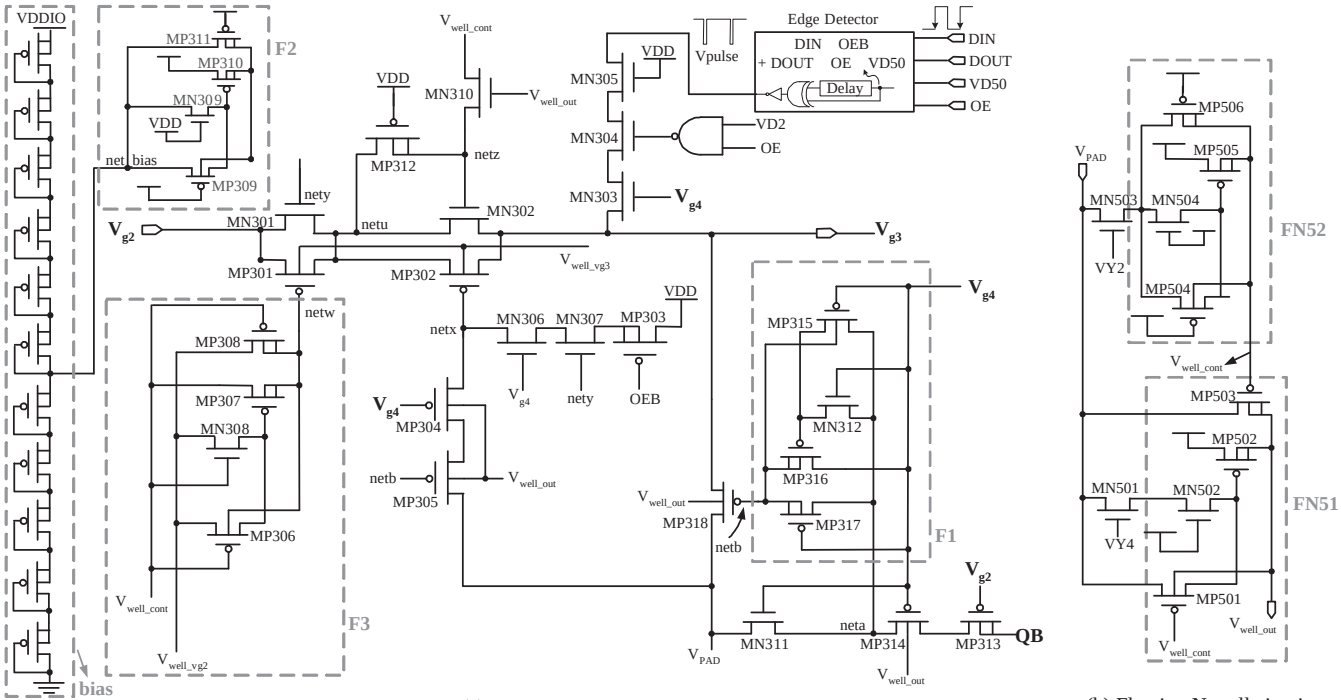
where $\mathrm{V_{IL}}$ and $\mathrm{V_{IH}}$ are set to 0.35×VDD and 0.65×VDD, respectively [5]. Moreover, Output Stage are operated in the triode region. Thus, by taking above conditions and the characteristic of transistors in triode region into consideration, the W/L ratio of PMOS and NMOS in the Output Stage can be determined to be 720 μm/ 180 nm and 180 μm/ 180 nm, respectively.

III. Measurement Results

The proposed design is implemented with a typical 0.18 μm logic CMOS process. Fig. 8 shows the layout and the die photo of the proposed mixed-voltage I/O buffer. Fig. 9 depicts the waveforms of $\mathrm{V_{PAD}}$ and $\mathrm{D_{IN}}$ with different $\mathrm{V_{PAD}}$ voltages in the RX mode, whereas $\mathrm{D_{IN}}$ is recovered at 1.8 V in all cases. The maximum TX data rate with different VDDIOs is measured, as shown in Fig. 10. The mark level of $\mathrm{V_{PAD}}$ is same as the voltage level of VDDIO. Fig. 11 reveals the measured eye diagram of the output signal in the TX mode when VDDIO=5.0 V at 40 MHz and VDDIO=0.9 V at 33 MHz, respectively. The sampling windows are all higher than 18 ns for both TX/RX modes. The performance of the proposed mixed-voltage I/O buffer is summarized in Table II compared with several previous I/O buffers. Table II shows that a wide voltage range, sub-3×VDD, is successfully achieved by this work.

TABLE II
PERFORMANCE CAPARISON OF MIXED-VOLTAGE I/O BUFFER

	Year	Transmitting voltage mode (V)	Process (μm)	Frequency (MHz)	Area (μm$\times\mu$m)
This work	2009	0.9/1.2/1.8/2.5/3.5/5	0.18	66	65×785
[6]	2009	5/3.3/1.8	0.35	60	1328×1126
[1]	2008	1.5/3.3	0.18	266	N/A
[2]	2007	1.2/2.5	0.13	133	107.73×65.38
[3]	2007	1.8/3.3	0.18	200	N/A
[4]	2006	2.5/5	0.25	50	N/A



(a) V_{g3} generator (b) Floating N-well circuit

Fig. 6. V_{g3} generator circuit and the floating N-well circuit.

IV. CONCLUSION

A 0.9 V to 5 V mixed-voltage tolerant I/O buffer is proposed in this paper. The signal from $\frac{1}{2}\times$VDD to sub-3$\times$VDD can be transmitted and received simultaneously. Besides, the effects of gate-oxide overstress and the leakage current are both eliminated.

V. ACKNOWLEDGMENT

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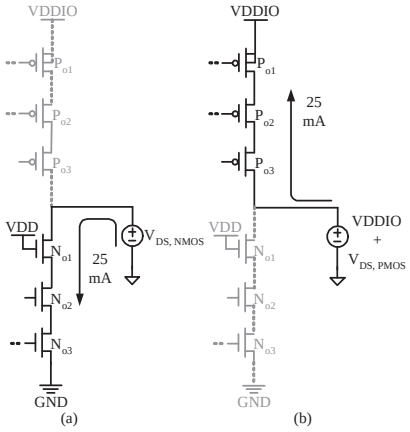

Fig. 7. The simplified circuit of output stage with ESD protection. (a) Discharging path. (b) Charging path.

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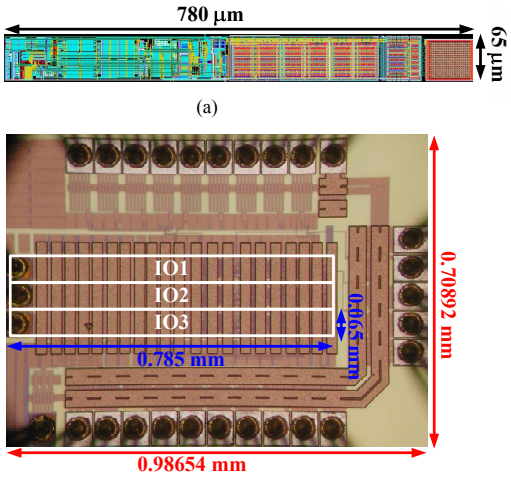

Fig. 8. (a) Layout (b) Die photo of the proposed mixed-voltage I/O buffer.

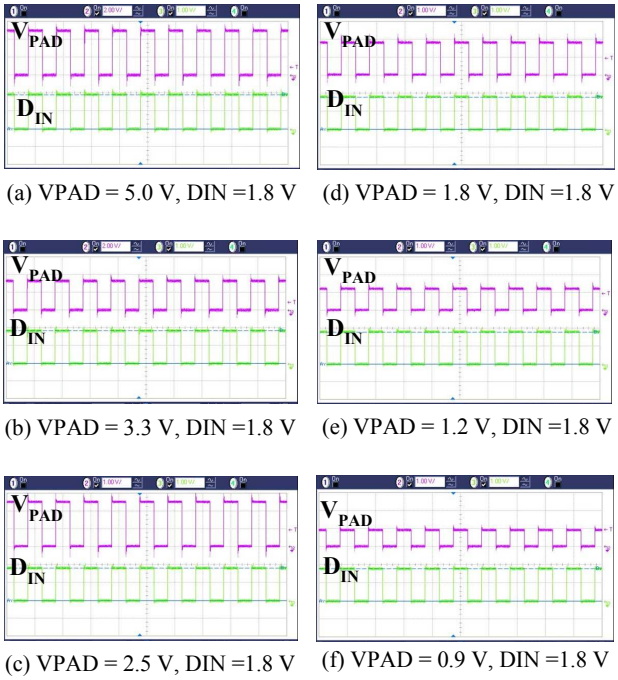

Fig. 9. Measured D_{IN} in the RX mode for different V_{PAD} voltages.

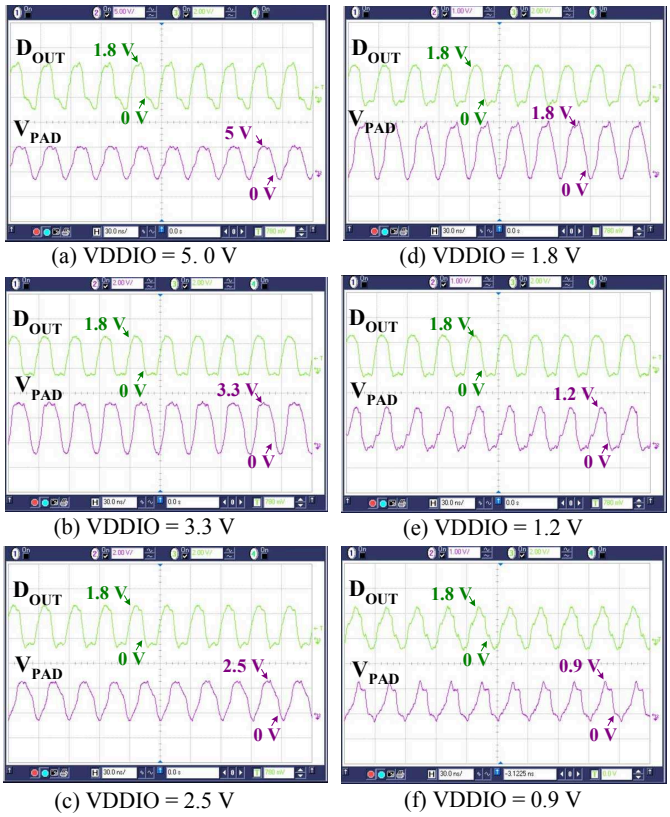

Fig. 10. Measured V_{PAD} at 66 MHz in the TX mode for different VDDIOs.

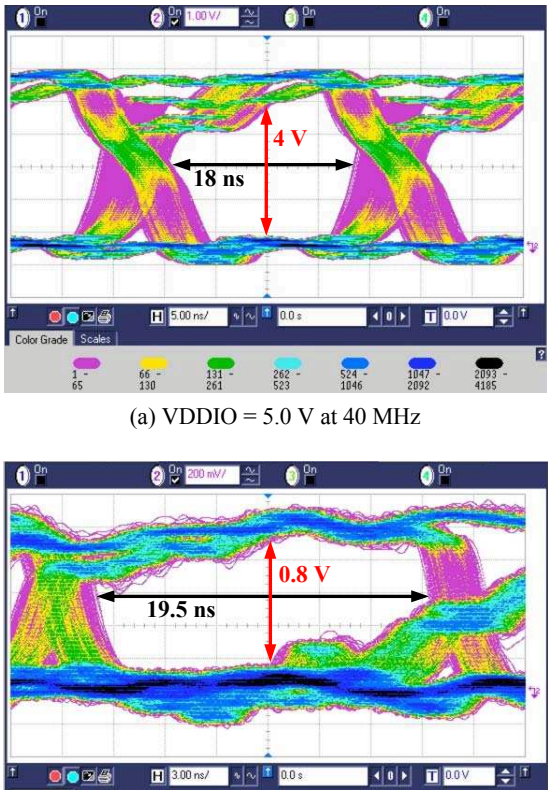

Fig. 11. Measured eye diagrams of the output signal V_{PAD} (a) when VDDIO = 5.0 V at 40 MHz (b) when VDDIO = 0.9 V at 33 MHz.