A $1/2 \times$ VDD to $3 \times$ VDD Bidirectional I/O Buffer With a Dynamic Gate Bias Generator

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***Abstract*—This paper presents a wide-range I/O buffer able to transmit and receive signals of 0.9/1.2/1.8/3.3/5.0 V by using a typical 0.18 μm CMOS process. The Dynamic gate bias circuit in the proposed I/O buffer is composed of two voltage converters, an EOS (Electrical Overstress) protector, and standard logic cells. A High voltage detector detects voltage level of VDDIO and then generates several bias voltages to the Dynamic gate bias circuit. By using the Dynamic gate bias generator to generate appropriate gate drives for the triple-stacked MOS transistors in the Output stage, the gate-oxide overstress and hot-carrier degradation are avoided. A Floating N-well circuit in the proposed I/O buffer is used to remove undesirable leakage current paths. The proposed I/O buffer can operate at 10/40/50/40/10 MHz when VDDIO are biased at 5.0/3.3/1.8/1.2/0.9 V, respectively. The maximum speed is 50 MHz given a 19 pF load. The maximum static power consumption is merely 3.9 μW justified by the measurements on silicon.**

***Index Terms*—Dynamic gate bias, floating N-well, I/O buffer, mixed-voltage tolerant, wide-range.**

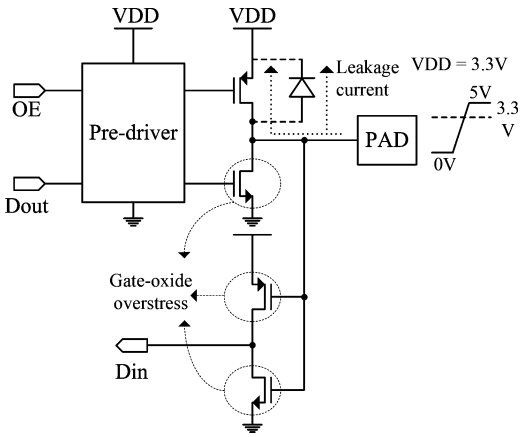

Fig. 1. Traditional I/O buffer.

I. Introduction

With the rapid evolution of CMOS (Complementary Metal-Oxide-Semiconductor) technology, supply voltage and feature size of chips are scaled down to reduce power consumption and area cost. However, the compatibility among chips is an imminent problem when chips with different logic voltage levels are integrated on a PCB (Printed Circuit Board) based system. Conventional I/O buffers are no longer capable of exchanging signals in such a scenario. In Fig. 1, the Output stage of a traditional I/O buffer is typically composed of a pMOS and an NMOS. The normal power supply voltage is 3.3 V. When the input signal at the I/O pad is pulled up to 5.0 V, i.e., $\mathrm{V_{PAD}} = 5.0$ V or VDDH. These I/O buffers then suffer from hazards of gate-oxide overstress, hot-carrier degradation, and the undesirable leakage current paths [1], [2]. The gate-oxide overstress might cause the gate-oxide breakdown to make the chip fail. The overstress problem will be accumulated if the applied voltage is beyond the tolerant voltage of MOS for a long time [3], [4]. Though the thin oxide process can resolve the problem when the gate is biased at a high voltage, the thin oxide may cause the dielectric breakdown or tunneling effect. It then will lead to a permanent damage, when the electric field across the thin gate oxide is too large [2].

Many prior studies were proposed to resolve these problems, namely, mixed-voltage-tolerant I/O buffers. They basically employed a Floating N-well circuit and a Gate-tracking circuit [5]–[7], as shown in Fig. 2. The stacked-NMOS structure [8], [9] can avoid the hot-carrier degradation, which can even operate at a voltage up to 60 V using a standard CMOS technology. Moreover, the stacked-NMOS structure was also reported to avoid the gate-oxide overstress [10]. The main idea of the stacked MOS structure is to bias the gates of the Output stage MOS transistors and share the voltage drop to avoid the high voltage stress. The bias voltage constraining the MOS's $|\mathrm{Vgs}|$ and $|\mathrm{Vdg}|$ is biased at VDD. Therefore, the gate-oxide overstress is avoided. To eliminate the leakage current path through the pMOS at Output stage of the conventional I/O buffer when $\mathrm{V_{PAD}}$ is VDDH, the Gate-tracking circuit provides an appropriate voltage level to the gate drive of pMOS at the Output stage. In the receiving mode (Rx), the Floating N-well circuit generates VDDH to the N-well of output pMOS when $\mathrm{V_{PAD}}$ is biased at VDDH. Thanks to the Floating N-well circuit, the leakage current path of the parasitic diode is eliminated, because it can not be turned on [11]. Priorly proposed I/O buffers have been proved to receive $3 \times$ VDD signal by using an NMOS-blocking technique [6], [12], [13]. By using the NMOS-blocking method, the I/O buffers can receive a higher voltage level signal at the PAD without any hazard. However, the applications are drastically limited because these I/O buffers can not transmit the signals with a higher level in the transmitting mode (Tx). Figs. 3–5 show the reasons why. Referring to Fig. 3, the Gate-tracking circuit can not provide a VDDH to turn off the output pMOS to generate logic 0 in Rx

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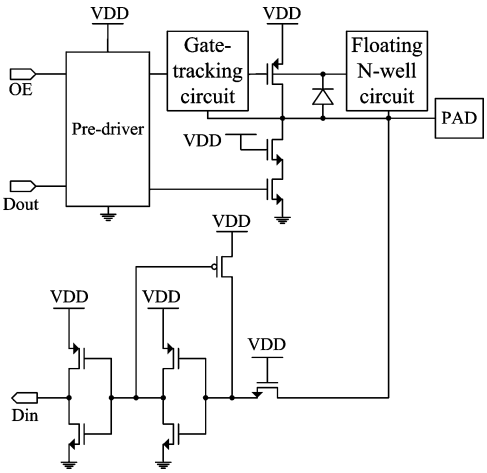

Fig. 2. Schematic of the typical mixed-mode-tolerant I/O buffer.

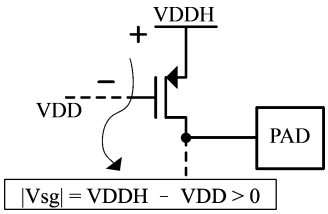

Fig. 3. Output pMOS should be turned off.

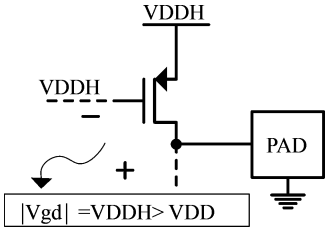

Fig. 4. V_{PAD} is biased at 0 V.

or Tx. Referring to Fig. 4, even though the gate of pMOS is pulled up to VDDH, the V_{gs} of pMOS is larger than VDD when V_{PAD} is equal to logic 0. It will jeopardize the transistor. Finally, referring to Fig. 5, assume VDDH is transmitted. The V_g and V_s of the output pMOS are biased at 0 V and VDDH, respectively. The V_{sg} is equal to VDDH, which causes the gate-oxide overstress problem. Therefore, a bias circuit is required to generate the desired gate voltage to avoid the gate-oxide overstress. The charge redistribution topologies and the diode-connected MOS were employed to generate the desired bias voltages [14]. However, the complexity of this approach is a high price to pay, since several additional control signals are needed to determine the operation stage. Nevertheless, the hot-carrier problem can be resolved by adding the Gate-tracking circuit [15]. A decoupling technology was also proposed to reduce coupling on biases when VDDIO is switching [16]. Negative Bias Temperature Instability (NBTI) is also a reliability concern for the CMOS technology [17]. It causes a device degradation of the surface channel P-channel MOSFETs (metal-oxide-silicon

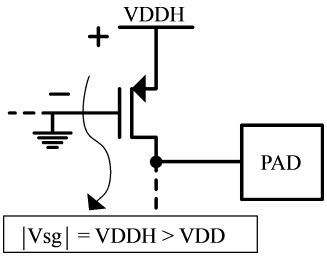

Fig. 5. Output pMOS should be turned on.

field-effect transistors) such that it has become a limiting factor for the lifetime of CMOS.

This paper proposes a fully wide-range I/O buffer which is implemented using a typical CMOS $0.18\ \mu$m process. Notably, a novel Dynamic gate bias generator is employed in the proposed I/O buffer, which is different from conventional voltage dividers [18]. The Dynamic gate bias generator circuit generates appropriate gate drives to the transistors of output PMOSs. The proposed design is proved on silicon to transmit and receive the signals with voltage levels of 0.9/1.2/1.8/3.3/5.0 V, i.e., $1/2 \times$ VDD $\sim 3 \times$ VDD. Moreover, the proposed I/O buffer does not need thick-oxide devices such that the fabrication cost is reduced.

II. $1/2 \times \mathrm{Vdd} \sim 3 \times \mathrm{Vdd}$ Bidirectional I/O Buffer

The block diagram of the proposed wide-range I/O buffer is shown in Fig. 6. It is composed of a Pre-driver, a Dynamic gate bias generator, a High voltage detector, a PAD voltage detector, an Output stage, a Floating N-well circuit, a Gate-tracking circuit, and an Input stage. Notably, VDDIO stands for the signal voltage level to be transmitted and received.

Stacked pMOS transistors, i.e., MP1, MP2, MP3, are employed at the Output stage to eliminate the gate-oxide overstress, as shown in Fig. 6. By applying proper the gate drives on the Output stage MOSs, the gate-oxide overstress can be avoided. Dynamic gate bias generator is in charge of generating these required gate drives for Output stage MOSs. The details of these sub-circuits are disclosed in the following text.

A. Pre-Driver

Pre-driver is a digital CMOS logic circuit, as shown in Fig. 7. OE determines which of the transmitting mode $(\mathrm{OE} = 1.8\ \mathrm{V})$ or receiving mode $(\mathrm{OE} = 0\ \mathrm{V})$ is selected. Dout is an input from internal circuitry. UP is an output signal to enable the Dynamic gate bias generator. DN is an output signal which is coupled with MN3 in Fig. 6. Table I shows the truth table of Pre-driver circuit.

Tx : When $\mathrm{Dout} = 0$ is transmitted, UP becomes 1 to enable Dynamic gate bias generator circuit to generate a bias voltage, Vmp1, which turns off the Output stage's MP1. Simultaneously, MN3 is turned on by $\mathrm{DN} = \mathrm{logic}\ 1$. On the contrary, when $\mathrm{Dout} = 1$ is transmitted, Dynamic gate bias generator circuit generates bias voltages, i.e., Vmp1, Vmp2, Vmp3, to turn on the corresponding pMOS transistors of the Output stage. MN3 is turned off at the same time.

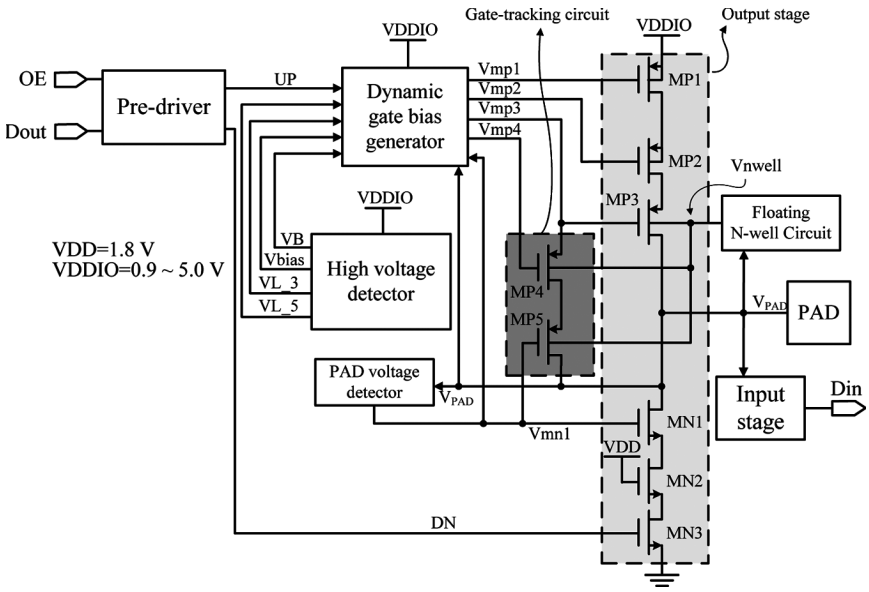

Fig. 6. Schematic of the proposed wide-range I/O buffer.

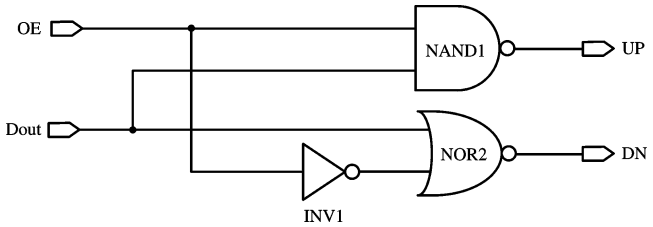

Fig. 7. Schematic of Pre-driver circuit.

TABLE I
TRUTH TABLE OF THE PRE-DRIVER CIRCUIT

	Input		Output	
	OE	Dout	UP	DN
Receiving Mode	0	×	1	0
Transmitting Mode	1 1	0 1	1 0	1 0

Rx : The signal Dout is irrelevant. The Output stage is shut off.

B. Dynamic Gate Bias Generator

The gate drives of MP1, MP2, and MP3, as shown in Fig. 6. These gate drive voltages must be biased at individually appropriate voltage levels to ensure the gate-oxide reliability in different scenarios, which are described as follows.

Tx : When transmitting logic 0 ($\mathrm{UP} = 1.8$ V), MP1 must be turned off, where Vmp1 should be biased at 0.9/1.2/1.8/3.3/5.0 V for $\mathrm{VDDIO} = 0.9/1.2/1.8/3.3/5.0$ V, respectively. At the same time, Vmp2 is set to 1.8/1.8/1.8/1.8/3.3 V, respectively, to turn off MP2 such that the hot-carrier effect on the Output stage is prevented. Vmp3 is equal to 1.8 V in this scenario.

When transmitting logic 1 ($\mathrm{UP} = 0$ V), MP1 must be turned on with no gate-oxide overstress. Therefore, if $\mathrm{VDDIO} = 0.9/1.2/1.8/3.3/5.0$ V, Vmp1, Vmp2, Vmp3 must be set to 0/0/0/1.8/3.3 V, respectively, to prevent such a hazard.

In short, to avoid the hot carrier effect, the gate-source voltage should not be operated in the linear region for a long time. Therefore, Vgs and Vds must be biased at VDD or 0 V. Vmp2 of the Output stage is then must be exactly biased at a predefined voltage to avoid the hot carrier effect.

Rx : If $\mathrm{VDDIO} = 0.9/1.2/1.8/3.3/5.0$ V, then we conclude that $\mathrm{Vmp1} = 0.9/1.2/1.8/3.3/5.0$ and $\mathrm{Vmp2} = 1.8/1.8/1.8/1.8/3.3$ V, respectively. To avoid any leakage current path through MP1, MP2 and MP3, Vmp3 will be biased at 5.0/3.3 V when $\mathrm{VDDIO} = 5.0/3.3$ V, respectively.

Therefore, Table II summarizes the functional table of Dynamic gate bias generator of all the scenarios in the above. Dynamic gate bias generator is in charge of generating all of the required bias voltages, i.e., Vmp1, Vmp2, Vmp3, etc. However, these bias voltages depend on VDDIO and Tx/Rx modes. Dynamic gate bias generator is realized by two level converters (VLC1 and VLC23), an electrical overstress (EOS) protector, and digital logic gates, as shown in Fig. 8.

Notably, a High voltage detector, which will be described later in following text, detects the voltage level of VDDIO and generates a pair of digital signals, VL_3 and VL_5, and two biases, VB and Vbias, to Dynamic bias generator. The details of VLC23, EOS protector, and VLC1, are given as follows.

1) VLC23: Referring to Fig. 9, VDDIO_VLC voltage depends on VDDIO. When $\mathrm{VDDIO} = 5$ V, MP206 is turned on and then VDDIO_VLC will be biased at 3.3 V ($= \mathrm{VB} - \mathrm{V_{TH\_MN214}}$), where VB is a bias generated by High voltage detector which will be described later, and $\mathrm{V_{TH\_MN214}}$ is the threshold voltage of MN214. Therefore, VDDIO turns off MP207 via MN214 and MP208. When $\mathrm{VDDIO} = 0.9/1.2/1.8/3.3$ V and $\mathrm{VL\_5} = 1.8$ V, MN216 is turned on. The gate drive of MP207 will be biased at 0 V, and then $\mathrm{VDDIO\_VLC} = 1.8$ V.

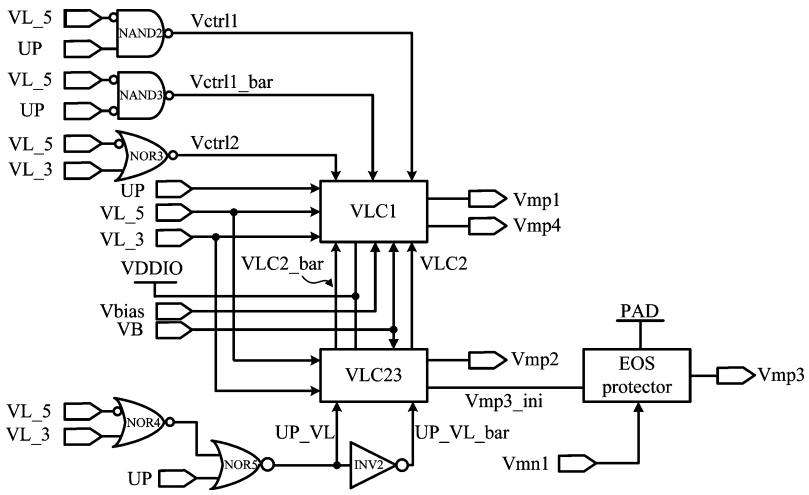

Fig. 8. Schematic of Dynamic gate bias generator.

TABLE II
FUNCTIONAL TABLE OF THE DYNAMIC GATE BIAS GENERATOR

Input				Output				Input	Output				
	OE = 1.8 V							OE = 0 V, UP = 1.8 V					
VDDIO	UP	VL_5	VL_3	Vmp1	Vmp2	Vmp3	Vmp4	PAD	Vmp1	Vmp2	Vmp3	Vmp4	Vmn1
5.0 V	0 V	0 V	0 V	3.3 V	3.3 V	3.3 V	5.0 V	0 V	5.0 V	3.3 V	1.8 V	3.3 V	1.8 V
	1.8 V	0 V	0 V	5.0 V	3.3 V	1.8 V	3.3 V	5.0 V	5.0 V	3.3 V	5.0 V	3.3 V	3.3 V
3.3 V	0 V	1.8 V	0 V	1.8 V	1.8 V	1.8 V	3.3 V	0 V	3.3 V	1.8 V	1.8 V	1.8 V	1.8 V
	1.8 V	1.8 V	0 V	3.3 V	1.8 V	1.8 V	1.8 V	3.3 V	3.3 V	1.8 V	3.3 V	1.8 V	2.2 V
1.8 V	0 V	1.8 V	1.8 V	0 V	0 V	0 V	1.8 V	0 V	1.8 V	1.8 V	1.8 V	0 V	1.8 V
	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	0 V	1.8 V	1.8 V	1.8 V	1.8 V	0 V	1.8 V
1.2 V	0 V	1.8 V	1.8 V	0 V	0 V	0 V	1.2 V	0 V	1.2 V	1.8 V	1.8 V	0 V	1.8 V
	1.8 V	1.8 V	1.8 V	1.2 V	1.8 V	1.8 V	0 V	1.2 V	1.2 V	1.8 V	1.8 V	0 V	1.8 V
0.9 V	0 V	1.8 V	1.8 V	0 V	0 V	0 V	0 V	0 V	0.9 V	1.8 V	1.8 V	0 V	1.8 V
	1.8 V	1.8 V	1.8 V	0.9 V	1.8 V	1.8 V	0 V	0.9 V	0.9 V	1.8 V	1.8 V	0 V	1.8 V

- When $\mathrm{VDDIO} = 5\ \mathrm{V}$, $\mathrm{UP} = 0\ \mathrm{V}$ and if $\mathrm{UP\_VL} = 1.8\ \mathrm{V}$, MN205 is turned off because $\mathrm{VL\_5} = 0\ \mathrm{V}$ as shown in Table II. Vmp3_bar is discharged through MP204, MN210, and MN212, which causes MP201 to be turned on, and $\mathrm{Vmp3\_ini} = \mathrm{VLC2} = 3.3\ \mathrm{V}$. When $\mathrm{Vmp3\_ini} = 3.3\ \mathrm{V}$, MN202 will be turned on, and Vmp3_bar is pulled up to 1.8 V. Simultaneously, Vmp2 will be pulled to 3.3 V by MN217 and MP209. VLC2_bar is pulled down to 0 V by MN212 and MN210.
- On the other hand, when $\mathrm{UP} = 1.8\ \mathrm{V}$ and $\mathrm{UP\_VL} = 0\ \mathrm{V}$, Vmp3_ini will be drawn to 1.8 V. Vmp3_bar will be pulled to 3.3 V. So is VLC2_bar. Vmp2 will be pulled to 3.3 V, and VLC2 will be pulled down to 0 V. Because the gate drive of MP205 is 3.3 V, which is larger than its drain to source voltage drop, MP205 is turned off to isolate Vmp1 and Vmp2.
- When $\mathrm{VDDIO} = 3.3\ \mathrm{V}$, $\mathrm{VL\_5} = 1.8\ \mathrm{V}$, and $\mathrm{UP\_VL} = 0\ \mathrm{V}$. Vmp3_bar is pulled down to 0 through MN204, MN206 and MN208 such that $\mathrm{VDDIO\_VLC} = 1.8\ \mathrm{V}$. Vmp3_ini is pulled up to 1.8 V through MP201. Vmp2 is also 1.8 V. MP201 is turned off.
- When $\mathrm{VDDIO} = 1.8/1.2/0.9\ \mathrm{V}$ and $\mathrm{UP} = 0\ \mathrm{V}$, $\mathrm{UP\_VL} = 1.8\ \mathrm{V}$, Vmp3_ini is pulled down to 0 through MN203, MN205 and MN207. Therefore, MP202 is turned on, and VDDIO_VLC will be 1.8 V. Vmp3_bar becomes 1.8 V and Vmp2 is 0 V. When $\mathrm{UP} = 1.8\ \mathrm{V}$, UP_VL is biased at 0 V, $\mathrm{Vmp3\_bar} = 0\ \mathrm{V}$, Vmp3_ini will be pulled to 1.8 V through MP201 and Vmp2 will be pulled to 1.8 V via MP205. Because VL_5 is equal to 1.8 V, MP210 is turned off.

In short, the mentioned biases in all of the above different scenarios of VLC23 are tabulated in Table III.

2) EOS: EOS (Electrical Overstress) protector circuit is shown in Fig. 10.

- In Tx mode, when $\mathrm{VDDIO} = 5\ \mathrm{V}$, $\mathrm{OE} = 1.8\ \mathrm{V}$, $\mathrm{VL\_5} = 0\ \mathrm{V}$, the complementary of UP will appear at the output of the low-left OR gate and pass through the transmission gate composed of MP7 and MN7. Therefore, the source of MN8 is equal to the complementary of UP. Meanwhile, MN8 is turned on by VDD, and MN6 is turned on by Vmn1 because $\mathrm{Vmn1} = 3.3\ \mathrm{V}$ given $\mathrm{VDDIO} = 5\ \mathrm{V}$ at PAD which will be explained in the "PAD voltage detector" section. In short, the gate drive of MP5 (Vgate1) and MP4 (Vgate2) are equal to complementary of UP. MP5 and MP4 are turned on, $\mathrm{Vmp3} = \mathrm{Vmp3\_ini}$. It is the bias to MP3 in Fig. 6 without gate-oxide overstress. When $\mathrm{VDDIO} = 3.3/1.8/1.2/0.9\ \mathrm{V}$, $\mathrm{OE} = 1.8$, and $\mathrm{VL\_5} = 1.8\ \mathrm{V}$, Vgate1 and Vgate2 are biased at 0 V. MP4 and MP5 will be turned on, and then $\mathrm{Vmp3} = \mathrm{Vmp3\_ini}$.
- In Rx mode, $\mathrm{OE} = 0\ \mathrm{V}$, MN7 and MP7 are turned off, Vgate1 and Vgate2 are biased at $\mathrm{V_{PAD}}$. Notably, Vmn1 provided by PAD voltage detector then would be biased at 3.3/2 V for $\mathrm{V_{PAD}} = 5.0/3.3\ \mathrm{V}$, respectively. Vmp3 will be

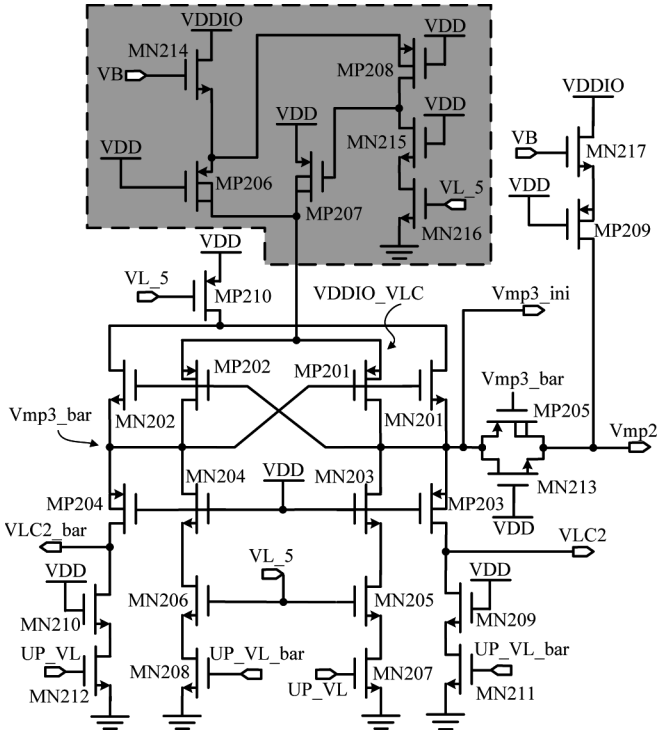

Fig. 9. Schematic of VLC23.

TABLE III
FUNCTIONAL TABLE OF VLC23

Output	Input		
	VDDIO	when V_{PAD} is logic 0	when V_{PAD} is logic 1
Vmp2	5.0 V	3.3 V	3.3 V
	3.3 V	1.8 V	1.8 V
	1.8 V	1.8 V	0 V
	1.2 V	1.8 V	0 V
	0.9 V	1.8 V	0 V
Vmp3_ini	5.0 V	1.8 V	3.3 V
	3.3 V	1.8 V	1.8 V
	1.8 V	1.8 V	0 V
	1.2 V	1.8 V	0 V
	0.9 V	1.8 V	0 V
VLC2	5.0 V	0 V	3.3 V
VLC2_bar	5.0 V	3.3 V	0 V

pulled up to 5.0/3.3 V. Therefore, MP6 is turned on, Vgate1 is charged to 5.0/3.3 V to turn off MP5. At the same time, Vgate2 is pulled at 3.3/2 V through MN6 such that MP4 will be turned off to avoid gate-oxide overstress. When $V_{PAD} = 0/0.9/1.2/1.8$ V, Vgate1 and Vgate2 are biased at 0/0.9/1.2/1.4, respectively, such that MP4 and MP5 are turned on to pass the bias voltage, 1.8 V, to Vmp3.

3) VLC1: Fig. 11 shows the schematic of VLC1.

- When $\mathrm{VDDIO} = 5.0$ V and $\mathrm{UP} = 0$ V, Vctrl1_bar and VLC2_bar are biased at 0 V due to $\mathrm{VL\_5} = \mathrm{VL\_3} = 0$ V. MN310 and MN308 are turned off. Vmp1 must be discharged to VDD to avoid overstress on MP303 and MN313. MP305 and MP307 are both on due to $\mathrm{Vctrl1\_bar} = \mathrm{VLC2\_bar} = 0$ V such that the source of MN313 is biased at VDD. MN313 and MP303 are also on by Vbias. Therefore, Vmp1 is biased at VDD. Then, MP302 will be turned on, and Vmp4 will be pulled at 5.0 V. Therefore, Vmp1 is pulled up to 3.3 V. When $\mathrm{UP} = 1.8$ V, Vctrl1 and VLC2_bar are both equal to 0, Vmp1 will be pulled to 5.0 V and $\mathrm{Vmp4} = 3.3$ V.
- When VDDIO is 3.3 V and UP is 0 V, Vctrl1, Vctrl2 and Vctrl1_bar are all biased at 1.8 V. VL_3 becomes 0 V such that MN308 is turned off. Vmp1 is discharged through MN311, MN309, MN313 and MN303. MP302 is turned on. Vmp4 will be pulled up to 3.3 V. Vmp1 will be pulled down to 1.8 V though MP312, MP310, and MN301. If $\mathrm{UP} = 3.3$, then Vmp1 will be pulled up to 3.3 V, and Vmp4 will be pulled down to 1.8 V.
- When $\mathrm{VDDIO} = 1.8/1.2/0.9$ V and $\mathrm{UP} = 0$ V, Vctrl1 and Vctrl1_bar are biased at 1.8 V. Vmp1 will be discharged to 0 V through MN311, MN309, MN307, MN305 and MN303 such that MP302 is turned on. Vmp4 will be pulled to 1.8/1.2/0.9 V, respectively. When $\mathrm{UP} = 1.8$, Vmp4 will be discharged to 0 V, and Vmp1 is pulled up to 1.8/1.2/0.9 V, respectively. VL_3 is equal to 1.8 V in such a scenario such that MP312 will be turned off.

In summary, Table IV tabulates the functional table of VLC1.

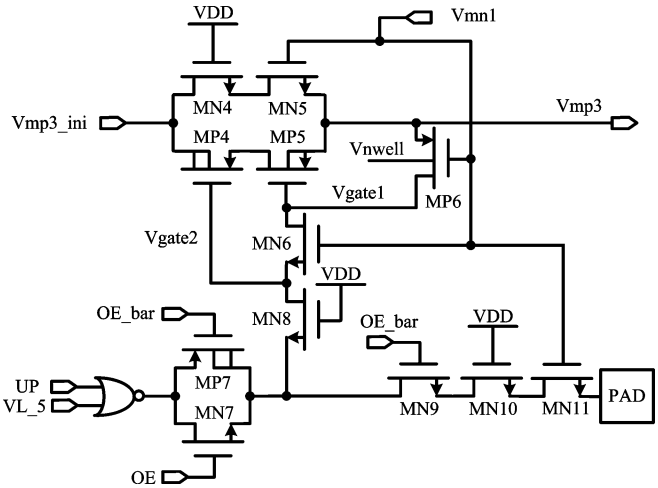

Fig. 10. Schematic of EOS protector.

C. High Voltage Detector

The schematic of the High voltage detector is shown in Fig. 12. It detects the voltage level of VDDIO to see if it is larger than 1.8 V or 3.3 V. Two corresponding signals, VL_5 and VL_3, and two biases, VB and Vbias, are generated to Dynamic gate bias generator. A close loop structure without any start-up circuit is utilized in this circuit.

- When $\mathrm{VDDIO} = 5.0$ V, MP106, MN106 and MN108 are turned on. Thus, MN109 is turned on and then VL_5 is pulled down to 0 V. MN107 is turned off. Notably, MN101 passes 1.8 V to the gate drives of MP104 and MP107. MN102 is turned on such that VL_3 is pulled down to 0 V, and MN103 is turned off. VC is approximately 3.3 V and MP101 is turned off.
- When $\mathrm{VDDIO} = 3.3$ V, MP106 is turned off, MP104 and MP107 are turned on. Then, VL_5 will be pulled to 1.8 V. MN107 is turned on to shut MN109 off. Meanwhile, MN102 is on such that VL_3 will be pulled to 0 V.

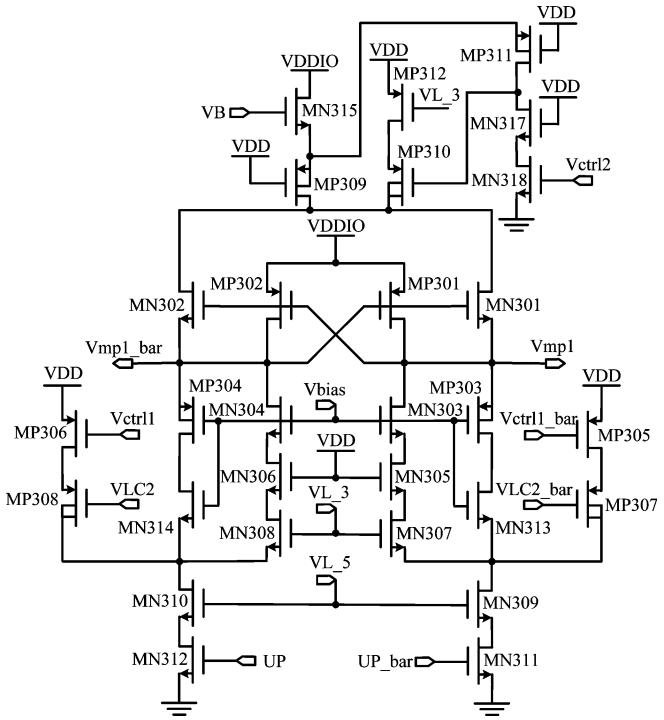

Fig. 11. Schematic of VLC1.

TABLE IV
FUNCTIONAL TABLE OF VLC1

Output	Input		
	VDDIO	when V_{PAD} is logic 0	when V_{PAD} is logic 1
Vmp1	5.0 V	5.0 V	3.3 V
	3.3 V	3.3 V	1.8 V
	1.8 V	1.8 V	0 V
	1.2 V	1.2 V	0 V
	0.9 V	0.9 V	0 V
Vmp4	5.0 V	3.3 V	5.0 V
	3.3 V	1.8 V	3.3 V
	1.8 V	0 V	1.8 V
	1.2 V	0 V	1.2 V
	0.9 V	0 V	0.9 V

Then, MN103 is turned off. VC is approximately 2.2 V and MN101 is turned off.

- When $\mathrm{VDDIO} = 1.8/1.2/0.9$ V, MP106 is off, MP104 and MP107 are turned on. Thus, $\mathrm{VL\_5} = 1.8$ V. MN107 will be turned to shut off MN109. Simultaneously, MP101 and MP102 are turned on to bias VL_3 at 1.8 V. MN102 will be turned off.

In short, when $\mathrm{VDDIO} = 5.0/3.3/1.8/1.2/0.9$ V, VL_5 is 0/1.8/1.8/1.8/1.8 V, and VL_3 is 0/0/1.8/1.8/1.8 V, respectively. The functional table of High voltage detector is summarized in Table V.

D. Pad Voltage Detector

Fig. 13 shows the proposed PAD voltage detector. Vx and Vy are, respectively, biased to drive the gates of MN401 and MP405 depending on $\mathrm{V_{PAD}}$ in order to generate Vmn1. Notably, Vmn1

TABLE V
FUNCTIONAL TABLE OF THE HIGH VOLTAGE DETECTOR

Input	Output			
VDDIO	Vbias	VL_5	VL_3	VB
5.0 V	3.3 V	0 V	0 V	4.3 V
3.3 V	1.8 V	1.8 V	0 V	2.6 V
1.8 V	1.8 V	1.8 V	1.8 V	1.1 V
1.2 V	1.8 V	1.8 V	1.8 V	0.5 V
0.9 V	1.8 V	1.8 V	1.8 V	0.2 V

TABLE VI
FUNCTIONAL TABLE OF THE PAD VOLTAGE DETECTOR

Input	Output
PAD	Vmn1
5.0 V	3.3 V
3.3 V	2.2 V
1.8 V	1.8 V
1.2 V	1.8 V
0.9 V	1.8 V
0 V	1.8 V

is needed in EOS protector, which is described in previous sections. The detailed description of PAD voltage detector is given as follows.

- When $\mathrm{V_{PAD}} = 5.0$ V, $\mathrm{Vx} = (\mathrm{V_{PAD}} - \mathrm{Vthn}) \cong 4.3$ V, where Vthn is a threshold voltage of NMOS. Vmn1 is then pulled up to $\mathrm{VDD} = 3.3$ V through MN401 and MP404. Vy is equal to $(\mathrm{V_{PAD}} - 2 \times \mathrm{Vthn}) \cong 3.6$ V such that MP405 is turned off to avoid the gate-oxide overstress of MN1 of the Output stage shown in Fig. 6.
- If $\mathrm{V_{PAD}} = 3.3$ V, Vx is 2.6 V. $\mathrm{Vmn1} \cong 2.2$ V through MN401 and MP404. Vy is approximately 2.0 V and MP405 is turned off.
- When $\mathrm{V_{PAD}}$ is 1.8/1.2/0.9 V, Vy is smaller than 1.8 V. Vmn1 is biased at 1.8 V through MP405. When $\mathrm{V_{PAD}}$ is 0 V, Vx and Vy are discharged through MP401 and MP402, to avoid gate-oxide overstress. Vmn1 is pulled to 1.8 V through MNP405.

The functional table of PAD voltage detector is then summarized in Table VI.

E. Output Stage

Stacked pMOS and stacked nMOS are adopted to prevent gate-oxide overstress. The gates of MP1, MP2, MP3, MN1, and MN3 in the Output stage circuit, as shown in Fig. 6, are biased at corresponding appropriate biases generated by the Pre-driver circuit, Dynamic gate bias generator, and PAD voltage detector. The corresponding biases of these transistors are tabulated in Table II.

F. Floating N-Well Circuit

The Floating N-well circuit is composed of MP503, MN501, MP502 and MP501, as shown in Fig. 14. It provides the N-well voltage of MP3 to prevent the leakage current path formed by the parasitic P+/N-well diode. As stated, $\mathrm{V_{PAD}} = 5.0/3.3$ V, $\mathrm{Vmn1} = 3.3/2.2$ V. Thus, MP501 and MP503 are turned on. MP502 and MN501 are turned off. Vnwell is equal to 5.0/3.3 V,

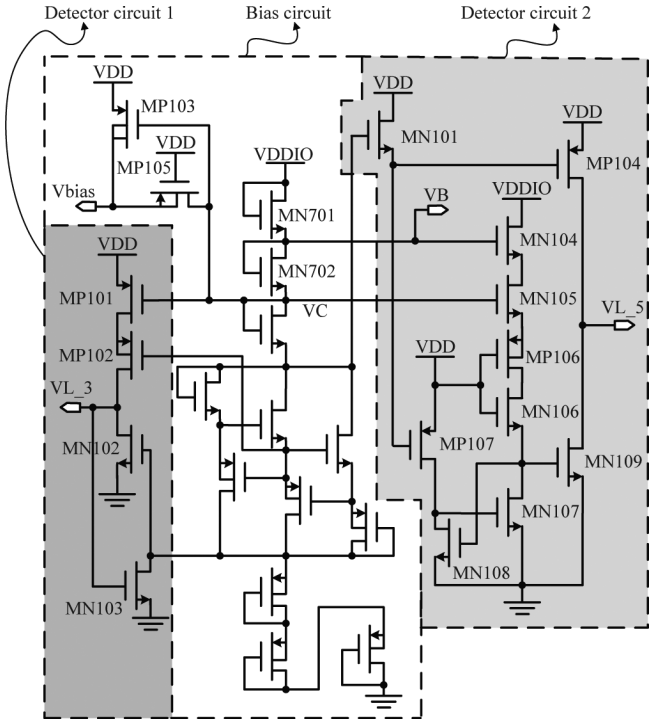

Fig. 12. Schematic of High voltage detector.

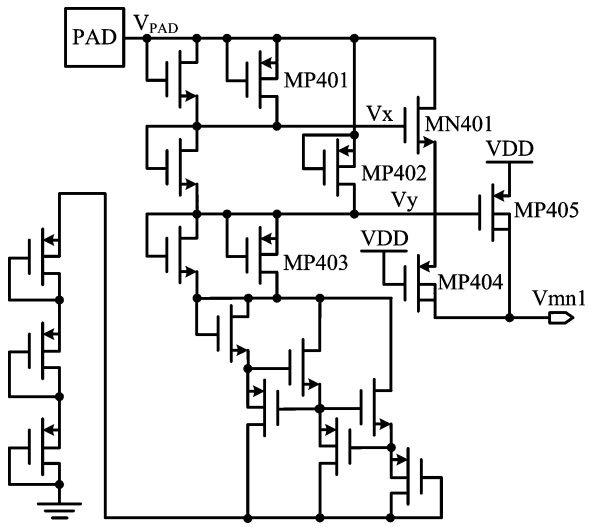

Fig. 13. Schematic of PAD voltage detector.

respectively, such that the parasitic diode of MP3 no longer exists. Besides, since $\mathrm{Vmn1} = 3.3/2.2$ V, all transistors of the Output stage have no gate-oxide overstress. When $\mathrm{V_{PAD}} = 0/0.9/1.2/1.8$ V, MP502 and MN501 will be turned on. MP503 and MP501 will be turned off. Therefore, Vnwell is pulled to 1.8 V through MP502, and $\mathrm{Vmn} = 1.8$ V.

G. Gate-Tracking Circuit

Gate-tracking circuit consists of MP4 and MP5, as shown in Fig. 6. It prevents the leakage current path through MP3 in the Rx mode. If $\mathrm{VDDIO} = 5.0/3.3$ V and logic 1 is received,

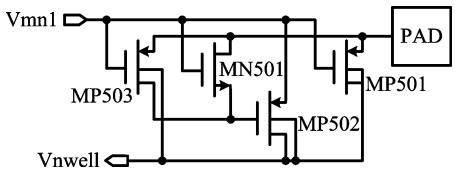

Fig. 14. Schematic of Floating N-well circuit.

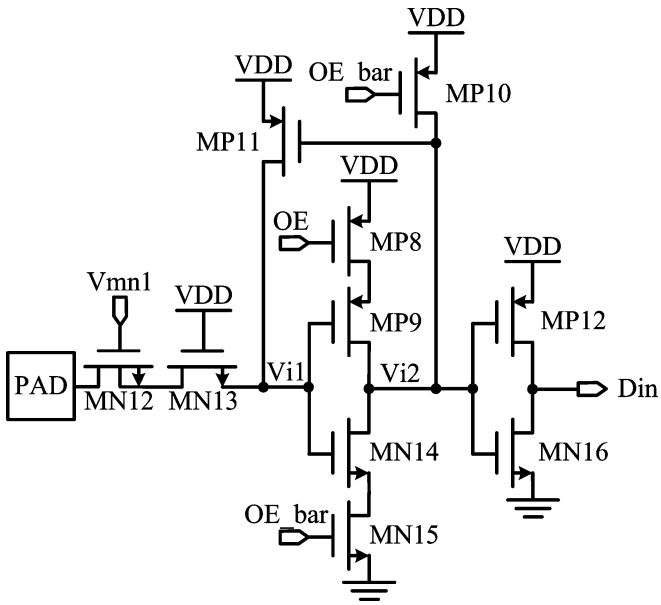

Fig. 15. Schematic of Input stage.

$\mathrm{Vmp4} = 5.0/3.3$ V to turn off MP4. Vmp3 is then not affected by $\mathrm{V_{PAD}}$. In the Tx mode, if $\mathrm{VDDIO} = 5.0/3.3$ V and $\mathrm{Vmp4} = 3.3/1.8$ V, MP4 will be turned on to equalize the gate voltage of MP3 and $\mathrm{V_{PAD}}$. Thus, the leakage current through MP3 will not exist. The gate-oxide overstress of MN4 and MP5 is also eliminated.

H. Input Stage

Several input stages have been reported to be able to receive the input signal with a voltage level higher than the supply voltage VDD, e.g., [5]. It can accept the voltage from 0.9 V to 5.0 V by tuning transistor aspects. The Input stage of the prior I/O buffers might have gate-oxide overstress when the received signal is 5.0 V or 3.3 V if a standard 0.18 μm CMOS process is used. MN12 and MN13 in the Input stage of the proposed I/O shown in Fig. 15 are able to isolate any unexpected high voltage at PAD. When $\mathrm{V_{PAD}}$ is 5.0/3.3 V, Vi1 would be close to 1.4 V, the gate-oxide overstress hazard of MN14 is eliminated. When $\mathrm{V_{PAD}}$ is logic 1, Vi2 becomes 0 V to turn on MP11. MP11 pulls Vi1 up to 1.8 V to ensure MP9 is turned off. If in the Tx mode, $\mathrm{OE} = 1.8$ V. MP8 and MN15 are turned off. MP10 is then turned on such that Vi2 is pulled up to 1.8 V to turn off MP11. The leakage, thus, is avoided. Notably, an isolated p-well is used for MN12 to prevent the hazard from the overstress between the bulk and p-substrate. Although the

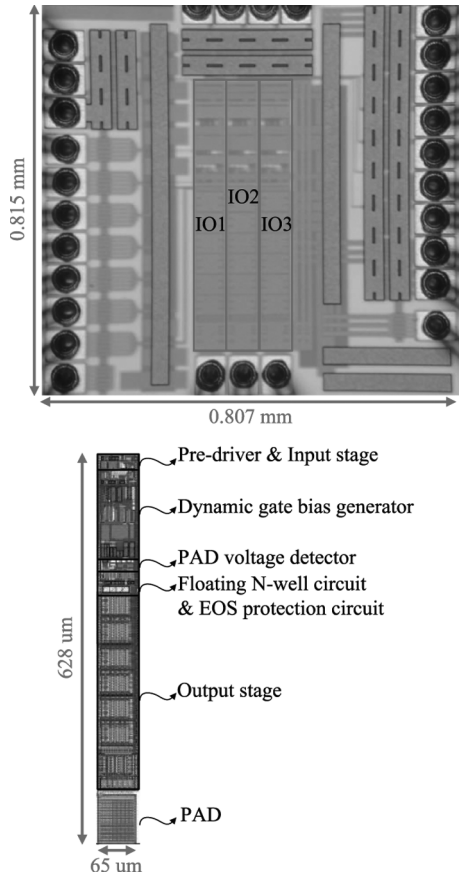

Fig. 16. The die photo of the proposed I/O buffer.

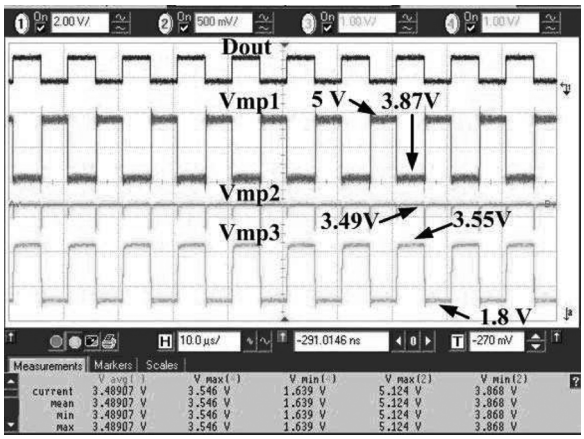

Fig. 17. Measured Vmp1, Vmp2, Vmp3 and Dout at 100 KHz in Tx mode $(\mathrm{VDDIO} = 5.0\,\mathrm{V})$.

isolated p-well needs one mask, the cost is still lower than that of thick-oxide devices.

III. Implementation and Measurement

TSMC (Taiwan Semiconductor Manufacturing Company) standard $0.18\ \mu$m CMOS technology is adopted to carry out the proposed I/O buffer. To reduce the cost of the process and the manufacture, the proposed I/O buffer employed no thick-oxide devices. Fig. 16 is the die photo of the proposed design. Three proposed I/O buffers are included in the same die for testing consideration. Vmp1, Vmp2, Vmp3 and Vnwell are respectively output for measurement and observation. Guard rings are drawn to avoid latch up problems. The area of the proposed I/O buffer is $65 \times 628\ \mu\mathrm{m}^2$. Notably, VDD should be powered up

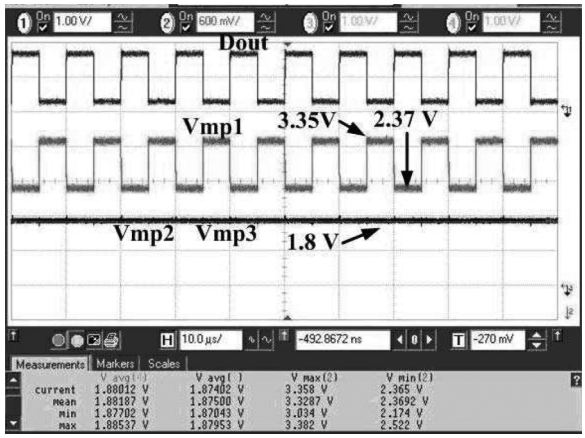

Fig. 18. Measured Vmp1, Vmp2, Vmp3 and Dout at 100 KHz in Tx mode $(\mathrm{VDDIO} = 3.3\,\mathrm{V})$.

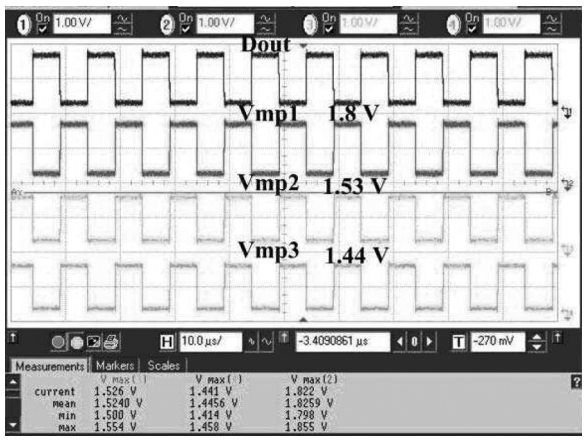

Fig. 19. Measured Vmp1, Vmp2, Vmp3 and Dout at 100 KHz in Tx mode $(\mathrm{VDDIO} = 1.8\,\mathrm{V})$.

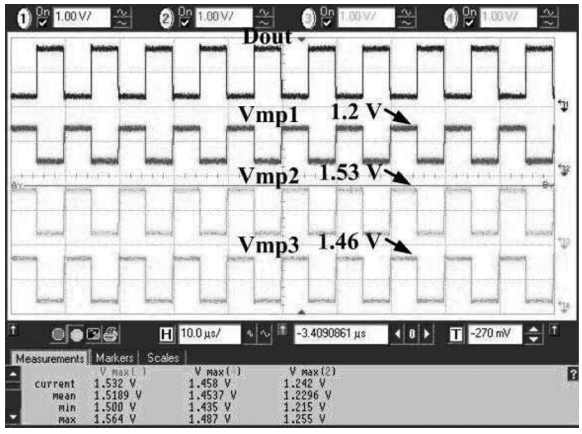

Fig. 20. Measured Vmp1, Vmp2, Vmp3 and Dout at 100 KHz in Tx mode $(\mathrm{VDDIO} = 1.2\,\mathrm{V})$.

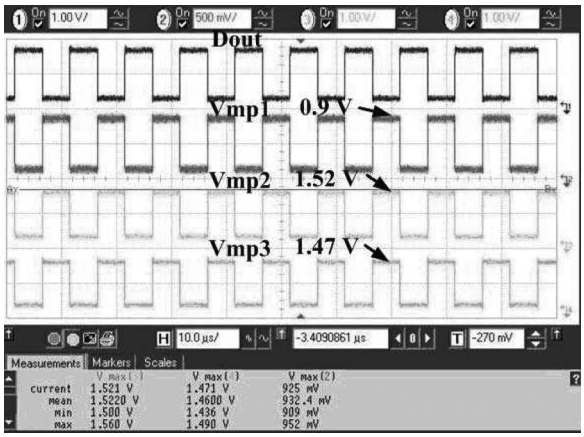

Fig. 21. Measured Vmp1, Vmp2, Vmp3 and Dout at 100 KHz in Tx mode ($\mathrm{VDDIO} = 0.9\,\mathrm{V}$).

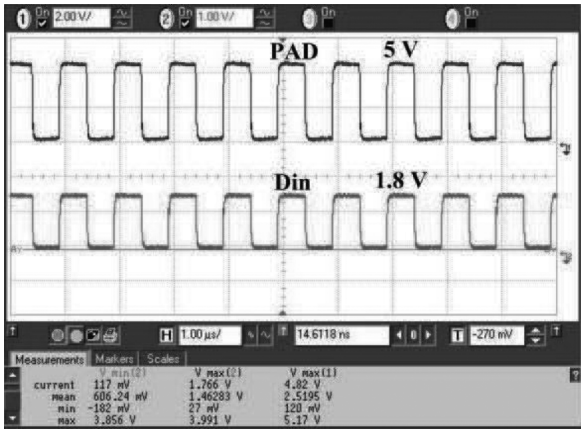

Fig. 22. Measured $\mathrm{V_{PAD}}$, and Din at 1 MHz in Rx mode ($\mathrm{VDDIO} = 5.0\,\mathrm{V}$).

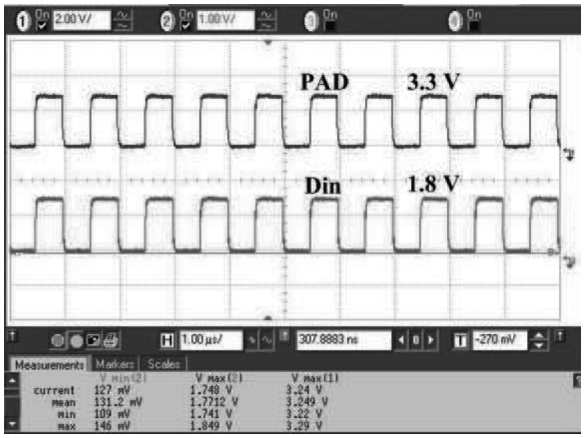

Fig. 23. Measured $\mathrm{V_{PAD}}$, and Din at 1 MHz in Rx mode ($\mathrm{VDDIO} = 3.3\,\mathrm{V}$).

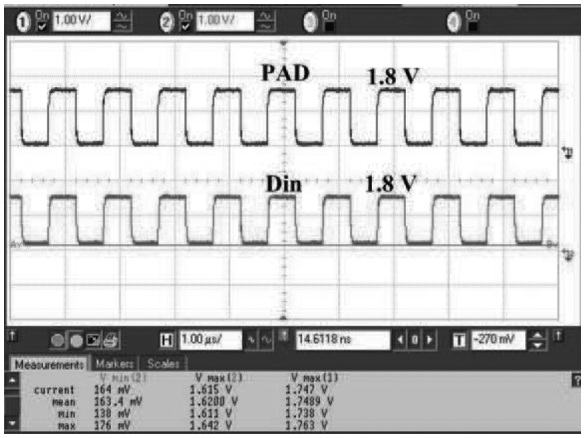

Fig. 24. Measured $\mathrm{V_{PAD}}$, and Din at 1 MHz in Rx mode ($\mathrm{VDDIO} = 1.8\,\mathrm{V}$).

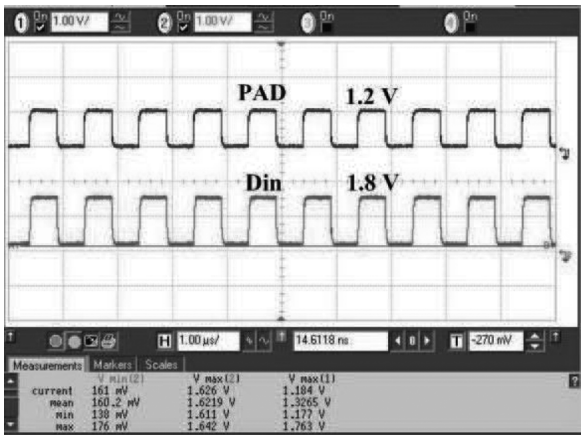

Fig. 25. Measured $\mathrm{V_{PAD}}$, and Din at 1 MHz in Rx mode ($\mathrm{VDDIO} = 1.2\,\mathrm{V}$).

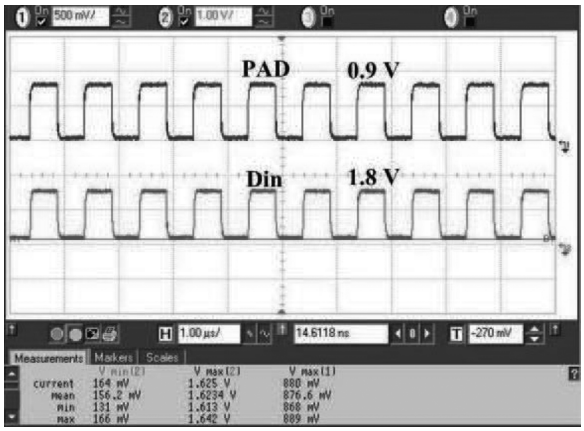

Fig. 26. Measured $\mathrm{V_{PAD}}$, and Din at 1 MHz in Rx mode ($\mathrm{VDDIO} = 0.9\,\mathrm{V}$).

before VDDIO to avoid the risk that the high voltage causes the MOS break down, when VDDIO is biased at 5 V or 3.3 V.

Figs. 17–21 illustrate the measurement results of Vmp1, Vmp2, Vmp3 and Dout at 100 KHz on silicon in the Tx mode for $\mathrm{VDDIO} = 5.0/3.3/1.8/1.2/0.9$ V, respectively. For $\mathrm{VDDIO} = 5.0$ V, Vmp1 is biased at 3.87/5.0 V for transmitting logic 1/0, respectively, as shown in Fig. 17. Moreover, Vmp2 and Vmp3 are biased at 3.49 V and 1.8/3.55 V, respectively. Therefore, the gate-oxide reliability for MP2 and MP3 is ensured.

Figs. 22–26 show $\mathrm{V_{PAD}}$, and Din in Rx mode for $\mathrm{VDDIO} = 5.0/3.3/1.8/1.2/0.9$ V when given 5.0/3.3/1.8/1.2/0.9 V signals at the PAD, respectively.

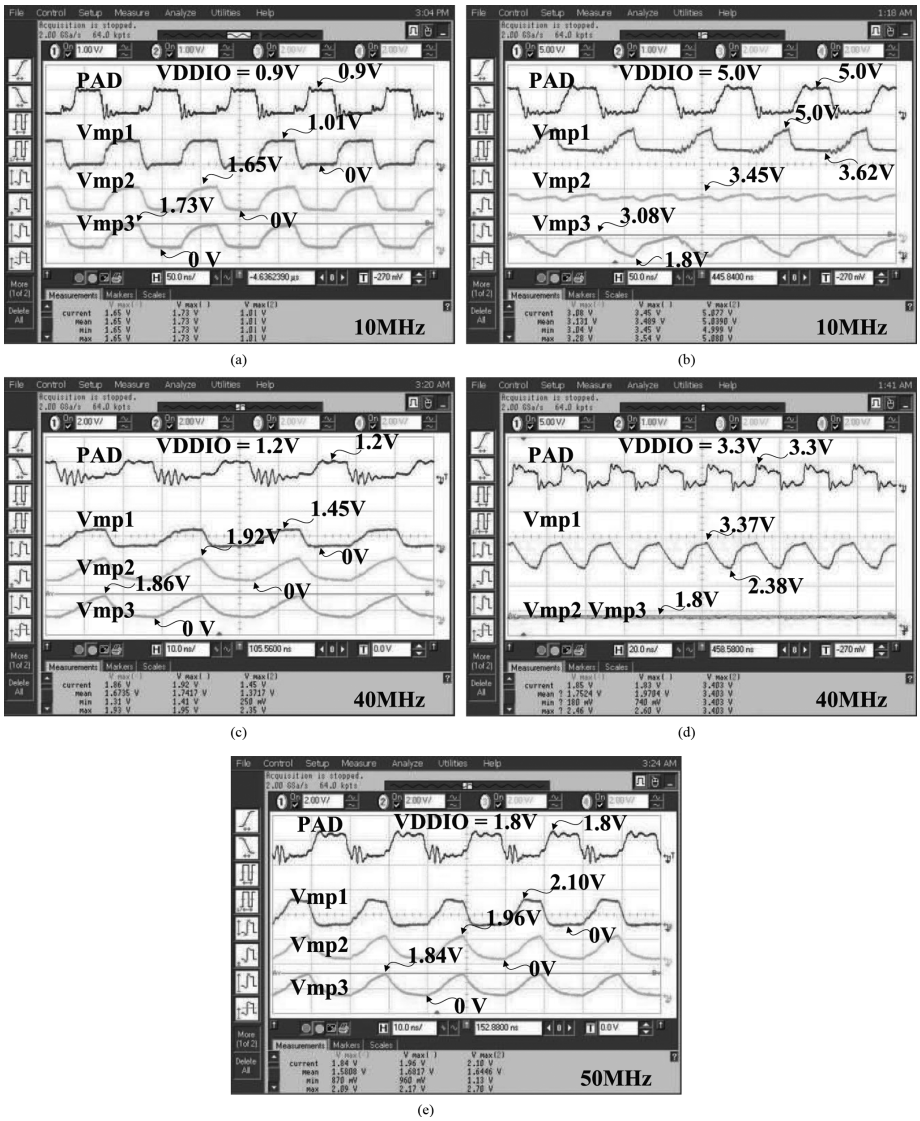

Fig. 27. Maximum speed of different VDDIO in Tx mode ($\mathrm{VDDIO} = 5.0/3.3/1.8/1.2/0.9$ V).

TABLE VII
CORNER SIMULATION RESULTS OF THE STATIC POWER CONSUMPTION

	VDD = 1.98 V transistor model = FF T = -20°C VDDIO = VDDIO×1.1	VDD = 1.8 V transistor model = TT T = 25°C VDDIO = VDDIO	VDD = 1.62 V transistor model = SS T = 100°C VDDIO = VDDIO×0.9
VDDIO = 5.0 V	12.44	0.788	0.81
VDDIO = 3.3 V	36.16	3.58	0.71
VDDIO = 1.8 V	0.014	0.020	0.162
VDDIO = 1.2 V	0.0082	0.015	0.13787
VDDIO = 0.9 V	0.00789	0.0146	0.134

*The unit of static power consumption is μW.

Fig. 27 shows the measurement result of the maximum speed of each VDDIO in Tx mode. When $\mathrm{VDDIO} = 5.0/3.3/1.8/1.2/0.9$ V, the maximum speed in Tx are 10/40/50/40/10 MHz, respectively. On the other hand, the measurement result of the maximum speed in Rx is 50 MHz. The load of the speed measurement is 19 pF (the wire load + input capacitance of the OSC probe).

Table VII shows the corner simulation results of the static power consumption. When VDD = 1.98 V and VDDIO = 5.5 V or 3.63 V, the power consumptions are obviously larger than that of other corners. The reason could be that some transistors are not be turned off completely.

The proposed I/O buffer circuit is also tested on silicon at 100°C and −20°C using thermo stream chamber (TP 0400A-2B21-2). The measurement results of Vmp1, Vmp2, Vmp3, Vnwell, and V_{PAD} closely match those in Figs. 17–21. The power consumption is 3.9 μW. Table VIII shows the comparison with several prior works. The proposed I/O buffer provides the widest

TABLE VIII
COMPARISON WITH SEVERAL PRIOR WORKS

	[11]	[20]	[5]	[6]	[12]	[21]	Ours
# of voltage modes	1	1	2	2	1	3	5
Tx VDDH	Yes	Yes	No	No	Yes	Yes	Yes
Tx VDDL	No	No	No	No	No	Yes	Yes
Rx VDDH	Yes	No	Yes	Yes	No	Yes	Yes
Rx VDDL	No	No	No	No	No	Yes	Yes
Max. operating voltage	2.2 × VDD	3 × VDD	2 × VDD	3 × VDD	3.3 × VDD	1.5 × VDD	3 × VDD
Min. operating voltage	2.2 × VDD	3 × VDD	VDD	VDD	3.3 × VDD	0.54 × VDD	0.5 × VDD
Output stage	3P3N	3P3N	1P2N	1P1N	2P2N	2P2N	3P3N
Thick-oxide	No	No	No	No	Yes	No	No
Normal voltage (VDD)	2.5 V	2.5 V	2.5 V	1.0 V	1.0 V	3.3 V	1.8 V
Process (μm)	0.25	0.25	0.25	0.13	0.13	0.35	0.18
Area (mm^2)	N/A	5.76	N/A	0.0105	0.0316	0.0336	0.04082
Power (mW)	N/A	N/A	0.0116	N/A	29.77	N/A	0.0039
Speed (MHz)	50	10	470	133	133	80	50
Year	2005	2005	2006	2006	2007	2009	2009

operating voltage $(0.5 \times \text{VDD} \sim 3 \times \text{VDD})$ and low power dissipation.

IV. CONCLUSION

A wide-range bidirectional I/O buffer with 0.9/1.2/1.8/3.3/5.0 V tolerant is proposed in this study. The proposed I/O buffer can transmit and receive the signals with voltage levels over $1/2\text{VDD} \sim 3$ VDD by using an extra supply voltage VDDIO. No thick-oxide devices are needed in this work. Dynamic gate bias provides appropriate voltages for the gate drives of the stacked pMOS to ensure gate-oxide reliability. The static power consumption is merely 3.9 μW by measurement on silicon. Compared with several prior works, the proposed design attains the widest range voltage.

V. ACKNOWLEDGEMENT

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REFERENCES

[1] M. J. M. Pelgrom and E. C. Dijkmans, "A 3/5 V compatible I/O buffer," *IEEE J. Solid-State Circuits*, vol. 30, no. 7, pp. 823–825, Jul. 1995.

[2] C.-H. Chuang and M.-D. Ker, "Design on mixed-voltage-tolerant I/O interface with novel tracking circuits in a 0.13-μm CMOS technology," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2004, vol. 2, pp. 577–580.

[3] E. R. Minami, S. B. Kuusinen, E. Rosenbaum, P. K. Ko, and C. Hu, "Circuit-level simulation of TDDB failure in digital CMOS circuit," *IEEE Trans. Semiconduct. Manufact.*, vol. 8, no. 8, pp. 370–374, Aug. 1995.

[4] R. Moazzami and C. Hu, "Projecting gate oxide reliability and optimizing reliability screens," *IEEE Trans. Electron Devices*, vol. 37, no. 7, pp. 1643–1650, Jul. 1990.

[5] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Overview and design of mixed-voltage I/O buffers with low-voltage thin-oxide CMOS transistors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 9, pp. 1934–1945, Sep. 2006.

[6] M.-D. Ker and S.-L. Chen, "Design of mixed-voltage I/O buffer by using NMOS-blocking technique," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2324–2333, Oct. 2006.

[7] M. Takahashi, T. Sakurai, K. Sawada, K. Nogami, M. Ichida, and K. Matsuda, "3.3 V–5 V compatible I/O circuit without thick gate oxide," in *Proc. IEEE Custom Integr. Circuit Conf.*, 1992, pp. 23.3.1–23.3.4.

[8] C. Petersen and A. R. Barlow, "High voltage circuits in standard CMOS processes," in *Proc. IEDM Tech. Dig.*, 1982, pp. 287–291.

[9] M.-D. Ker and C.-H. Chung, "Electrostatic discharge protection for design for mixed-voltage CMOS I/O buffers," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1046–1055, Aug. 2002.

[10] G. Liu, Y. Wang, and S. Jia, "A new design of mixed-voltage I/O buffers with low-voltage-thin-oxide CMOS process," in *Proc. Int. Conf. ASIC*, Oct. 2007, pp. 201–204.

[11] A.-J. Annema, G. J. G. M. Geelen, and P. C. de Jong, "5.5-V I/O in a 2.5-V 0.25-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 528–538, Mar. 2001.

[12] S.-L. Chen and M.-D. Ker, "An output buffer for 3.3-V applications in a 0.13-μm 1/2.5-V CMOS process," *IEEE Trans. Circuits Syst. II, Exp. Brief*, vol. 54, no. 1, pp. 14–18, Jan. 2007.

[13] M.-D. Ker and S.-L. Chen, "Mixed-voltage I/O buffer with dynamic gate-bias circuit to achieve $3 \times$ VDD input tolerance by using $1 \times$ VDD devices and single VDD supply," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2005, vol. 1, pp. 524–614.

[14] H. Sanchez, J. Siegel, C. Nicoletta, J. P. Nissen, and J. Alvarez, "A versatile 3.3/2.5/1.8-V CMOS I/O driver built in a 0.2-μm, 3.5-nm tox, 1.8-V CMOS technology," *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp. 1501–1511, Nov. 1999.

[15] M.-D. Ker and F.-L. Hu, "Design on mixed-voltage I/O buffers with consideration of hot-carrier reliability," in *Proc. Int. Symp. VLSI Design, Auto. Test*, Apr. 2007, pp. 36–39.

[16] R. Chauhan, K. Rajagopal, V. Menezes, H. M. Roopashree, and S. K. Jacob, "A high performance, high voltage output buffer in a low voltage CMOS process," in *Proc. IEEE 2005 Custom Integr. Circuits Conf.*, Sep. 2005, pp. 227–230.

[17] A. T. Krishnan, V. Reddy, S. Chakravarthi, J. Rodriguez, S. John, and S. Krishnan, "NBTI impact on transistor and circuit: Models, mechanisms and scaling effects," in *Proc. IEEE Int. Electron Device Meeting Tech. Dig.*, Dec. 2003, pp. 14.5.1–14.5.4.

[18] G. P. Singh and R. B. Salem, "High-voltage-tolerant I/O buffers with low-voltage CMOS process," *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp. 1512–1525, Nov. 1999.

[19] T.-J. Lee, W.-C. Chang, and C.-C. Wang, "Mixed-voltage-tolerant I/O buffer using a clamping dynamic gate bias generator," in *Proc. IEEE Region 10 Conf. TENCON 2007*, Oct. 2007, p. 148, CD-ROM, FrSC-O 9.3.

[20] B. Serneels, T. Piessens, M. Steyaert, and W. Dehanene, "A high-voltage output driver on a 2.5-V 0.25-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 576–583, Mar. 2005.

[21] T.-J. Lee, T.-Y. Chang, and C.-C. Wang, "Wide-range 5.0/3.3/1.8 V I/O buffer using 0.35-μm 3.3-V CMOS technology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 4, pp. 763–772, Apr. 2009.

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