Self-Sampled All-MOS ASK Demodulator for Lower ISM Band Applications

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***Abstract*—An all-MOS ASK demodulator with a wide bandwidth for lower industrial, scientific and medical (ISM) band applications is presented. The chip area is reduced without using any passive element. It is very compact to be integrated in a system-on-chip for wireless biomedical applications, particularly in biomedical implants. Because of low area cost and low power consumption, the proposed design is also easy to integrate in other mobile medical devices. The self-sampled loop with a MOS equivalent capacitor compensation mechanism enlarges the bandwidth, which is more than enough to be adopted in any application using lower ISM bands.**

***Index Terms*—Amplitude shift keying (ASK) demodulator, industrial, scientific and medical (ISM) band, self-sampled, wireless communication.**

I. Introduction

RECENTLY, implantable biomedical devices, i.e., bioimplants, have become a popular research topic, particularly in applications of electrical stimulations. Biomedical implants have been developed to diagnose or cure patients' diseases, e.g., bladder stimulation for urine control [1], neuron electrical microstimulation to alleviate paralysis and atrophy [2], and cortical neural prosthesis for deep brain stimulation, which has been deemed as one of the promising solutions for the disabilities of Parkinson's disease [3].

Two of the most important issues of biomedical implants are the patient's safety and comfort. To avoid the risk of infection on any wound caused by wired connections, wireless connection has widely been adopted in many implants. The implants can be powered and commanded by a pair of coils (external and internal) using a transcutaneous magnetic coupling method to ensure safety. The amplitude shift keying (ASK) modulation is particularly suitable for the coil-coupling method in biomedical implants because of its simplicity [4]–[11]. Moreover, due to the recent development of system-on-chip (SOC) technology, the size of the implants is drastically shrunk.

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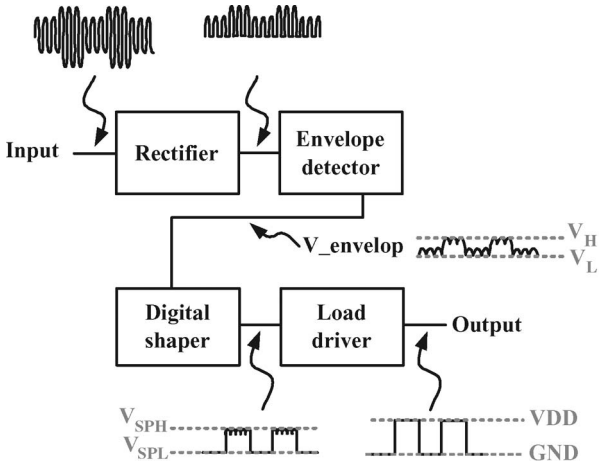

Fig. 1. Architecture of the proposed ASK demodulator.

Traditionally, ASK demodulators in implanted devices [4]–[6] needed a large capacitor, which can either be a discrete component on a printed circuit board or occupy a huge area on chip. Consequently, an extra discrete component increases the size of the implants, which might cause discomfort to the patient. On the other hand, the area cost becomes very expensive if advanced processes are used for the SOC realization for the implants. Obviously, a large capacitor becomes unaffordable for the ASK demodulator in SOC solutions. Then, the ASK demodulator in [7] without using any capacitor was proposed to save area, as well as cost. Furthermore, the design in [11] got rid of another passive element, i.e., a resistor, to save more area on silicon. However, the ASK demodulator in [11] needed a unit gain buffer, which works as a rectifier and causes redundant power consumption. In addition, the bandwidth of all of the prior ASK demodulators is too low to be employed for many industrial, scientific and medical (ISM) bands, including 6.78, 13.56, 27.120, and 40.68 MHz [12]–[14]. All of these public bands are widely utilized in ISM applications. The ASK demodulator bandwidth should cover as wide as possible in the ISM band such that it could be employed in a variety of wireless applications.

Therefore, a novel ASK demodulator is proposed without using any passive element in this work. By decoupling the parasitic capacitor, the bandwidth of the proposed ASK demodulator is more than 300 MHz, which is more than enough for almost all kinds of biomedical SOC implants using lower ISM bands.

II. System Consideration and Circuit Design

The proposed ASK demodulator is composed of four subcircuits, as shown in Fig. 1, including a rectifier, an envelope

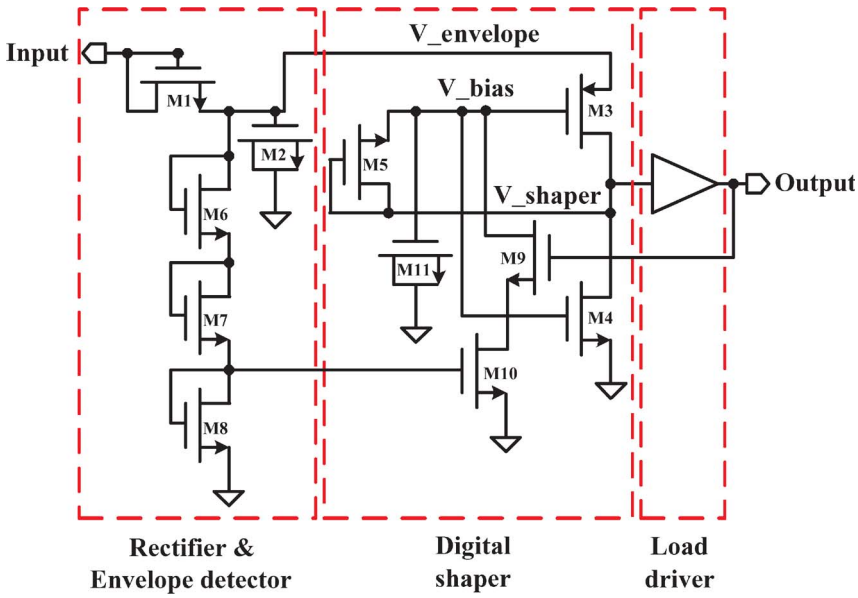

Fig. 2. Schematic of the proposed ASK demodulator.

detector, a digital shaper, and a load driver. Because of the limited input range, the amplitude of the ASK signal delivered from the coil of implants must be reduced by a voltage divider (not shown). Then, the rectifier converts the received ASK signal into a half-wave. The envelope detector picks up the envelope of the half-wave. The digital shaper is the most important part, which recovers the digital data from the envelope. At last, the load driver provides a large driving current to pull the output from rail to rail. Fig. 2 shows the entire circuit of the proposed design. Since the load driver is composed of two inverters, the proposed ASK demodulator is very compact without any passive element.

A. Rectifier and Envelope Detector

Referring to Fig. 2, the diode-connected transistor (M1) and the current path (M6–M8) work as a rectifier to reject the negative voltage of the ASK signal. M2 serves as a peak detector to pick up the envelope voltage of the half-wave from the rectifier, i.e., V_envelope. The mark (high voltage) level of V_envelope(V_H) is generated when the high level of the ASK signal is received, and vice versa for the space (low voltage) level.

B. Digital Shaper

The digital shaper converts the envelope signal generated by M2 into a digital signal such that the following load driver can provide a rail-to-rail logic output accordingly. The operation of the digital shaper is described as follows:

Start-Up: In the initial state, V_bias is 0 V, and M3 is turned on. If there is any positive voltage on the source of M3, V_bias would be biased on a certain voltage via M3 and the diode-connected M5.

Normal Operation: When V_envelope $= V_H$, the V_bias will turn on M3. M3–M5 operate in the saturation region, and the drain current of M3 and M4 I_{M3} can be written as

$$\begin{aligned} I_{M3} &= \frac{\beta_3}{2}(V_H - V_{\mathrm{SPH}} + V_{\mathrm{TH5}} - V_{\mathrm{TH3}})^2 \\ &= \frac{\beta_4}{2}(V_{\mathrm{SPH}} - V_{\mathrm{TH5}} - V_{\mathrm{TH4}})^2 \end{aligned} \tag{1}$$

where V_{TH4} and V_{TH5} are the threshold voltages of M4 and M5, respectively, V_{TH3} is the threshold voltage of M3, V_{SPH} is the high-voltage value of $V_{\mathrm{ENV\_SIG}}$, and β_3 and β_4 represent the device parameters of M3 and M4, respectively.

On the other hand, when V_envelope $= V_L$, M3 operates in the cutoff region, and V_L can be expressed as

$$V_L = V_{\mathrm{SPH}} + V_{\mathrm{TH3}} - V_{\mathrm{TH5}}. \tag{2}$$

When the output voltage is at logic 0, M3 is turned off, and M4 is turned on. V_shaper is discharged to 0 V, and V_{SPL} now is also assumed to be 0 V. Notably, V_{SPL} is the low voltage of V_{shaper}.

Given $V_{\mathrm{TH4}} = V_{\mathrm{TH5}} = V_{\mathrm{THN}}$, (1) can be simplified as

$$V_H = V_{\mathrm{SPH}} + V_{\mathrm{TH3}} - V_{\mathrm{THN}} + \sqrt{\frac{\beta_4}{\beta_3}}(V_{\mathrm{SPH}} - 2V_{\mathrm{THN}}). \tag{3}$$

If (2) and (3) are both taken into consideration, the difference between V_H and V_L can be derived as

$$\Delta V = V_H - V_L = \sqrt{\frac{\beta_4}{\beta_3}}(V_{\mathrm{SPH}} - 2V_{\mathrm{THN}}). \tag{4}$$

Equation (4) shows that the difference between high- and low-level signals can be adjusted by the β ratio of M3 and M4. In order to minimize ΔV, the size of M3 should be much larger than that of M4. In addition, ΔV is designed to be

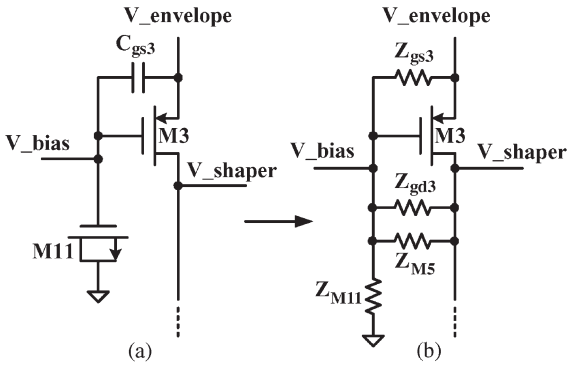

Fig. 3. Equivalent circuit at high frequency.

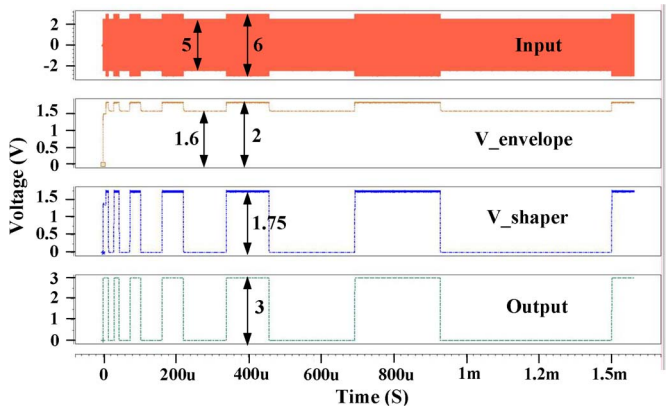

Fig. 4. Worst-case postlayout simulation result.

proportional to $\sqrt{\beta_4/\beta_3}$, which can eliminate the side effect caused by process deviation.

C. Noise Analysis

According to the preceding analysis, V_bias is the critical gate drive for M3 to slice the logic level of the envelope signal. Hence, it is important to keep the V_bias stable. M11 acts as an S-D-shorted capacitor C_{M11} to resist the high-frequency noise from the ripple of V_envelope. Referring to Fig. 3(a), which is the simplified schematic of M3, the parasitic capacitance $C_{\rm gs3}$ between the gate and source of M3 is much smaller than C_{M11}. In other words, Z_{M11} is far smaller than $Z_{\rm gs3}$ at a high frequency. Therefore, the equivalent circuit shown in Fig. 3(b) gives the equation of the noise on V_bias coupled from V_envelope as follows:

$$\text{N\_bias} = \frac{\text{N\_envelope} \times Z_{M11}//Z_{\rm gd3}//Z_{M5}}{Z_{M11}//Z_{\rm gd3}//Z_{M5} + Z_{\rm gs3}} + \frac{\text{N}_{\rm shapper} \times Z_{M11}//Z_{\rm gs3}}{Z_{M11}//Z_{\rm gs3} + Z_{\rm gd3}//Z_{M5}} \quad (5)$$

where N_bias is the noise on V_bias, N_envelope is the noise on V_envelope, N_shaper is the noise on V_shaper, $Z_{\rm gd3}$ is the parasitic impedance between the gate and drain of M3, and Z_{M5} is the parasitic impedance of M5. When $Z_{M11} \ll Z_{\rm gs3}$ and $Z_{M11} \ll Z_{\rm gd3}$ at a high frequency, the preceding equation can be derived as

$$\text{N\_bias} = \frac{\text{N\_envelope} \times Z_{M11}//Z_{M5}}{Z_{M11}//Z_{M5} + Z_{\rm gs3}} + \frac{\text{N\_shapper} \times Z_{M11}}{Z_{M11} + Z_{M5}}. \quad (6)$$

Since $Z_{M11} \ll Z_{M5}$ again at a high frequency, the N_shaper term approaches zero such that (6) can be simplified as

$$\text{N\_bias} = \frac{\text{N\_envelope} \times Z_{M11}//Z_{M5}}{Z_{M11}//Z_{M5} + Z_{\rm gs3}}. \quad (7)$$

Therefore, the M11 can resist the high-frequency noise from V_shaper. In short, V_bias is decoupled from V_envelope in high-frequency bands.

D. Self-Sampled Loop

If there is no dc path from V_bias to ground, the redundant charge from the noise of V_envelope would be accumulated on V_bias to increase the bias voltage. Then, the slicing function of the digital shaper will be contaminated because of the wrong gate drive voltage of M3. Therefore, M10 works as an active load to provide a dc path through M9. When the V_envelope is high, M9 will be turned on to discharge the redundant charge on V_bias. On the other hand, when the V_envelope is low, V_shaper will be 0 V and cut off M5. Since there is no charging path to V_bias, M9 is also cut off to stabilize V_bias. The loop through M9 is called the self-sampled loop, which means that the loop, which is a path from the output to the input or a certain node at the middle of the circuit, can generate a reference voltage level, compared to the input voltage of the ASK demodulator on chip. In prior works, an extra voltage signal is needed in the ASK demodulator as a reference bias [13]. By contrast, our design does not need such a reference voltage. We simply "sample" the output voltage as a reference voltage to achieve the same function.

E. Loop Driver

The output signal of the digital shaper is digital pulses with noise ripple. What is even worse is that it is not a rail-to-rail logic. Therefore, a load driver is required to generate a perfect digital signal and boost the driving current. The load driver is composed of two inverters whose switch points have been tuned to match the output signal of the digital shaper.

III. Simulation and Measurement Results

The Taiwan Semiconductor Manufacturing Company (TSMC) 0.35-μm 2P4M CMOS process is adopted to carry out the proposed ASK demodulator design. According to the worst-case transient postlayout simulations shown in Fig. 4, the proposed design can perfectly demodulate the ASK signal in different data rates. Fig. 5 shows each minimum threshold for ASK high-level voltage in every process, voltage, and temperature (PVT) corner. For the sake of robustness, the ASK

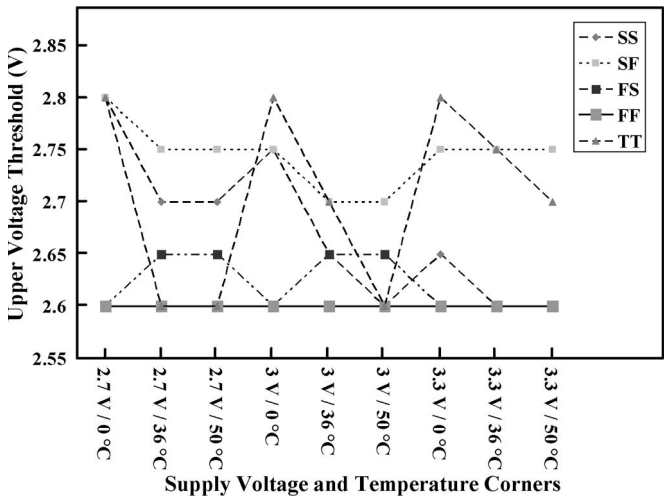

Fig. 5. Upper voltage threshold at 45 different corners.

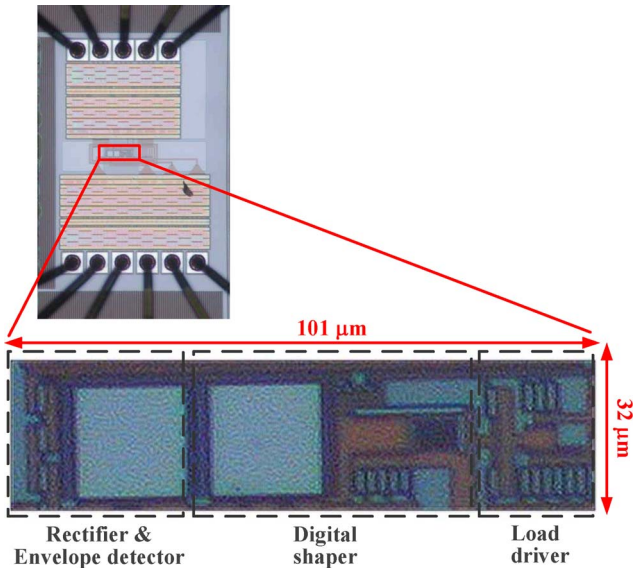

Fig. 6. Die photo of the proposed design.

low level has been selected to be 2.5 V. Meanwhile, referring to Fig. 5, the worst threshold of the ASK high level is 2.8 V. Therefore, basing on the threshold (2.5 V, 2.8 V), the maximum carrier frequency and maximum data rate are 240 MHz and 50 kb/s, respectively.

Fig. 6 shows the die photo of the proposed all-MOS ASK demodulator. The chip area is 101 μm $\times$ 32 μm, which occupies merely 0.003025 mm^2. In order to determine the maximum data rate, the carrier frequency is fixed at 13.56 MHz. Fig. 7 shows the measured waveform of the ASK modulated and ASK demodulated signals when the data rate is 1 Mb/s. Moreover, Fig. 8 shows that the proposed ASK demodulator can even recover the modulated signal correctly when the data rate is up to 1.2 Mb/s. For wireless communication used in biomedical applications, the maximum data rate is about 240 kb/s [15]. Therefore, the proposed circuit has met the demands of many biomedical applications. Table I reveals the performance com-

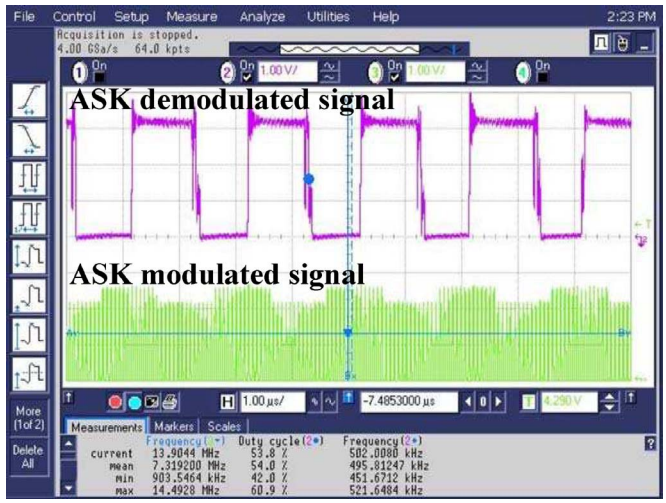

Fig. 7. Measurement waveform of the proposed ASK demodulator with data rate = 1 Mb/s and carrier frequency = 13.56 MHz.

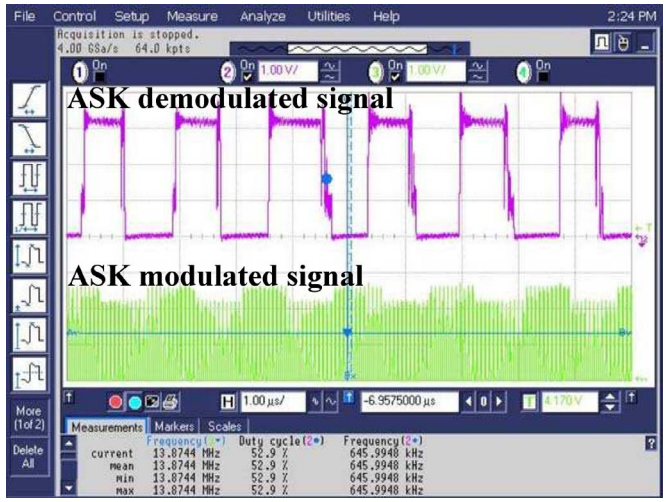

Fig. 8. Measurement waveform of the proposed ASK demodulator with data rate = 1.2 Mb/s and carrier frequency = 13.56 MHz.

parison with several prior works. The figure of merit (FOM) is defined as

$$\text{FOM} = \frac{\text{Data rate}}{\text{Gate count} \times \text{Power} \times \text{Core area}}. \quad (8)$$

Without using any passive element, the area of the proposed design is more compact. By (8), the proposed ASK demodulator has the best FOM, compared to all of the prior works.

IV. Conclusion

A novel ASK demodulator has been proposed in this brief. Without any passive element, the chip size has been drastically reduced. The maximum data rate of 1.2 Mb/s has been achieved, which is far more than enough to be used in a variety of low ISM band applications. The proposed design is very compact for wireless biomedical implants, as well as other portable wireless communication systems.

TABLE I
SPECIFICATION OF THE PROPOSED ASK DEMODULATOR

	Year	Process (μm)	Passive element	Gate count	Carrier freq. (MHz)	Data rate (Kbps)	Power (mW)	Core area (μm^2)	FOM ($\frac{\text{Kbps}}{\text{mW}\cdot\mu\text{m}^2}$)
[7]	2004	0.35	1 R	17	2	10	23.9	12700	0.0194×10^{-4}
[11]	2007	0.35	0	12	2	20	1.01	3025	5.45×10^{-4}
[12]	2007	0.35	0	>19	10	2000	0.084	N/A	N/A
Ours	2009	0.35	0	15	13.56	1200	0.306	3300	792×10^{-4}

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