A Transceiver Front End for Electronic Control Units in FlexRay-Based Automotive Communication Systems

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***Abstract*—This paper presents an in-car networking transceiver front end that is compliant with FlexRay automotive electronic standards. A low-voltage differential-signaling-like transmitter is proposed to drive the twisted pair of the bus. Furthermore, a three-comparator scheme is used to carry out bit slicing and state recognition at the receiver end. In order to resist process and temperature variation, a 20-MHz clock generator with process, supply voltage, and temperature compensation is proposed in this paper. A prototype system as well as a chip implemented by using a typical 0.18 μm single-poly six-metal CMOS process is reported in this paper. The proposed prototypical transceiver front end has been tested by the thermo chamber and a FlexRay development board to certify its operation in the $[-40\ ^{\circ}\mathrm{C} - +125\ ^{\circ}\mathrm{C}]$ temperature range and FlexRay standards. The power consumption of the whole chip is 43.01 mW at a 10 Mbit/s throughput. The core area of this design is 0.117 mm^2. The maximal throughput of the proposed prototypical transceiver front end can reach 40 Mbit/s.**

***Index Terms*—Automobile electronic, FlexRay, in-car networking, low power, transceiver.**

I. Introduction

CAR ELECTRONICS has been deemed as the fourth "C" right after computer, communication, and consumer electronics. Many novel electronic devices have been introduced and installed in recently publicized cars. Therefore, an in-car network has been proposed to control and supervise all of the automobile electronics. Owing to the fast evolution of semiconductor technology, devices with an electronic control unit (ECU) have been installed in automobiles. In 1990, the average quantity of ECUs in an automobile was 14. By now (2008), the number of ECUs reaches 40 to 60. Notably, certain luxury automobiles can even have over 100 ECUs. According to the prediction of the marketing research institution Gartner, the market scale of global automobile-used ECU will grow up to $5300 million in 2008 and grow up to $6300 million further in 2012.

Manuscript received July 14, 2008; revised December 18, 2008. First published June 02, 2009; current version published February 10, 2010. This work was supported in part by the National Science Council, Taiwan, under Grant NSC 96-2628-E-110-018-MY3 and in part by the Ministry of Economic Affairs under Grant 97-EC-17-A-01-S1-104. This paper was recommended by Associate Editor: P. K. T. Mok.

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Digital Object Identifier 10.1109/TCSI.2009.2023932

The FlexRay standard [1] is designed for in-car networks. It will not replace existing networks. By contrast, it can combine or integrate with these networks, including controller area network, local interconnection network [2], Media Oriented System Transport [3], [4], J1850 protocol [5], etc. FlexRay requires 10 Mbit/s data rate in either one of the two channels of an ECU. If a single channel is used alone, the total data rate should reach 20 Mbit/s. Therefore, even the video signals, multimedia, and control signals can communicate via the FlexRay system with such a high-bandwidth benefit. The goal of FlexRay is that the automobile is X-by-wired ($\mathrm{X} = \mathrm{steer}$, brake, accelerate, audio/video, safety, etc.), i.e., all of the current machine-based mechanisms, e.g., steer, brake, accelerate, etc., can be controlled by electronics through FlexRay-based networks. Fig. 1 shows a scenario when FlexRay is used in a car. Notably, different networking systems can be integrated by the FlexRay backbone.

As well known by car industry and business, "safety" and "reliability" are the primary design requirements. Otherwise, we can put it another way: "fault tolerance" is a must. Therefore, instead of using some novel or even radical design or circuitry, it is better to select well proven but a little bit old designs to ensure safety and reliability. The major contribution of this work is that we successfully integrate several prior circuits with our circuitry and make them work and function together to meet the requirements set by FlexRay standards.

II. Transceiver Front-End Design for In-Car Networking Systems

Fig. 2 shows the block diagram of ECU nodes in a FlexRay system. The component of each node contains a host microcontroller (μC), a communication controller (CC), a bus guardian, and two bus drivers (BDs). Traditionally, the transceiver front end in the BD should be implemented by a high-voltage silicon process [6], [7]. However, our design can be implemented by a typical 0.18 μm mixed-signal CMOS process instead. Hence, the proposed design can be integrated with other digital blocks easily besides the advantage of reduced cost.

According to the FlexRay standards [1], there are two signals of the BD, denoted as Bus Plus (BP) and Bus Minus (BM). BP and BM are, in fact, a pair of differential signals which can reduce the noise on a connection by rejecting common-mode interference and have tolerance of ground offsets. The timing and amplitude characteristics of BP and BM required by the FlexRay standards are shown in Fig. 3.

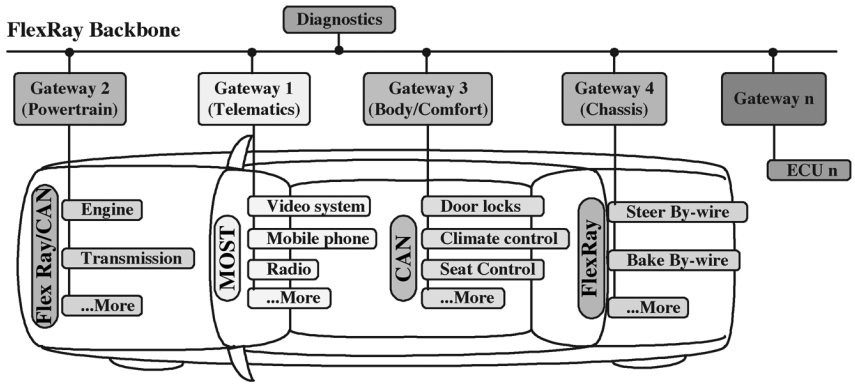

Fig. 1. FlexRay used as an in-car network.

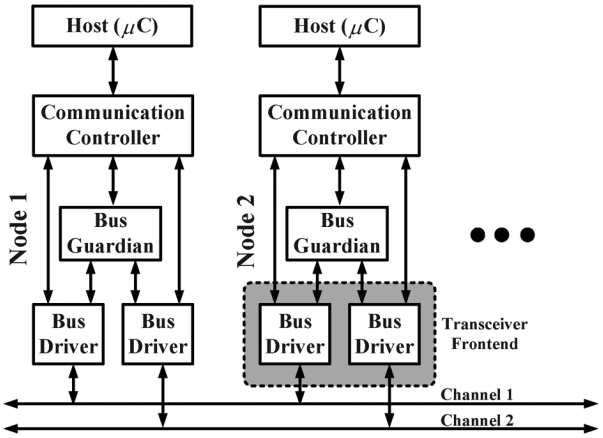

Fig. 2. Block diagram of ECU nodes in a FlexRay system.

TABLE I
FUNCTIONS OF THE CONTROL SIGNALS, BP, AND BM

Control signal of transmitter	Differential signal of BP	Differential signal of BM
Data0	Low	High
Data1	High	Low
Idle	Idle_bias[1]	Idle_bias
Idle_LP	Idle_LP_bias[2]	Idle_LP_bias
Differential signal on the bus	**Rdata**	**Ridle**
Data0	Low	Low
Data1	High	Low
Idle	High	High
Idle_LP	High	High

The block diagram of the proposed design is shown in Fig. 4, including the regulators, a transmitter (Tx) circuit, and a receiver (Rx) circuit. $\mathrm{Data0\_C}$, $\mathrm{Data1\_C}$, $\mathrm{Idle\_C}$, and $\mathrm{Idle\_LP\_C}$ are one-hot decoded control signals for the Tx to transmit the data and the state. On the other hand, Rdata and Ridle are control signals generated by the Rx after the received differential signals are recovered and decoded. The functions associated with those control signals and the differential-bus signals are summarized in Table I.

A. Tx

There are a total of four types of "Signals" in the FlexRay systems, which are the $\mathrm{Data\_1}$ Signal and $\mathrm{Data\_0}$ Signal in the Active State, and the $\mathrm{Idle\_LP}$ Signal and Idle Signal in the Idle State. We propose a low-voltage differential-signaling (LVDS)-like Tx design as shown in Fig. 5. LVDS is a differential-signaling scheme, which means that it transmits two different voltages that will be compared at the Rx. LVDS utilizes the voltage difference between the two wires to encode the information [8], [9]. In the proposed Tx design, $\mathrm{Data0\_C}$, $\mathrm{Data1\_C}$, $\mathrm{Idle\_C}$, and $\mathrm{Idle\_LP\_C}$ are control signals decoded by a one-hot decoder and fed into the BD. $\mathrm{Data0\_C}$ and $\mathrm{Data1\_C}$ are a pair of digital differential signals generated by a CC to notify the bit to be transmitted over the bus. $\mathrm{Idle\_C}$ and $\mathrm{Idle\_LP\_C}$ are a pair of idle signals. When the $\mathrm{Idle\_C}$ is asserted, BP and BM must be locked on the same Vref, which is 2 V in this work. By contrast, as soon as the $\mathrm{Idle\_LP\_C}$ is asserted, indicating that the low-power mode is chosen, then BP and BM are pulled down to GND. Notably, VDD denotes that the supply voltage is 3.3 V. En and EnB are enable and disable signals, respectively, generated by $\mathrm{Idle\_C}$ and $\mathrm{Idle\_LP\_C}$ to select the gate drives of M101, M102, M103, and M104. The relationship between the control signals BP and BM is presented in Table I. For instance, if $\mathrm{Data1\_C} = 1$, $\mathrm{Data0\_C} = 0$, $\mathrm{Idle\_C} = \mathrm{Idle\_LP\_C} = 0$, then $\mathrm{En} = 0$ and $\mathrm{EnB} = 1$ such that M103 and M102 are both turned on, which will pull down BM and pull up BP to generate $\mathrm{Data\_1}$ signal. Then, logic "1" is transmitted.

In order to conform to all the required specifications of the FlexRay standards with rigorous automotive environmental temperature, the dimensions of the MOSs are selected carefully after thorough simulations. For the same reason, the variation of differential voltages caused by the process, supply voltage, and temperature (PVT) should be taken into account. Similarly, the rejection to the process and temperature drifting can be achieved by tuning the aspect of each transistor. The derivation steps of each transistor size is described as follows.

First of all, we select 0.8 V as the voltage difference between the central voltage and the maximal voltage of each differential signal, which is compliant with the FlexRay standards, as shown in Fig. 3. According to the FlexRay specifications, the physical bus wire should be loaded with a small resistor of 40 or 45 Ω in parallel with a large capacitor of 100 pF. Therefore, the current

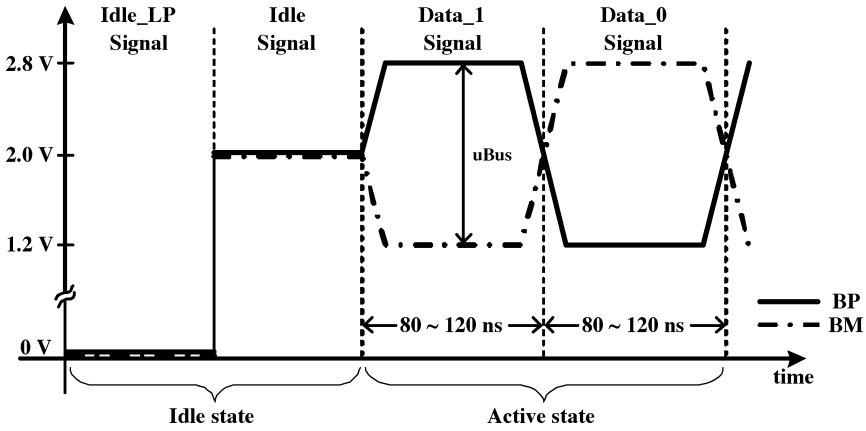

Fig. 3. Characteristics of BP and BM required by FlexRay standards [1].

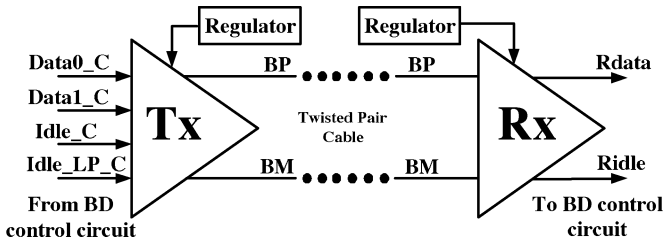

Fig. 4. Block diagram of the proposed design.

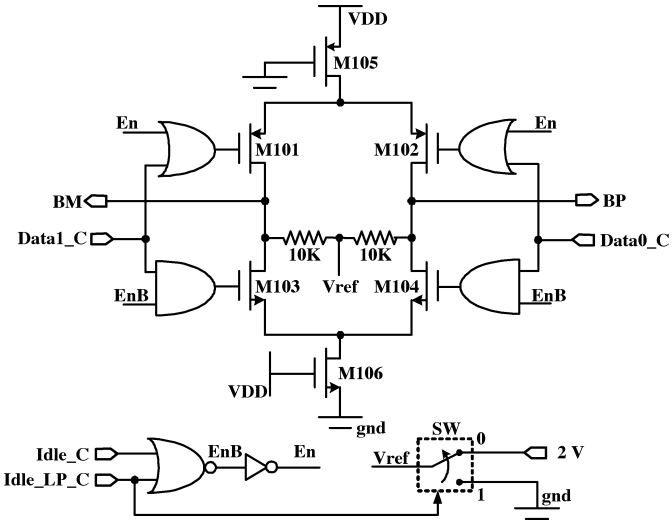

Fig. 5. Schematic of the proposed Tx

(I) through the load, given the control voltage, could be estimated roughly by (1)

$$I = \frac{0.8\ \text{V} \times 2}{40\ \Omega} = 0.04\ \text{A} = 40\ \text{mA}. \tag{1}$$

Referring to the drain current in (2), we can estimate the dimension of each transistor, where $V_{\text{GS}} = 3.3$ V, $V_{\text{DS}} = 2 - 0.8 = 1.2$ V, and the channel-length-modulation factor, denoted as λ, is assumed as 0.01 by using at least five times of the feature length. Notably, the process parameters are tabulated in Table II, i.e.,

$$I_{\text{DS}} = \frac{1}{2}\mu C_{\text{ox}}\frac{W}{L}(V_{\text{GS}} - V_{\text{th}})^2(1 + \lambda V_{\text{DS}}) \tag{2}$$

TABLE II
PARAMETERS FROM FOUNDRY

Demanded Parameter	Values
V_{thN0}	0.741
V_{thP0}	-0.697
μ_{N0}	0.040
μ_{P0}	0.013
t_{oxn}	6.80×10^{-9}
t_{oxp}	6.77×10^{-9}

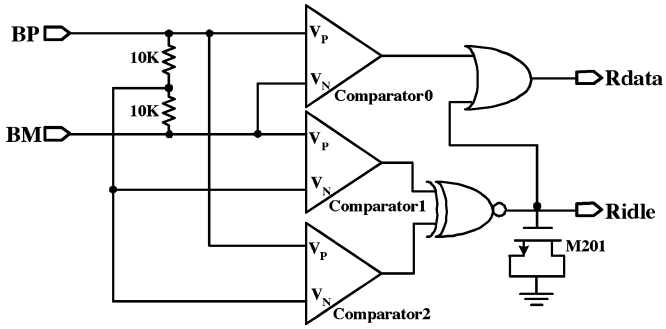

Fig. 6. Schematic of the proposed Rx.

where μ is the mobility of the MOS, C_{ox} is the oxide capacitance which is given as $\varepsilon_{\text{ox}}/t_{\text{ox}}$, and V_{th} is the threshold voltage.

Considering environmental temperature and reliability, several factors that might affect the characteristics of (2) should be taken into account. Two of the most critical parameters that vary with temperature are the mobility of the charge carriers and the threshold voltage. The variation of these two factors are shown in (3) and (4), respectively, where the temperature coefficient $\alpha_{V_{\text{th}}}$ is negative [10], [11]. Other major factors affecting the threshold voltage and the mobility are variations of gate-oxide thickness and doping concentrations.

$$\mu \propto T^{-2.2} \tag{3}$$

$$V_{\text{th}}(T) = V_{\text{th0}} - K(T - T_0) = V_{\text{th0}}(1 + \alpha_{V_{\text{th}}}T). \tag{4}$$

Process variation mainly due to variations in gate-oxide thickness and doping concentrations might also slightly affect the threshold voltage and the mobility of the MOS transistor.

The mismatch between the raising time and the falling time of the differential signals are also defined strictly ($\leq$4 ns) which

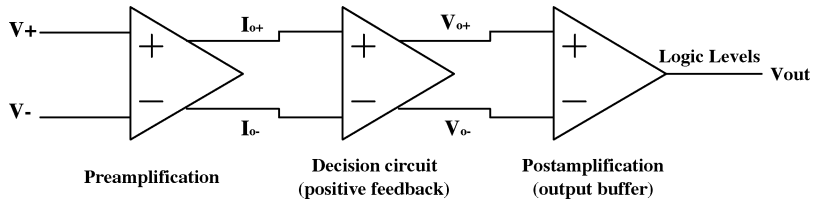

Fig. 7. Block diagram of the comparator.

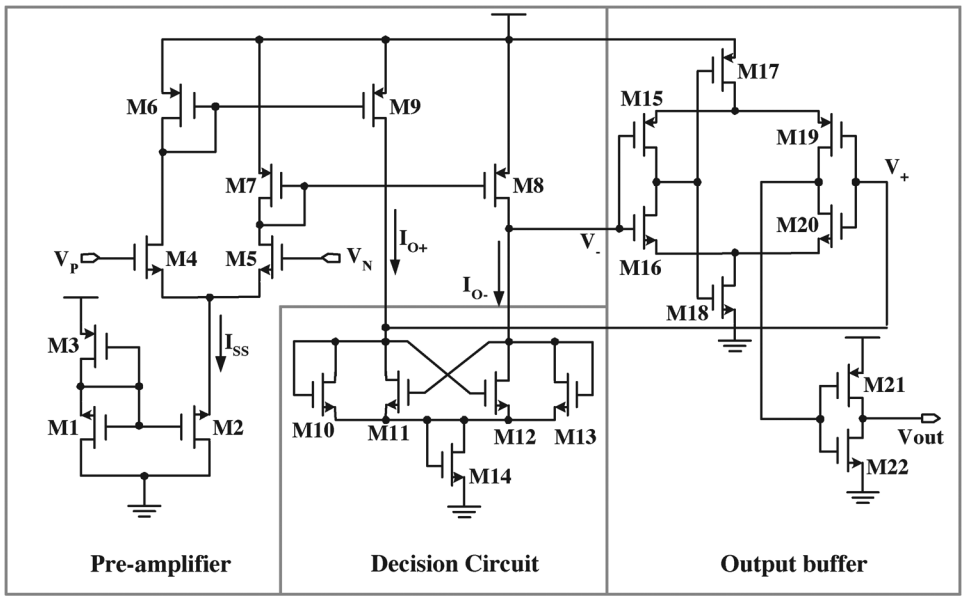

Fig. 8. Schematic of the comparator.

means that the aspect ratio of the p-type and n-type transistors should be carefully selected. By iteratively employing the operating point analysis and simulation, accurate dimensions of each MOS transistor can be derived.

B. Rx

Apart from the Rx circuits' design of traditional buses, the Rx for FlexRay systems must recognize the Idle State besides slicing the received bits. Therefore, we propose a three-comparator scheme to achieve the required functions. Comparator0 is used to determine if $\mathrm{Data\_0}$ or $\mathrm{Data\_1}$ is in the Active State. Comparator1 and Comparator2 are used to detect whether the input signals on the bus are in the Idle State or not. For instance, if $\mathrm{BP} = \mathrm{BM}$, the outputs of Comparator1 and Comparator2 are reversed and Ridle is asserted. Meanwhile, the Rdata is asserted as well. Then, the Rx is able to recognize the Idle State on the bus. The source–drain (S-D) connected MOS M201 is used as a capacitive filter to remove the glitches that occurred resulting from switching between Comparator1 and Comparator2. Fig. 6 shows the schematic of the proposed Rx.

These three comparators are constructed by low-power comparator circuits [12]. The circuit mainly consists of three blocks: Preamplification, Decision circuit, and Output buffer, as shown in Fig. 7. Fig. 8 shows the schematic of the comparator. A differential pair and active loads are used to achieve the Preamplification function. The Decision circuit needs to distinguish in a few millivolt level the difference between the differential inputs in order to have a high precision. Therefore, the resolution of the output currents of the preamplifier is critical. By (5), we attain the output currents I_{O+} and I_{O-} of the first stage, where I_{SS} is set to 20 μA and g_m is the transconductance of transistor M11.

$$I_{O+} = \frac{g_m}{2}(V_+ - V_-) + \frac{I_{SS}}{2} = I_{SS} - I_{O-} = 20\,\mu A - I_{O-}. \quad (5)$$

The Decision circuit needs to distinguish in a few millivolt level the difference around the GND voltage in order to have a high precision. We use a positive feedback network composed of M11 and M12 to increase the gain of the Decision circuit.

If $I_{O+} \gg I_{O-}$, $\beta_{10} = \beta_{13} = \beta_A$, and $\beta_{11} = \beta_{12} = \beta_B$, where β_{10}, β_{11}, β_{12}, and β_{13} are the β's of M10, M11, M12, and M13, respectively, then transistor M10 and M12 are turned on, and M11 and M13 are turned off. We can derive T_{V+} by (6), where V_{thn} is the threshold voltage of the NMOS.

$$T_{V+} = \sqrt{\frac{2I_{O+}}{\beta_A}} + V_{\mathrm{thn}}. \quad (6)$$

When I_{O-} increases and I_{O+} decreases at the same time, the output voltage of the Output buffer will be inverted, given that the gate voltage of M7 is equal to V_{thn} of M6. In the meantime, the drain current of M11 increases, and the drain current of M10 decreases. Then, M12 will be turned off because the V_{DS} of M10 decreases. Then, we can derive the I_{O-} as follows:

$$I_{O-} = \frac{\beta_B}{2}(T_{V+} - V_{\mathrm{thn}})^2 = \frac{\beta_B}{\beta_A} \cdot I_{O+}. \quad (7)$$

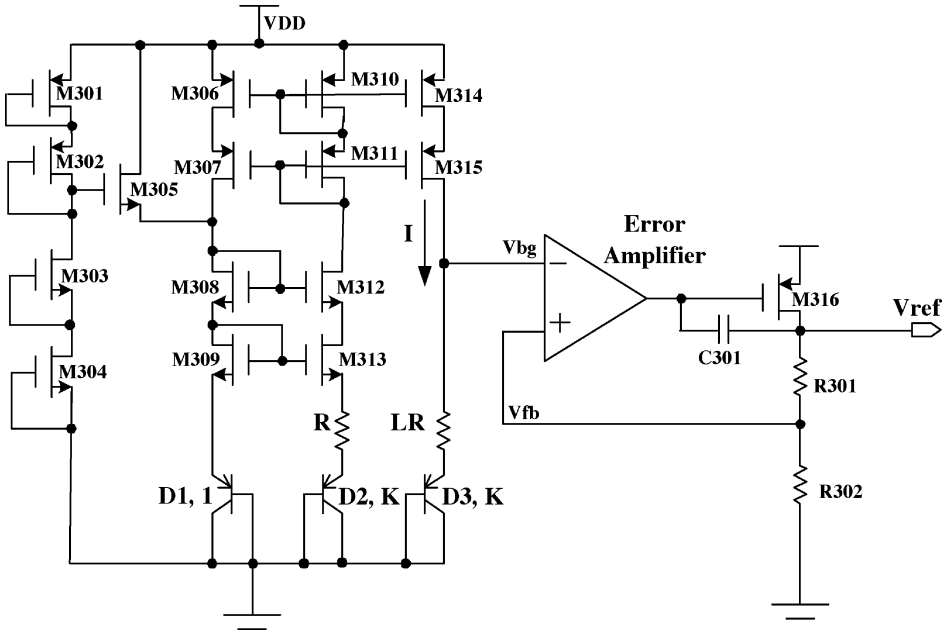

Fig. 9. Schematic of the voltage regulator.

Based on (7), if $\beta_B = \beta_A$, we can observe that the output voltage will be inverted when $I_{O+} = I_{O-}$. Besides, we can add the hysteresis effect by regulating β_A and β_B to reject the noise coupled from the power supply.

The Output-buffer stage is used to slice the output signal of the Decision circuit into digital signals. The circuit accepts a differential input signal without any limitation regarding slew rate. A self-biasing differential amplifier and an inverter are used in this Output buffer, as shown in Fig. 8. The inverter, composed of M21 and M22, increases the gain of the Output buffer and avoids the load effect of the self-biasing differential amplifier. Notably, a hysteresis design is included to reject the coupled noise.

C. Design of the Voltage Regulator

Since stable reference voltages are needed in Tx and Rx, respectively, to serve as the common-mode bias voltages in the differential signaling on the bus, we utilize a low-dropout voltage regulator to provide these stable voltages [11]. Fig. 9 shows the schematic of the voltage regulator. The regulator provides a stable voltage reference to reject the variation and noise from the supply voltage.

A bandgap bias circuit generates a PVT-independent reference voltage Vbg. The series resistors R301 and R302 monitor the output voltage by a simple voltage division. A feedback voltage Vfb is fed back to be compared with the output voltage of the bandgap circuit by an error amplifier. The error amplifier then feeds a control voltage into the pass transistor M316 to regulate the output voltage according to the difference between the feedback and output voltages of the bandgap circuit. The faster speed of the feedback loop comes along with the more stable output voltage. The loop gain of the voltage regulator feedback loop is 68.7 dB. It is measured by Vref over Vbg, given a small testing signal at Vbg.

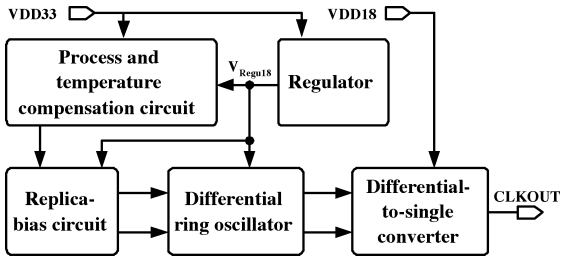

Fig. 10. Architecture of the proposed 20-MHz clock generator.

III. 20-MHz Clock Generator With PVT Compensation

When it comes to vehicle applications, reliability and safety are classified as among the most important issues. Since the time-triggered scheme is required by FlexRay systems, several conscientious and careful timing characteristics are defined. Thus, a high-precision clock generator with reliable PVT compensation is very much needed in FlexRay-based ECUs. Fig. 10 shows the architecture of the proposed 20-MHz clock generator. The regulator provides a stable voltage reference, which could reject the variation and noise from the supply voltage. A three-stage differential ring oscillator is used in this design with a replica bias circuit generating a stable bias to the active load. The last part of this design is a differential-to-single converter, which could provide a 50% duty-cycle output [13]. The compensation scheme for both process and temperature variations adopts a threshold-voltage compensation mechanism [14]. The details of each block of the proposed 20-MHz clock generator are described as follows.

A. Differential Ring Oscillator

The ring oscillator with differential delay cells is preferred due to its better substrate and supply-noise rejection capability

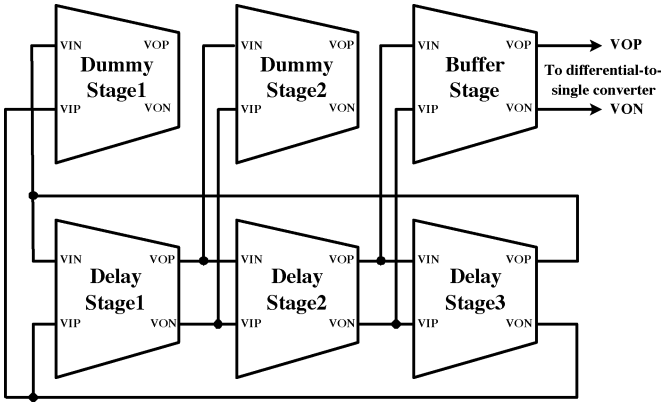

Fig. 11. Schematic of the three-stage ring oscillator.

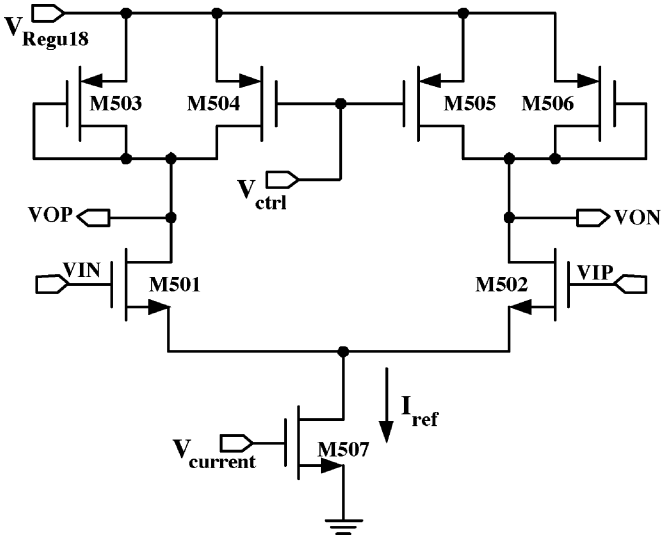

Fig. 12. Schematic of the proposed delay cell.

[15]. Fig. 11 shows the schematic of the proposed three-stage ring oscillator. The dummy and the buffer stages are used to eliminate the asymmetric loading of the delay stages caused by the differential-to-single converter.

Active load (current source) and linear loads (resistors) have been used in the differential delay cells. Amplifiers with active loads offer a better small-signal gain and a higher oscillation amplitude. On the other hand, amplifiers with linear loads provide a better large-signal power supply rejection ratio (PSRR).Fig. 12 shows the delay cell schematic of the proposed clock generator with symmetric loads: an active load (M504 and M505) and a linear load (M503 and M506). $V_{\rm ctrl}$ is a control voltage generated by the process and temperature compensation circuit through the replica bias circuit. The output swing could be adjusted by changing $V_{\rm ctrl}$. $V_{\rm current}$ is a bias voltage generated from the replica bias circuit. It provides a bias for M507 to generate the current $I_{\rm ref}$. The delay produced by the circuit is shown as follows:

$$t_d = \frac{C_{\rm out}(V_H - V_L)}{I_{\rm ref}} \tag{8}$$

where $C_{\rm out}$ is the total capacitance seen at the output of each stage. V_H and V_L are equal to $V_{\rm Regu18}$ and $V_{\rm ctrl}$, respectively.

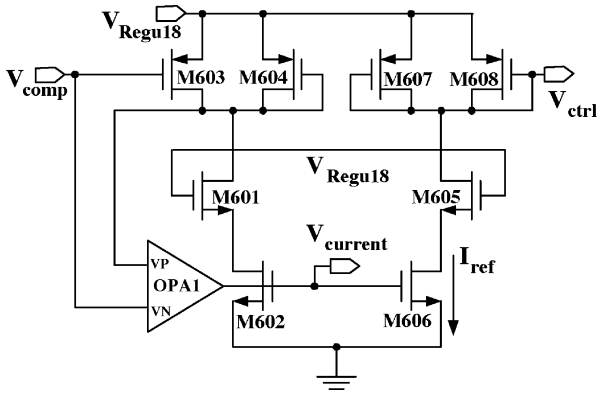

Fig. 13. Schematic of the proposed replica bias circuit.

The delay of each stage can be tuned by changing $V_{\rm current}$ or/and the output swing, which means changing $V_{\rm ctrl}$.

B. Replica Bias Circuit

To generate a constant oscillator amplitude regardless of process and temperature conditions, a replica bias circuit is used to provide the required bias voltages for each delay cell. Fig. 13 shows the schematic of the proposed replica bias circuit. $V_{\rm comp}$ is the compensation voltage generated from the process and temperature compensation circuit. A feedback bias loop using OPA1 forces the voltage drop on M604 to be equal to $V_{\rm comp}$ by tuning the current bias $V_{\rm current}$. The symmetric structure (M605 $\sim$ M608) replicates $V_{\rm comp}$ to $V_{\rm ctrl}$. The bias current could be derived approximately by using the standard square-law method, i.e.,

$$I_{\rm ref} \approx K_{604}\frac{W_{604}}{L_{604}}(V_{\rm Regu18} - V_{\rm th604} - V_{\rm comp})^2. \tag{9}$$

The delay produced and the frequency of the ring oscillator are derived, respectively, as follows:

$$t_d = \frac{C_{\rm out}(V_{\rm Regu18} - V_{\rm comp})}{I_{\rm ref}} \tag{10}$$

$$f = \frac{1}{N \cdot t_d} \tag{11}$$

where N is the number of stages in the ring oscillator, which is three in our design.

By substituting $I_{\rm ref}$ in (10) with (9), t_d is derived. Then, t_d is plugged into (11). Finally, the frequency of the ring oscillator could be expressed as a function of $V_{\rm comp}$, i.e.,

$$f \approx K_{604}\frac{(W/L)_{604} \cdot (V_{\rm Regu18} - V_{\rm th604} - V_{\rm comp})^2}{N \cdot C_{\rm out} \cdot (V_{\rm Regu18} - V_{\rm comp})}. \tag{12}$$

C. Process and Temperature Compensation Circuit

Two critical parameters that vary with temperature, namely, mobility of carriers and threshold voltage, have been mentioned in (3) and (4). Notably, the junction capacitance model in BSIM 3.3.2 [16] is usually modeled as

$$C_x = C_{x0}(1 + \alpha_{C_{x0}}T). \tag{13}$$

where the temperature coefficient $\alpha_{C_{x0}}$ is negative.

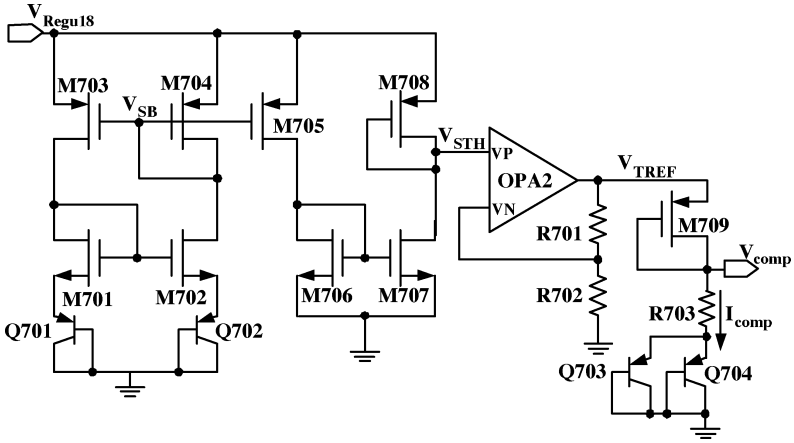

Fig. 14. Schematic of the process and temperature compensation circuit.

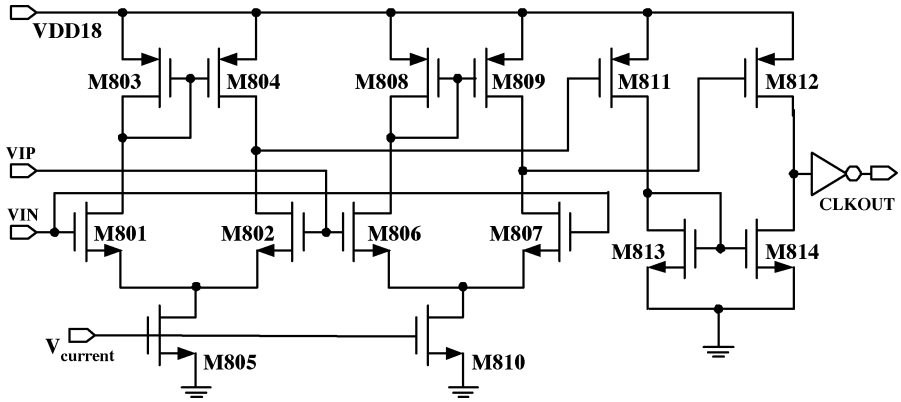

Fig. 15. Schematic of the process differential-to-single circuit.

Referring to [14], the compensated control voltage are derived approximately as follows:

$$V_{\rm comp} \approx A' - C'T \tag{14}$$

where $A' \approx V_{\rm Regu18} - V_{\rm thp0}$ with $V_{\rm thp0}$ denoting the threshold voltage of the PMOS at temperature 0 K and $C' \approx -(1/2)\cdot(f \cdot N \cdot C_{x0}/\mu C_{ox0}(W/L)_{603})$.

According to (14), the slope of the compensated control voltage is negative with respect to the temperature. By using the V_{BE} of the bipolar junction transistor (BJT), the negative slope can be realized. In other words, the linear approximation in (14) must be satisfied at all process conditions. Fig. 14 shows the schematic of the process and temperature compensation circuit. The self-bias reference $V_{\rm SB}$ provides a temperature-independent current source. M708 acts as a $V_{\rm th}$ sensor, offering a threshold-sensitive voltage $V_{\rm STH}$, with a temperature-independent current source load (M707). The amplifier OPA2 boosts the voltage $V_{\rm STH}$ to $V_{\rm TREF}$. The compensated control voltage is generated by the transistor M709, resistor R703, and the two diode-connected p-n-p transistors Q704 and Q703. By adjusting the aspect ratio of M709 and the resistor R703, the temperature slope of the control voltage $V_{\rm comp}$ can be tuned. Equation (15) shows the expression of the control voltage [11]. Replacing the current I_{comp} in (15) with the expression in (16) and assuming $\xi = (V_{\rm TREF} - |V_{\rm th709}| - 1/(R_{703}\mu C_{\rm ox}(W/L)_{709}))$, (17) is then attained [14]. The $V_{BE703,704}$ term in (17) offers the negative temperature coefficient. The proposed circuit is designed to give the required temperature slope across multiple process corners by adjusting the aspect ratio of M709 and R703.

V_{BE} varies with the collector current I_C, i.e., $|I_C| = I_S \cdot e^{V_{BE}/V_T}$, where I_S is the saturation current and V_T is the thermal voltage. However, $I_C = (1/2)I_{\rm comp} = (1/2)I_{\rm D709}$, where $I_{\rm D709}$ is the drain current of M709. Therefore, $(1/2)I_{\rm D709} = I_S \cdot e^{V_{BE}/V_T}$ is attained. Then, the equation can be rewritten as $V_{BE} = V_T \cdot \ln(I_{\rm D709}/2I_S) = V_T \cdot \ln(K_{709}(W/L)_{709} \cdot (V_{\rm TREF} - V_{\rm comp} - V_{\rm th709})^2/2I_S)$. Therefore, the V_{BE} of the BJT can be tuned by the aspect ratio of M709.

Furthermore, $V_{\rm comp}$ can be written as follows: $V_{\rm comp} = I_{\rm comp} \times R703 + V_{BE}$. Finally, by adjusting the aspect ratio of M709 and the resistor R703, the temperature slope of the control voltage $V_{\rm comp}$ can be tuned, i.e.,

$$V_{\rm comp} = V_{\rm TREF} - |V_{\rm th709}| - \sqrt{\frac{2I_{\rm comp}}{\mu C_{\rm ox}(W/L)_{709}}} \tag{15}$$

$$I_{\rm comp} = \frac{V_{\rm comp} - V_{BE703,704}}{R_{703}}. \tag{16}$$

D. Differential-to-Single Converter

Fig. 15 shows the schematic of the proposed differential-to-single converter. It is composed of two out-of-phase

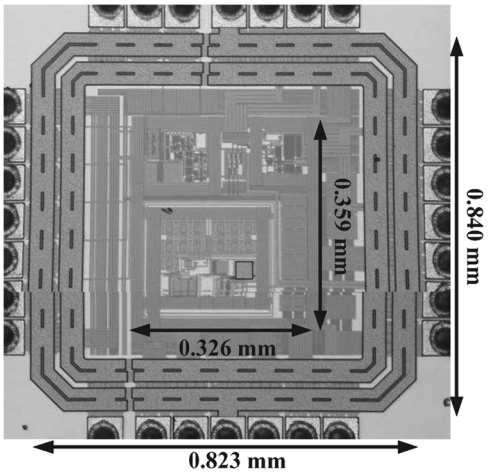

Fig. 16. Die photograph of the proposed transceiver front-end design.

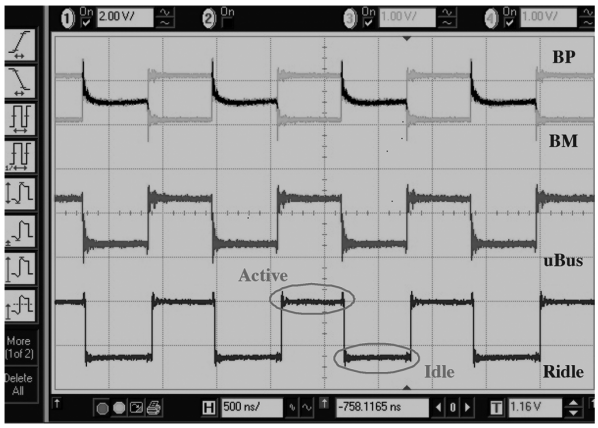

Fig. 17. Waveforms of the proposed design alternately in Active state and Idle state.

NMOS-pair differential amplifiers, two common-source PMOS amplifiers, and an output buffer. To ensure the correct common-mode input-voltage level, a pair of symmetric load buffer is used (M801 $\sim$ M809). It provides amplified signals and dc bias to the PMOS common-source amplifier (M811 and M812) with a current mirror load (M813 and M814). The signals are amplified again by these two common-source amplifiers and converted into a single-ended output signal through the current mirror. Such a two-step amplification with a large bandwidth provides the same transition time for the two differential signals. Therefore, the 50% duty cycle for the output signal is attained. Notably, the output buffer provides a sufficient output diving current, i.e.,

$$V_{\text{comp}} = \xi + \sqrt{\xi^2 - V_{\text{TREF}} - V_{\text{th709}} + \frac{2V_{BE703,704}}{R_{703}\mu C_{\text{ox}}(W/L)_{709}}}. \tag{17}$$

IV. Implementation and Measurement

The proposed design is carried out by a typical 0.18 μm single-poly six-metal CMOS technology. Verified by all-PVT-corner postlayout simulations, the throughput of the Tx and the data rate of the Rx can reach 40 Mbit/s in a single channel.

TABLE III
Measurement of the Tx in Different Temperatures

Measurement Result	-40°C	25°C	125°C
Absolute value of uBus, while sending(*)	1528 mV	1398 mV	1169 mV
Absolute value of uBus, while Idle(*)	≈30 mV	≈30 mV	≈30 mV
Transmitter delay negative edge(***)	3.189 ns	4.713 ns	4.045 ns
Transmitter delay positive edge(***)	3.709 ns	6.296 ns	5.229 ns
Transmitter delay mismatch	0.52 ns	1.583 ns	1.184 ns
Fall time differential bus voltage(**)	12.909 ns	6.911 ns	11.959 ns
Rise time differential bus voltage(**)	13.898 ns	5.147 ns	11.733 ns

TABLE IV
Measurement of the Rx in Different Temperatures

Measurement Result	-40°C	25°C	125°C
Receiver delay, negative edge(*)	22.076 ns	20.577 ns	21.033 ns
Receiver delay, positive edge(*)	19.981 ns	22.109 ns	21.914 ns
Receiver delay mismatch	2.0950 ns	1.5320 ns	0.8810 ns
Idle reaction time(*)	40.227 ns	45.007 ns	69.807 ns
Active reaction time(*)	46.710 ns	39.977 ns	32.622 ns

Fig. 16 shows the die photograph of the proposed transceiver front end on silicon. Fig. 17 shows the waveforms of the proposed design alternately in Active state and Idle state. The signals BP and BM are modulated by the proposed Tx, and the Ridle is decoded by the proposed Rx. Fig. 18 shows the shmoo plot of this work. The minimum operating supply voltage can be as low as 2.2 V, and the maximum throughput is more than 40 Mbit/s. The measurement results of Tx and Rx operation in different temperatures are shown in Tables III and IV. We ran the same measurement over 30 samples and got almost the same result. Last but not least, we physically connected our chip with a commercial TJA1080 and made them communicate with each other successfully. Fig. 19 shows the waveforms of the proposed Tx. The eye size can be measured from the output waveforms, which is 47 ns (width) $\times$ 1.4 V(height).

In the FlexRay standards, all the FlexRay physical layer devices shall support the operation under automotive environmental temperature range of $-40\ ^{\circ}\text{C} - +125\ ^{\circ}\text{C}$. A reliability test over such a wide temperature range is carried out by a thermo chamber, which is used to provide these harsh temperature suites. Fig. 20 shows the chip in the thermo chamber, and Fig. 21 shows the thermo test between $-40\ ^{\circ}\text{C} - +125\ ^{\circ}\text{C}$. Tables V and VI show the comparison of measurement results between the FlexRay specification and our Tx/Rx design. Table VII shows the clock generator comparison with the prior work [14].

A TZM FlexEntry development board is used to build a FlexRay system test environment as shown in Fig. 22. The **FlexEntry (1)** generates the standard FlexRay frames to the

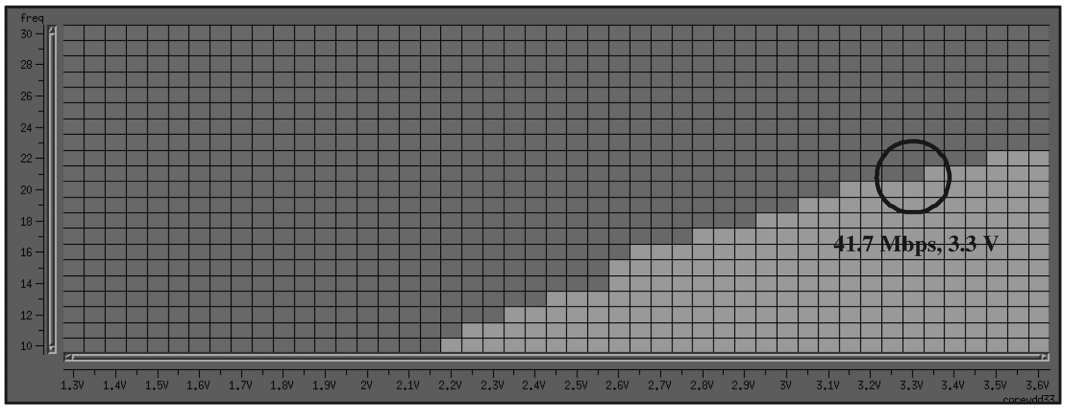

Fig. 18. Shmoo plot of the proposed design on silicon.

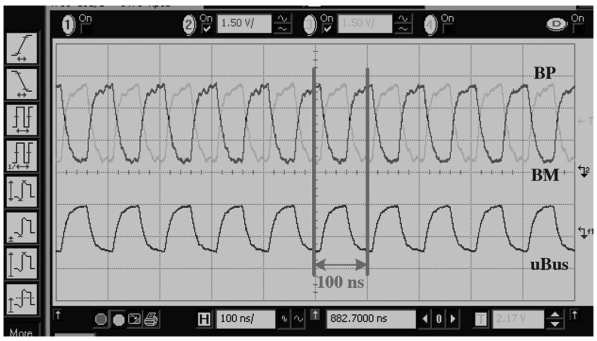

Fig. 19. Output waveforms of the proposed Tx.

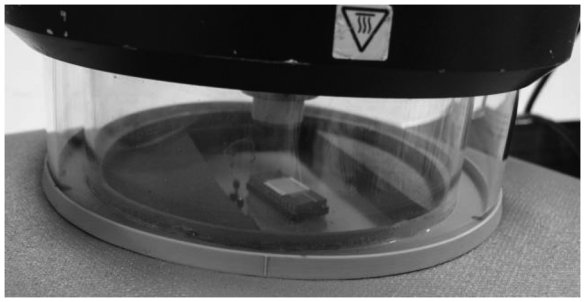

Fig. 20. Chip in the thermo chamber.

TABLE V
COMPARISON OF FLEXRAY STANDARDS AND THE PROPOSED TX

FlexRay Tx Specification		Measurement Result	[20]
Absolute value of uBus, while sending(*)	600∼2000 mV	1380 mV	1600 mV
Absolute value of uBus, while Idle(*)	0∼30 mV	≈30 mV	25 mV
Transmitter delay, negative edge(***)	$<$ 100 ns	13.32 ns	31 ns
Absolute value of uBus, positive edge(***)	$<$ 100 ns	13.29 ns	32 ns
Transmitter delay mismatch	$<$ 4 ns	0.029 ns	1 ns
Fall time differential bus voltage(**)	5∼25 ns	7.581 ns	12 ns
Rise time differential bus voltage(**)	5∼25 ns	5.686 ns	12 ns
Throughput	10 Mbps	41.76 Mbps	10 Mbps

TABLE VI
COMPARISON OF FLEXRAY STANDARDS AND THE PROPOSED RX

FlexRay Rx Specification		Measurement Result	[20]
Receiver delay, negative edge(*)	$<$ 100 ns	9.492 ns	28 ns
Receiver delay, positive edge(*)	$<$ 100 ns	9.065 ns	30 ns
Receiver delay mismatch	$<$ 5 ns	0.427 ns	2 ns
Data Rate	10 Mbps	41.74 Mbps	10 Mbps

TABLE VII
COMPARISON OF CLOCK GENERATORS

	[14]	Ours
Frequency achieved	7.02 MHz	20.05 MHz
Temperature variation	0.84%	0.84%
Process variation	2.12%	1.29%
Supply voltage variation	0.31%	0.14%
Worst case variation	2.64%	2.98%
Duty cycle	49.6% $\pm$ 2.4%	48.6% $\pm$ 1.05%

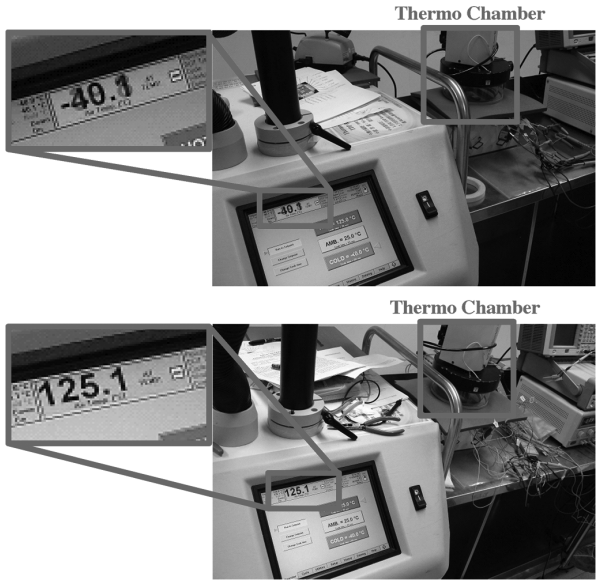

Fig. 21. Thermo test between $-40\,^{\circ}\mathrm{C}-+125\,^{\circ}\mathrm{C}$.

proposed Rx via **uBus (1)**. The proposed Rx transforms the differential signals into digital signals and passes it to the proposed Tx directly. At the same time, the proposed Tx generates a pair of differential signals and passes it to **FlexEntry (2)** via **uBus (2)**. Notably, the measured data frames on **uBus (1)** and **uBus (2)** are exactly the same, as shown in Fig. 23. The input

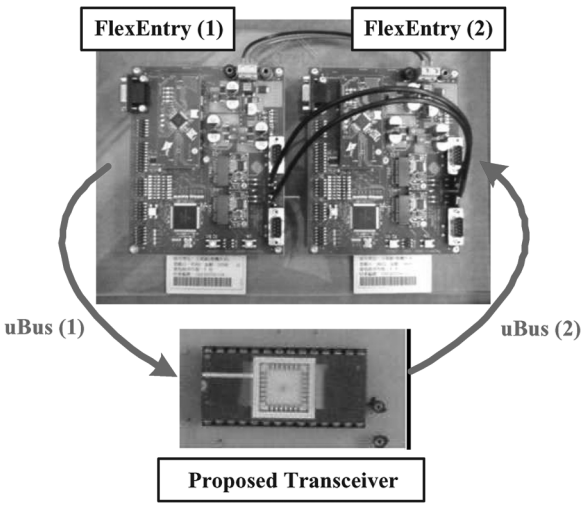

Fig. 22. Test environment of the FlexRay system and our design.

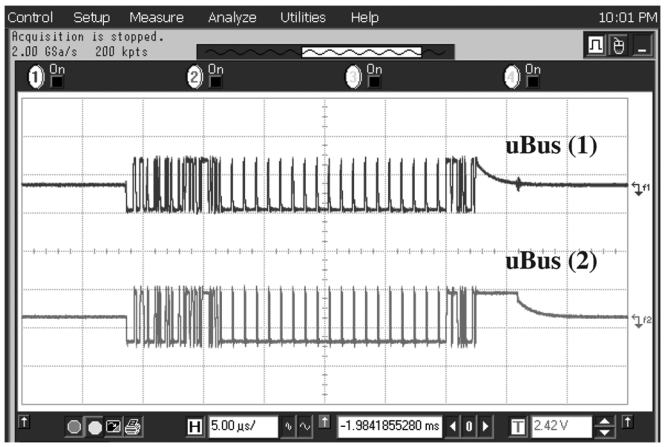

Fig. 23. Input and output signals of the proposed transceiver front end.

Fig. 24. Input and output signals of FlexEntry development board.

signal "TxD" of **FlexEntry (1)** and the output signal "RxD" of **FlexEntry (2)** shown in Fig. 24 are also identical. Therefore, we conclude that the functions of the proposed transceiver front end is compliant with the FlexRay standards.

V. Conclusion

In this paper, we have proposed a transceiver front-end design which can be used in a FlexRay-based automotive system. The design is implemented in a typical TSMC 0.18 μm mixed-signal CMOS process, which justifies the integration feasibility of various ECUs. The prototype device was fabricated and measured in rigorous automotive environmental temperature conditions. Our design is proven to be compliant with the FlexRay standards.

Acknowledgment

The authors would like to thank CIC of NSC for their professional chip-fabrication service, and the NXP Semiconductors (Taiwan) Ltd. for their strong support of the thermo chamber equipment.

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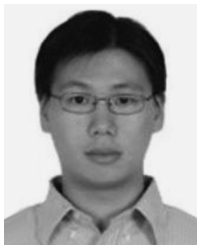

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