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High-PSR sync separator for TV signals

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Abstract This paper presents a novel NTSC video sync separator (NSS) with a high-PSR (power supply rejection) bias generation circuitry (BGC) which comprises a temperature compensation circuitry. The proposed BGC utilizes step-down regulators and a bandgap-based bias with cascode current control. The clamping voltages required for sync separation from an NTSC signal are generated. Detailed PSR analysis of the proposed BGC is also derived to circumscribe the clamping voltage variation. The proposed design is carried out using 0.35 μm 2P4M CMOS process. The measurement results verify that the HSYNC, the composite signal, and the Line 21 caption data can be separated successfully even if a 1 V noise is coupled in the supply voltage. The measured power consumption of the proposed chip is 31.92 mW.

Keywords NTSC · TV · Wireless network · Line 21 · PSR

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1 Introduction

Video decoders for NTSC TV products, e.g., [6], heavily rely on precise clock sources, particularly HSYNC, VSYNC, color burst, even/odd field, and back porch [3], [5]. However, these clock sources built in the TV-related products, particularly the compact hand-held or mobile TVs, will be drastically affected by the ambient temperature as well as the highly unreliable power supplies. Those mentioned clock signals existing in the NTSC composite signals might not be extracted correctly. On top of that, the generated heat will be very likely to drift the clock edges if there is no compensation mechanism. Severe damages are possibly made, e.g., fuzzy image and ghost shadow problems. Lots of work have been done to develop design methods of the NTSC sync separation circuitry. Most of the product datasheets, e.g., [5], were focused on the functionality of video signal processing. On the other hand, most of the related prior works were focused on either the bandgap designs [1, 4], or simple clock generations [6, 9, 10]. A fact which has been long ignored is that the hostile environment jeopardizes the clock locking and the voltage clamping of a video decoder [11]. Besides, the peak-to-peak amplitude of the received NTSC signals, called V_{pp}, will vary drastically. A temperature-insensitive bias generation circuitry, thus, is required to provide stable reference voltages for clock tracking, data slicing, and noise rejection. Hence, we present an NTSC sync separator

with a robust temperature-insensitive bias with high PSR (power supply rejection) comprising regulators and a reference voltage generator to resolve the mentioned problems. Moreover, a system clock is also generated for the following DSP (digital signal processing) core. The caption data carried in the Line 21 of the NTSC signal is also separated by the proposed design.

2 Robust NSTC sync separator

Although Electronic Industries Alliance (EIA) has announced that the V_{pp} of the NTSC signal is set to 140 IREs [3], the amplitude of V_{pp} might still be affected seriously in hostile environments [5]. Besides, the power supply voltage is likely to be an unreliable source, particularly in those hand-held TV sets. However, several clamping voltages are needed to extract the clock information in the received NTSC signal such that the peak white, black level, clip level, and sync tips can be correctly extracted and separated. The architecture of the proposed sync separator is shown in Fig. 1. The bias voltages generated by the High-PSR Bias are fed to OSC as well as Sync Generator. OSC is in charge of generating a stable clock, which is set to 12.0 MHz in this work, to the following DSP core. On the other hand, the digital to analog converter (DAC) converts digital signals from the DSP core into a voltage which is monitored by auto-gain control (AGC) to dynamically adjust threshold voltages required in the Clamper block.

2.1 High PSR bias generator

The performance of the entire NSS highly depends upon the sensitivity of the bias, i.e., High-PSR Bias in Fig. 1. The proposed bias circuit comprising two cascaded regulators, and a bandgap bias (BB) with high PSR, is proposed to resolve the difficulty of generating the required clamping voltages.

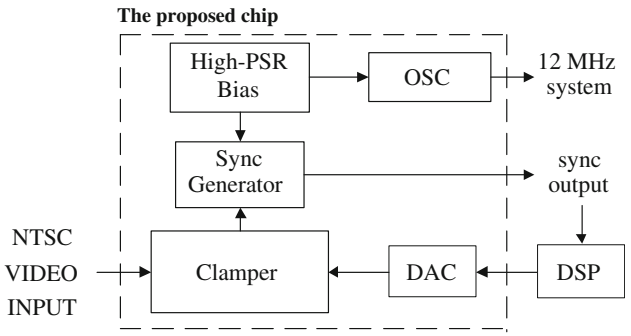

Fig. 1 Architecture of the proposed NTSC sync separator

The temperature independent bias generated by the BB, called V_{ref}, is fed into the plus input of the OP-AMP in Regulator 1 as well as the minus input of the OP-AMP in Regulator 2. Meanwhile, the BB also supplies a pair of bias voltages, V_{C1}, V_{C2}, to control the gate drives of the cascode pair in Regulator 1 which in turn stabilizes the source current (tail current) of the built-in OP-AMP (A_{OP2}) in Regulator 1, as shown in Fig. 2 and Fig. 4.

2.2 High PSR bandgap

The bandgap reference, i.e., BB, is shown in Fig. 3. Notably, the cascode configuration comprising PM31, PM32, PM33, PM34, PM35, and PM36, and the feedback loop consisting of OP-AMP A_{OP1} and NM31 are employed to resist the noise coupled with the power supply, VDD. The output impedance from V_{ref} looking into the drain of PM34 will be increased to around $g_m r^2_o$ at the sacrifice of the "headroom" of the output swing. However, since the the circuitry is aimed at the clamping voltage generation

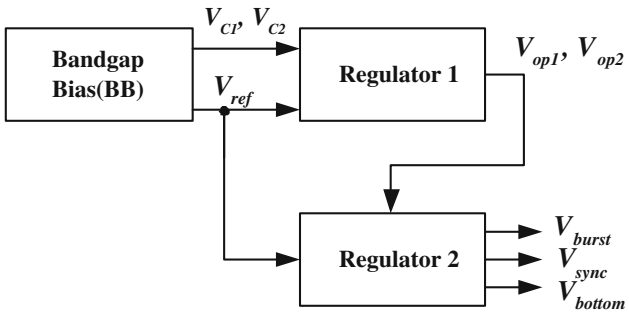

Fig. 2 The proposed high-PSR bias circuit

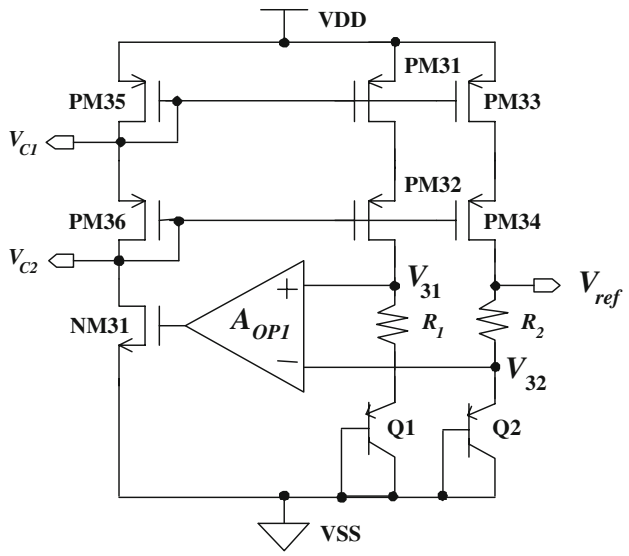

Fig. 3 The bandgap reference

which is usually below 2.0 V, it will not cause any problem. Meanwhile, A_{OP1} monitors the voltage difference between node V_{31} and V_{32} to control the current via NM31, which in turn stabilizes the voltage of the PMOS cascode configuration, V_{C1} and V_{C2}.

Assume A_1 and A_2 are the area of the BJTs, Q_1 and Q_2, respectively. The expected V_{ref} is analyzed as follows.

$$V_{ref} = I_2 \times R_2 + V_{EB2} = V_{EB2} + L \times V_T \times \ln(K), \quad (1)$$

where K is the BJT area ratio, i.e., A_1/A_2, the ratio of R_2/R_1 is assumed to be L. Hence, the bandgap reference can be pre-determined by tuning L and K.

2.2.1 PSR analysis

Since the NM31 acts as a current subtractor to control the gate drives of PM32, PM34, and PM36, we simply analyze the voltages applied to the plus and minus inputs of the OP-AMP A_{OP1} to find out the PSR which is defined as: $V_{32} = \frac{\frac{1}{g_{mQ_2}}}{R_2+\frac{1}{g_{mQ_2}}+g_{mp}r_{op}^2} \times VDD$, $V_{31} = \frac{R_1+\frac{1}{g_{mQ_1}}}{R_1+\frac{1}{g_{mQ_1}}+g_{mp}r_{op}^2} \times VDD$, where g_{mQ_1} and g_{mQ_2} denotes the transconductance of Q_1 and Q_2, respectively, g_{mp} and r_{op} represents the transconductance and the output impedance of the PMOS transistors in the cascode configuration. Thus, the PSR is found to be,

$$PSR \approx \frac{VDD}{V_{32} - V_{31}} \times \frac{1}{A_{OP1}} \approx \frac{1}{\frac{R1}{g_{mp}r_{op}^2}} \times \frac{1}{A_{OP1}} \quad (2)$$

The A_{OP1} is supposed to be an ideally large gain to avoid other side effects. Hence, we can reduce $\frac{R_1}{g_{mp}r_{op}^2}$ to increase the PSR by a small R_1 and a cascode configuration.

2.2.2 Cascaded regulators

One of the most efficient approaches to avoid the effects of unstable power supplies is to employ step-down bandgap-referenced voltage regulators to supply a temperature independent reference voltage, V_{ref}, to the rest of the circuitry [10]. Since the received V_{pp} might be as low as 2.0 V, the generated V_{ref} should be no higher than this lower bound. Referring to Fig. 4, Regulator 1 is composed of PM41, PM42, NM41, R_0, R_L, and OP-AMP A_{OP2}. A_{OP2} is shown in Fig. 5, where the V_{C1} and V_{C2} are supplied by the bandgap reference.

Notably, PM41 and PM42 are cascoded to provide a high output impedance and two stable reference voltages, V_{P41}, V_{P42} to the following OPA Bias Generator (OBG). With large $\frac{\partial I_{o1}}{\partial V_{o1}}$ (V_{o1} is the voltage at NODE A.), the loading effect at NODE A can be reduced. Assume R_{out1} is the output impedance from OBG looking into NODE A.

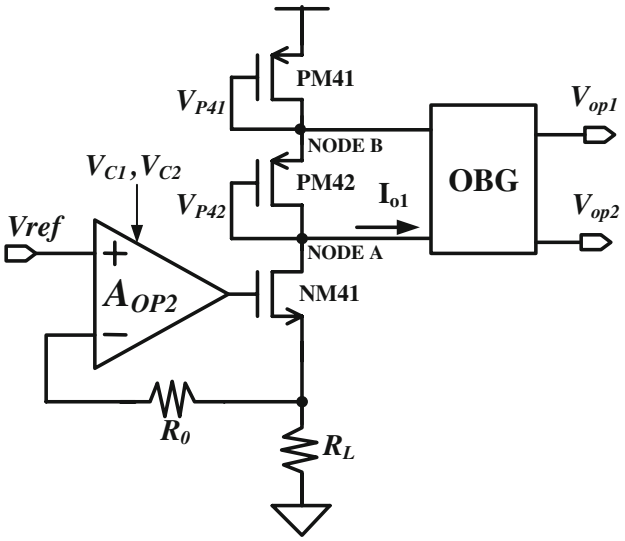

Fig. 4 The circuitry of Regulator 1

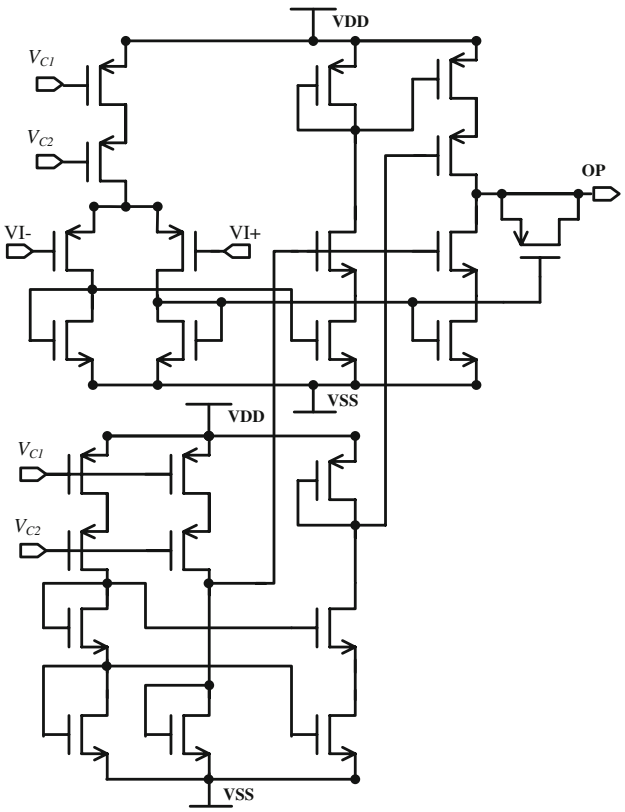

Fig. 5 The circuitry of A_{OP2}

g_{m_PM41} and g_{m_PM41} are the transconductances of PM41 and NM41, respectively. Since PM41 and PM42 are sized equally, the transconductance of PM42 is equal to $g_{m_{PM41}}$. The relationship between $\frac{\partial I_{o1}}{\partial V_{o1}}$ and R_{out1} can be derived as: $\frac{\partial I_{o1}}{\partial V_{o1}} = \frac{1}{R_{out1}}$. NM41 has become a Common Source amplifier with source degeneration in the small-signal AC model. Besides, the output impedance of A_{OP2}, r_{oA2}, is relatively

small compared to the gate impedance of NM41. We then can easily derive the impedance looking A node from OBG as $R_{out1} \approx \frac{2}{g_{m_{PM41}}} \parallel (1 + g_{m_{NM41}}(R_o \parallel R_L)) \cdot r_{o_{NM41}} \approx \frac{2}{g_{m_{PM41}}} \parallel (g_{m_{NM41}} \cdot r_{o_{NM41}} \cdot (R_o \parallel R_L)) \approx \frac{2}{g_{m_{PM41}}}$, where $r_{o_{NM41}}$ is the output impedance of NM41.

Because of small R_{out1}, $\frac{\partial I_{o1}}{\partial V_{o1}}$ will be large enough to ignore the loading effect such that stable bias voltages can be achieved. Similar results can be derived at NODE B.

Figure 6 shows the schematic of OBG. The regulated voltages, V_{P41} and V_{P42}, are translated to another pair of voltage levels, V_{op1} and V_{op2}. The output bias of OBG, V_{op1} and V_{op2}, are used to control the tail current of the differential stage of A_{OP3}. Regulator 2 comprising A_{OP3}, PM61, and a resistor string, is shown in Fig. 7. Notably, A_{OP3} is identical to A_{OP2} except that the bias voltages, V_{C1} and V_{C2}, in A_{OP2} are replaced with V_{op1} and V_{op2}, respectively.

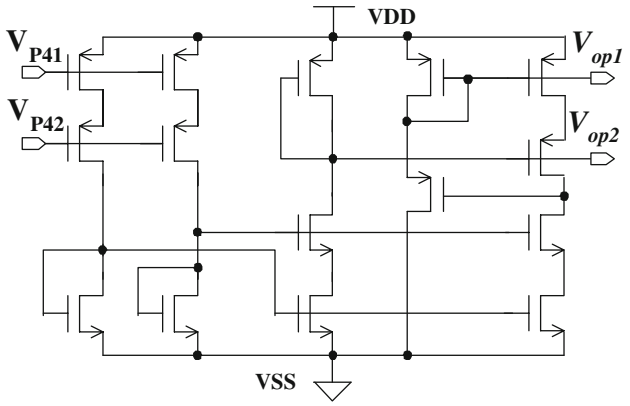

Fig. 6 The schematic of OBG

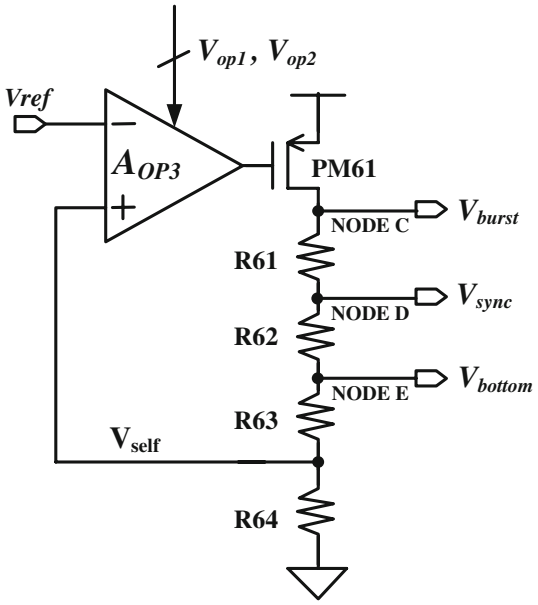

Fig. 7 The circuitry of Regulator 2

2.3 Clamper and timing

The generated V_{burst}, V_{sync}, and V_{bottom}, are fed into the Clamper shown in Fig. 8 to serve as the slicing thresholds. The NTSC signal will be coupled to the clamper via a LPF (low pass filter) with a 600 KHz stopband. By contrast, if the color burst signal is also taken into account, the LPF can be switched to a 3.58 MHz stopband. The external digital control signals, DI3, …, DI6, cooperated with the output of A_{OP6}, i.e., DI7, to control the switches in the clamper, as shown in Fig. 8. The truth table of the digital control block is given in Table 1.

The output voltage of the digital-to-analog converter (DAC) is coupled to the positive input of A_{OP5} where the negative input is the V_{LPF}, which is the output of the filtered NTSC signal. The output of A_{OP5} is fed into the gate drive of NM101 in Fig. 9 which is the schematic of the

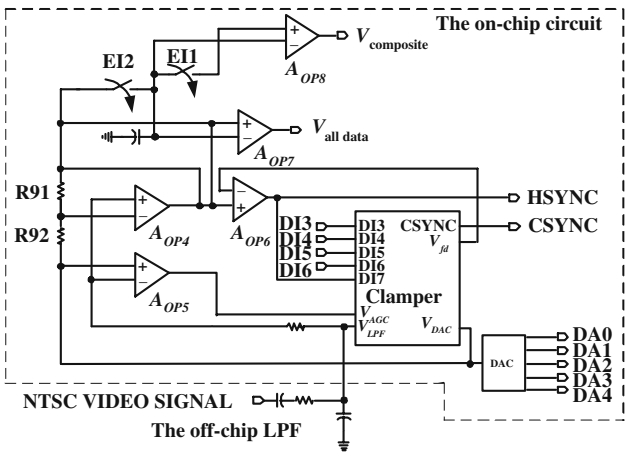

Fig. 8 Architecture of the clamper, sync generator, and the DAC

Table 1 Truth table of the digital control block

Input						
DI3	DI4	DI5	DI6	DI7		
0	0	X	X	X		
0	1	X	X	X		
1	0	X	X	X		
1	1	1	0	1		
Output						
SW00	SW01	SW02	SW03	Clamper	DO1	DO2
ON	OFF	ON	OFF	ON	0	1
ON	OFF	ON	OFF	ON	0	1
OFF	X	OFF	ON	OFF	1	0
ON	OFF	OFF	OFF	ON	0	1

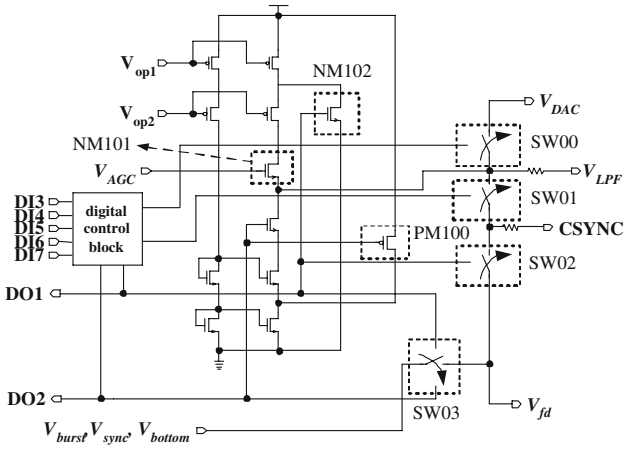

Fig. 9 Schematic of the clamper

Clamper. Namely, it is the auto gain control (AGC) pin to dynamically adjust the threshold voltage level. In short, the operation of the AGC loop comprising Clamper and A_{OP5} is summarized as follows.

$V_{LPF}\uparrow \Rightarrow V_{AGC}\downarrow \Rightarrow$
$V_DAC = V_LPF$, when SW00 is turned on $\Rightarrow V_LPF$ stable.

Thus, the DAC output voltage serves as a dynamically adjustable level to determine and clamp the NTSC video signal.

2.4 Sync generator

The proposed sync separator also generates two critical digital signals which will be utilized in any following DSP core.

HSYNC: HSYNC is generated at the output of A_{OP6} by comparing the V_{fd} which is a DC level provided by Clamper and the output of A_{OP4} which is a threshold voltage level.

$V_{all\ data}$: This signal is present at the output of A_{OP7} which comprises all of the edges of the original NTSC

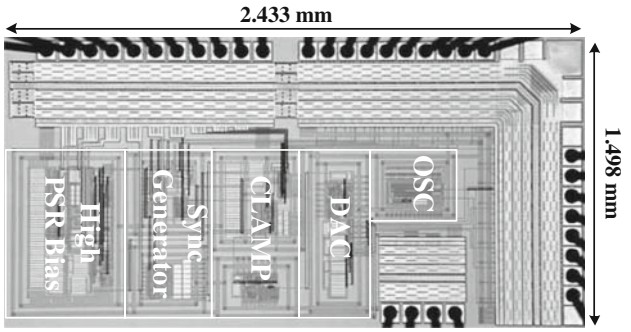

Fig. 10 Diephoto of the proposed sync separator

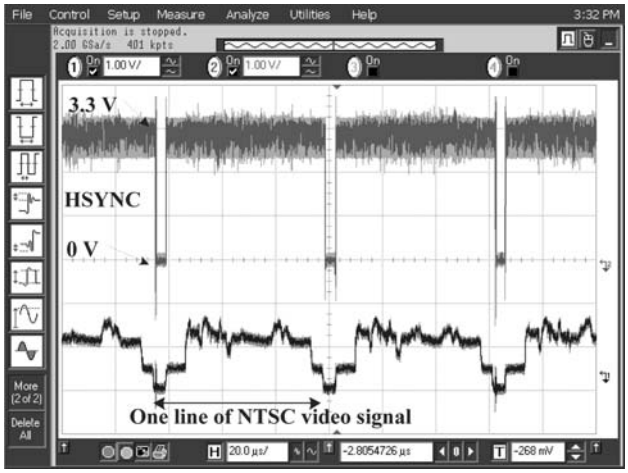

Fig. 11 The measured HSYNC and the corresponding input NTSC signal

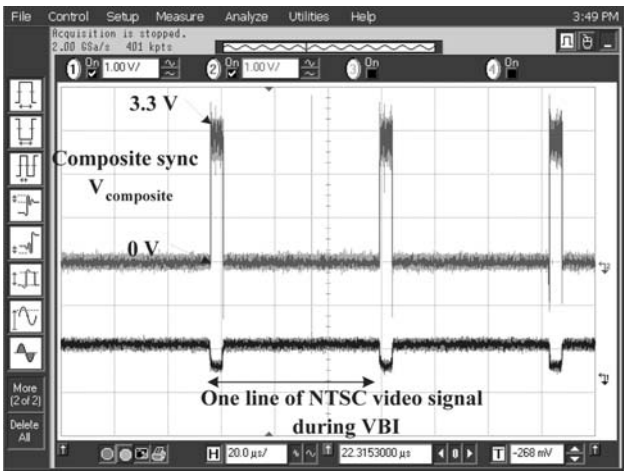

Fig. 12 The measured $V_{composite}$ and the corresponding input NTSC signal

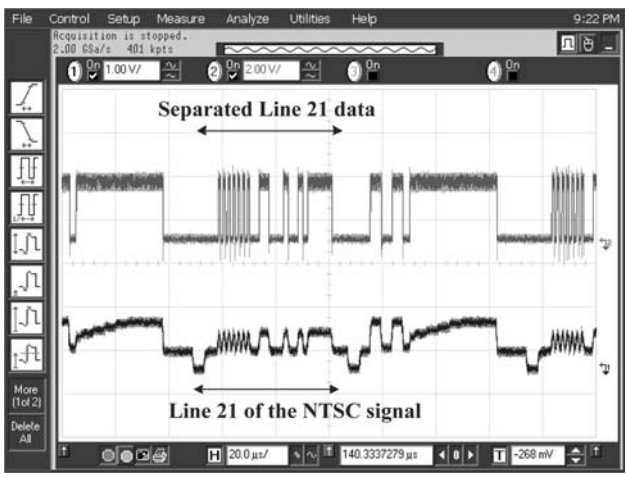

Fig. 13 The measured $V_{alldata}$ and the 0 input NTSC signal

Table 2 Specifications comparison with prior works

	Ours	[5]	[8]	[7]
Process	0.35 μm CMOS	N/A	N/A	0.5 μm CMOS
Generated signals	H-sync, V-sync, C-sync, 12 MHz CLK, Line-21 data	Burst output, V-sync, C-sync, Odd/even output	H-sync, V-sync, C-sync, Phase	comparator output
H-sync V-sync, C-sync				
Temp. (°C)	0–70	0–70	−20–75	N/A
Power (mW)	31.92	1100	350	N/A
Supply voltage (V)	3.3	5	5	3.3
Year	2006	2003	N/A	1998
Performance with supply noise	Functional worked with 1 V supply noise	N/A	N/A	28 dB power supply immuity

signal. When EI2 is turned on, the clamped NTSC signals are sampled. On the other hand, the clamped NTSC signals are hold when EI2 is turned off. Thus, the comparing reference voltage level needed on the negative input of A_{OP7} is obtained by means of the hold operation.

$V_{composite}$: By the combination of switches EI1 and EI2, A_{OP8} outputs a waveform composed of VSYNC and HSYNC which are both required in the later DSP operations. Because of the different line delay caused by EI1 and EI2, the clamped NTSC signal has the cross voltage drops on the sync tip between positive and negative inputs of A_{OP8}. Consequently, the composite sync signal could be generated by voltage comparison.

3 Implementation and measurement

Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm 2P4M CMOS process was adopted to carry out the proposed design. According to Eq. 1, the following equality for a temperature-independent bandgap reference is derived.

$$\frac{\partial V_{ref}}{\partial T} = L \times \ln(K) \times \frac{\partial V_T}{\partial T} + \frac{V_{EB2}}{\partial T} = 0 \quad (3)$$

By substituting all of the parameters in the above equation and setting $L = 10$, $K = 8$, $R_1 = 140\ \Omega$, the V_{ref} is found to be approximately 1.15 V. Then, we select the most common clamping voltages for the NTSC signal given a 3.3 V power supply: $V_{burst} = 3.05$ V, $V_{sync} = 1.78$ V, and $V_{bottom} = 1.57$ V, to design the entire bias circuitry. The simulation and measurement results show that the proposed BGC, which does not require any compensation capacitor, possesses 34 and 30 dB PSR up to 1 MHz, respectively. By contrast, the prior work, [2], employed a capacitor of 22.45 pF to increase the frequency up to 1 MHz where a 37 dB PSR is provided by simulation only. Figure 10 shows the die photo of the proposed design.

Figure 11 shows the separated HSYNC signal and the corresponding input NTSC signal measured on silicon when a noise with a magnitude of 1 V is present in the power supplies. Figure 12 reveals the signal $V_{composite}$, which is the composite sync signal. The NTSC signal shown in Fig. 12 is the vertical blanking interval (VBI) of the NTSC video signal. The separated Line 21 data is shown in Fig. 13. he power consumption of the proposed design is measured to be 31.92 mW. Table 2 lists the specifications of the proposed design compared with several prior works.

4 Conclusion

We have proposed a temperature-insensitive high-PSR bias generation circuitry for the sync separation of NTSC signals in this paper. The cascode configuration as well as the cascaded regulators stabilize the clamping levels to cope with hostile receiving environments. Besides the physical implementation, the detailed PSR analysis of the proposed design is also revealed to illustrate our methodology. According to the measurement results, all of the required sync signals are successfully extracted for any later digital signal processing even if a large noise is coupled in the supply voltage.

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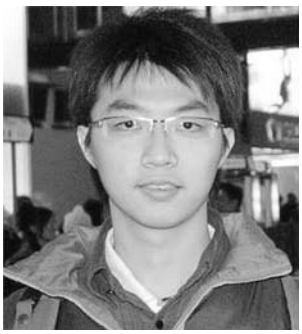

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