Wide-Range 5.0/3.3/1.8 V I/O Buffer Using 0.35-μm 3.3-V CMOS Technology

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***Abstract*— A 5.0/3.3/1.8 V tolerant I/O buffer implemented using typical CMOS 2P4M 0.35 μm process is proposed in this paper. Unlike traditional mixed-voltage-tolerant I/O buffers, the proposed I/O buffer can transmit and receive the signals with voltage levels of 5.0/3.3/1.8 V. By using stacked PMOS and stacked NMOS at the output stage and a dynamic gate bias generator providing appropriate control voltages for the gates of the stacked PMOS, the gate-oxide overstress and hot-carrier degradation are avoided. Moreover, gate-tracking and floating N-well circuits are used to remove the undesirable leakage current paths. The proposed topology can be applied to any technologies with the constraint of VDD $<$ VDDH $<$ 2 $\times$ VDD, which should be considered carfully in sub-100 nm technologies. Measurement results on silicon verify the function and the gate-oxide reliability of the proposed I/O buffer. The maximum transmitting speed of the proposed I/O buffer is measured to be 80/120/84 Mbps for the supply voltage of I/O buffer at 5.0/3.3/1.8 V, respectively, given the load of 29 pF.**

***Index Terms*— fully mixed-voltage-tolerant, I/O buffer, gate-tracking, floating N-well, level converter**

I. Introduction

WITH the evolution of CMOS technology, the supply voltage of the integrated circuit (IC) is scaled down to reduce power consumption. For example, 5.0 V, 3.3 V, and 1.8 V voltage supplies are needed for 0.5 μm, 0.35 μm, and 0.18 μm processes, respectively. When these chips fabricated by different processes are integrated on a PCB-based system, as shown in Fig. 1 (a), conventional I/O buffers are no longer suitable to be the I/O interface. Referring to Fig. 2, the output stage of a traditional I/O buffer is constructed by a PMOS and a NMOS transistor. Therefore, the gate-oxide overstress, hot-carrier degradation, and the undesirable leakage current path through the unexpected turned-on PMOS at the output stage, and the activated parasitic diode of the output PMOS will appear, if a high voltage (VDDH) is biased at the PAD [1]- [3].

Mixed-voltage-tolerant I/O buffers, generally composed of a stacked-NMOS output stage, a gate-tracking circuit, a floating N-well circuit, and a pre-driver, were introduced to overcome these problems [4]- [7], as shown in Fig. 3. By

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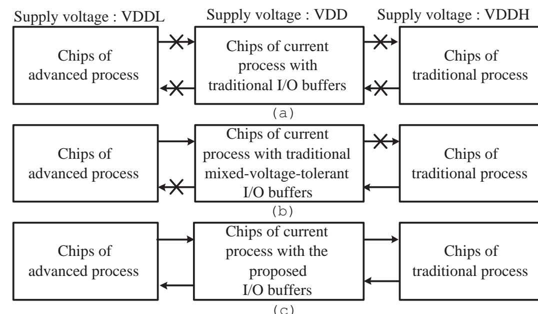

Fig. 1. Applications for different I/O buffers.

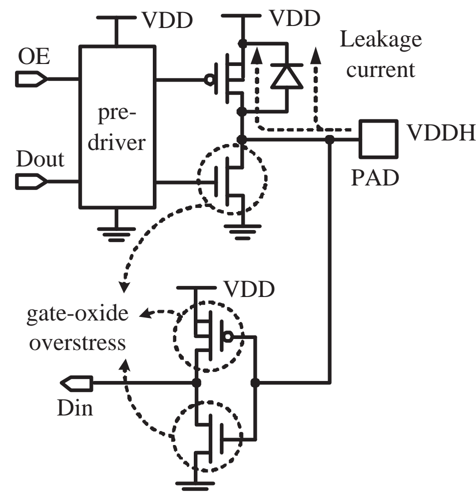

Fig. 2. Schematic of traditional I/O buffer.

using the stacked-NMOS schematic, the gate-oxide overstress and the hot-carrier degradation on the output stage can be avoided when a high supply voltage (VDDH) is applied at the PAD. In order to remove the two leakage current paths in the traditional I/O buffer when VDDH is present, the gate-tracking circuit is employed to trace the voltage on the PAD (V_{PAD}) and then provide an appropriate voltage level, VDDH, for the gate of PMOS at the output stage. Thus, the leakage current path (from the PAD to VDD) through the PMOS at the output stage is eliminated. Similarly, the floating N-well circuit can provide a voltage of VDDH for the N-well of the output PMOS when the PAD is biased at VDDH in the receiving (Rx) mode. With the floating N-well technique, the leakage current through the parasitic diode of the output PMOS would be removed because the parasitic diode would not be turned on. Moreover, even the signal which is as high as

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$3 \times$ VDD can be received correctly by using NMOS-blocking technique [8], [10]. Because the I/O buffers in these prior works allow the signals with a higher voltage level appearing at the PAD without any hazard, they can receive the signal from those chips using traditional processes (with high voltage levels, VDDH) and advanced process (with low voltage levels, VDDL) as shown in Fig. 1 (b). However, since the mixed-voltage-tolerant I/O buffers can not transmit the signals with higher voltage levels, the applications are drastically limited.

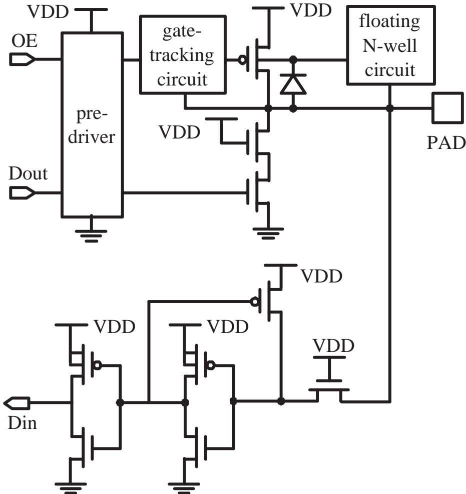
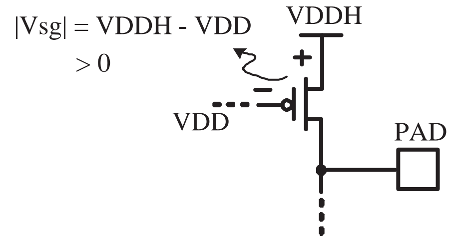


Fig. 3. Schematic of traditional mixed-voltage-tolerant I/O buffer.

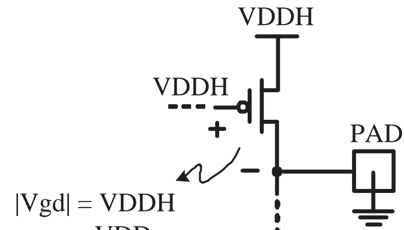
In order to transmit the signal with high voltage level (VDDH), VDDH must be supplied at the source of the PMOS transistor in the output stage no matter how VDDH is generated. Unfortunately, it will result in three problems, as shown in Fig. 4. Firstly, the traditional gate-tracking circuit and the pre-driver can not provide the required high voltage, VDDH, to turn off the output PMOS in the receiving mode or to transmit a logic 0, as shown in Fig. 4 (a). Secondly, even if the gate of the output PMOS can be biased at VDDH, the gate-drain voltage of the output PMOS is larger than the constrained voltage (VDD) when 0 V is biased at the PAD, as shown in Fig. 4 (b). It might cause the damage to the transistor. Thirdly, when VDDH is transmitted, 0 V would be biased at the gate of the output PMOS, as shown in Fig. 4 (c). With the source of the output PMOS biased at VDDH, the source-gate voltage is equal to VDDH and the undesired gate-oxide overstress is resulted.

In order to transmit the signal with voltage level of VDDH, Chen *et al.* [11] proposed an output buffer which can provide an 3.3 V output signal for the 1 V core supply voltage using a 0.13 μm CMOS process. To avoid the gate-oxide overstress, they employed the thick- and thin-oxide devices in the design. The thick-oxide devices can sustain a higher gate voltage such that the gate-oxide reliability can be ensured. However, using the thick-oxide devices would increase the process cost.

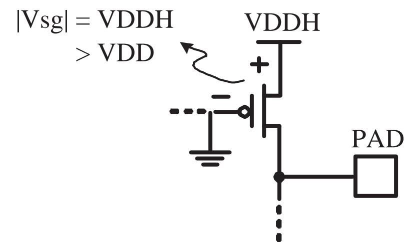
By contrast, this paper proposes a 5.0/3.3/1.8 V tolerant I/O buffer, which can both receive and transmit the signals with



(a) when the output PMOS should be turned off.



(b) when V_{PAD} is biased at 0V



(c) when the output PMOS should be turned on.

Fig. 4. Hazards in the traditional mixed-voltage-tolerant I/O buffer when VDDIO is biased at VDDH.

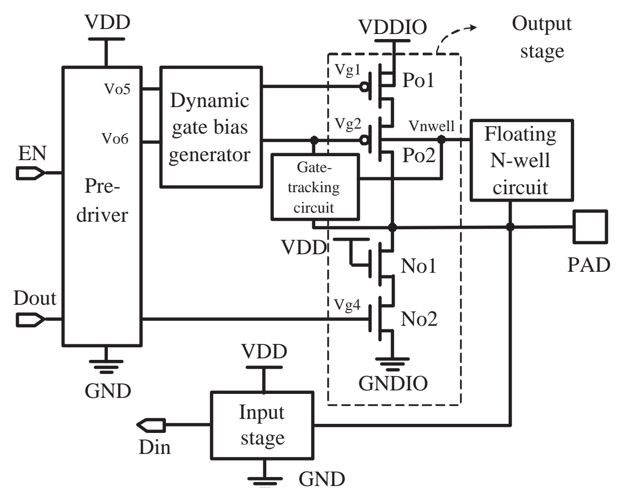


Fig. 5. Block diagram of the proposed 5.0/3.3/1.8 V tolerant I/O buffer.

either a high voltage level (5.0 V) or a low voltage level (1.8 V) without any gate-oxide overstress and leakage current path, as shown in Fig. 1 (c). The proposed 5.0/3.3/1.8 V tolerant I/O buffer is implemented using a typical 0.35 μm CMOS process. Moreover, only thin-oxide devices are used in the proposed I/O design to reduce the additional process cost required for thick-oxide devices.

II. WIDE-RANGE 5.0/3.3/1.8 V I/O BUFFER

Fig. 5 shows the block diagram of the proposed 5.0/3.3/1.8 V I/O buffer. The I/O buffer is composed of a Pre-driver, a Dynamic gate bias generator, an Output stage, an Input stage, a Gate-tracking circuit, a Floating N-well circuit, and a bonding PAD. The major difference of the proposed design from the traditional mixed-voltage-tolerant I/O buffer is that it possesses the VDDIO (different from voltage level for the core, VDD), which is mainly supplied to the output stage depending what voltage level is transmitted. By using VDDIO, transmitting signals with different voltage levels can be achieved. However, it also causes potential gate-oxide overstress problems.

In order to avoid the gate-oxide overstress, the proposed I/O buffer employs the stacked PMOS at the output stage, as shown in Fig. 5. Moreover, Vg1 must be equal to 5.0 V and Vg2 must be larger than 1.7 V (e.g., VDDH - VDD = 5.0 V - 3.3 V) in the receiving mode when VDDIO = 5.0 V and V_{PAD} = 0 V. Similarly, Vg1 and Vg2 must be larger than 1.7 V in the transmitting mode when VDDIO = 5.0 V and logic 1 is transmitted. By controlling the gate voltages, the gate-oxide overstress can be avoided completely. These gate drive voltages are generated by the Dynamic gate bias generator. Notably, VDDIO could be easily obtained from the existing voltage source in the system by engineers. Therefore, no excess cost will be increased. The only penalty is the additional power PADs for VDDIO.

Fig. 6 shows the schematic of the proposed I/O buffer. With various applications, the supply voltage for I/O buffer (VDDIO) might be 5.0/3.3/1.8 V depending on usages, while the supply voltage for the core (VDD) is always 3.3 V.

Pre-driver: The Pre-driver is for decoding and pre-driving. EN is the control signal to determine whether the transmitting (EN = 0 V) or receiving (EN = 3.3 V) mode is selected. The signal Dout is sent by the digital core and expected to be transmitted to external driven devices. In the transmitting mode, if Dout = 3.3 V, No2 in the output stage would be turned off while Po1 and Po2 are switched on such that V_{PAD} = VDDIO = 5.0/3.3/1.8 V. By contrast, V_{PAD} = 0 V when Dout = 0 V. In the receiving mode, the signal Dout is irrelevant.

Input stage: The input stage is a receiving circuit for the input signal with a voltage level higher than its normal supply voltage [7]. By tuning the transistor aspects, it can accept the voltage from 1.8 V to 5.0 V. Ni1 isolates any unexpected high voltage at the PAD. When V_{PAD} = 5.0/3.3 V, Vi1 would be close to VDD minus a threshold voltage (denoted by $\sim$3.3 V). Because the high voltage of 5.0 V is isolated, the gate-oxide reliability is ensured. With the feedback latch of Pi1, Vi1 would be pulled up to the full swing to reduce the static power consumption. Besides, Pi1 pulls Vi1 up to 3.3 V when V_{PAD} = 1.8 V is given. Therefore, if V_{PAD} = 5.0/3.3/1.8/0 V, Din = 3.3/3.3/3.3/0 V.

Output stage: In order to keep the gate-oxide reliability, stacked PMOS and stacked NMOS are employed. Moreover, Vg1 = 5.0 V and Vg2 $>$ 1.7 V must be provided when VDDIO = 5.0 V and V_{PAD} = 0 V in the receiving mode. When V_{PAD} is biased at 5.0 V in the receiving mode, Vg2 and Vnwell would be pulled to 5.0 V by the Gate-tracking circuit and the Floating N-well circuit, respectively, to avoid the mentioned undesired leakage current. In the transmitting mode, Vg1 and Vg2 must be larger than 1.7 V when VDDIO = 5.0 V and logic 1 (= 5.0 V) is transmitted to turn on the stacked PMOS and avoid the gate-oxide overstress. Vg1 and Vg2 will be generated by the Dynamic gate bias generator.

Gate-tracking circuit: Po3 is the gate-tracking circuit. The gate-tracking circuit is to bias Vg2 to 5.0 V when V_{PAD} = 5.0 V in the receiving mode. When V_{PAD} = 5.0 V, Po3 will be turned on such that Vg2 is charged to 5.0 V. With the source and gate voltages at the same voltage level of 5.0 V, Po2 will not be turned on and no leakage current will be introduced. Because of the NMOS No3 with its gate at 3.3 V, Vo2 (the source of No3) can just be pulled to the maximum voltage of $\sim$3.3 V even if Vg2 is biased at 5.0 V. Thus, the internal circuit (Dynamic gate bias generator) is protected from the high voltage signal of 5.0 V. When V_{PAD} is biased at 3.3, 1.8, or 0 V, Po3 will be off and Vg2 is determined by the Dynamic gate bias generator.

Floating N-well circuit: Po10, Po11, Po12, No14, and No15 consist of the Floating N-well circuit. The Floating N-well circuit provides the N-well voltages for Po2 and Po3 to avoid the leakage current path from parasitic diodes. When V_{PAD} = 5.0 V and VDDIO = 5.0/3.3/1.8 V, Vnwell will be coupled to 5.0 V through Po10, while Po11 is off by Vg11 = 5.0 V. When V_{PAD} = 0 V and VDDIO = 5.0/3.3/1.8 V, Po10 and Po12 are off and No15 is on such that Vg11 is pulled to 0 V. Thus, Po11 is turned on. For VDDIO =5.0/3.3 V, Vnwell would be biased at $\sim$3.3 V by the protection NMOS No14 and the turned-on PMOS Po11. For VDDIO = 1.8 V, Vnwell would be charged to 1.8 V by No14 and Po11. Therefore, the leakage current through the parasitic diode of Po2 and Po3 can be eliminated. Similarly, when V_{PAD} = 1.8 V and VDDIO = 5.0/3.3 V, Vnwell will be charged to $\sim$3.3 V by No14 and Po11. Notably, when VDDIO is at 1.8 V and V_{PAD} $\leq$ 1.8 V, Vnwell is coupled to 1.8 V but not be biased at 3.3 V (= VDD), which is the voltage generated by the traditional floating nwell circuit [1]. With Vnwell = 1.8 V, the body effect of Po2 is avoided in this case. It is helpful for transmitting a signal with VDDIO at 1.8 V using 0.35 μm devices. Therefore, the output driving capability of the stacked PMOS will be enhanced by pulling down the N-well voltage to 1.8 V of Po2 when VDDIO is biased at 1.8 V.

Dynamic gate bias generator: The Dynamic gate bias generator is composed of a Voltage level converter [12], a VDDIO detector, and a Voltage clamper. The voltage level converter receives a pair of complementary signals with volt-

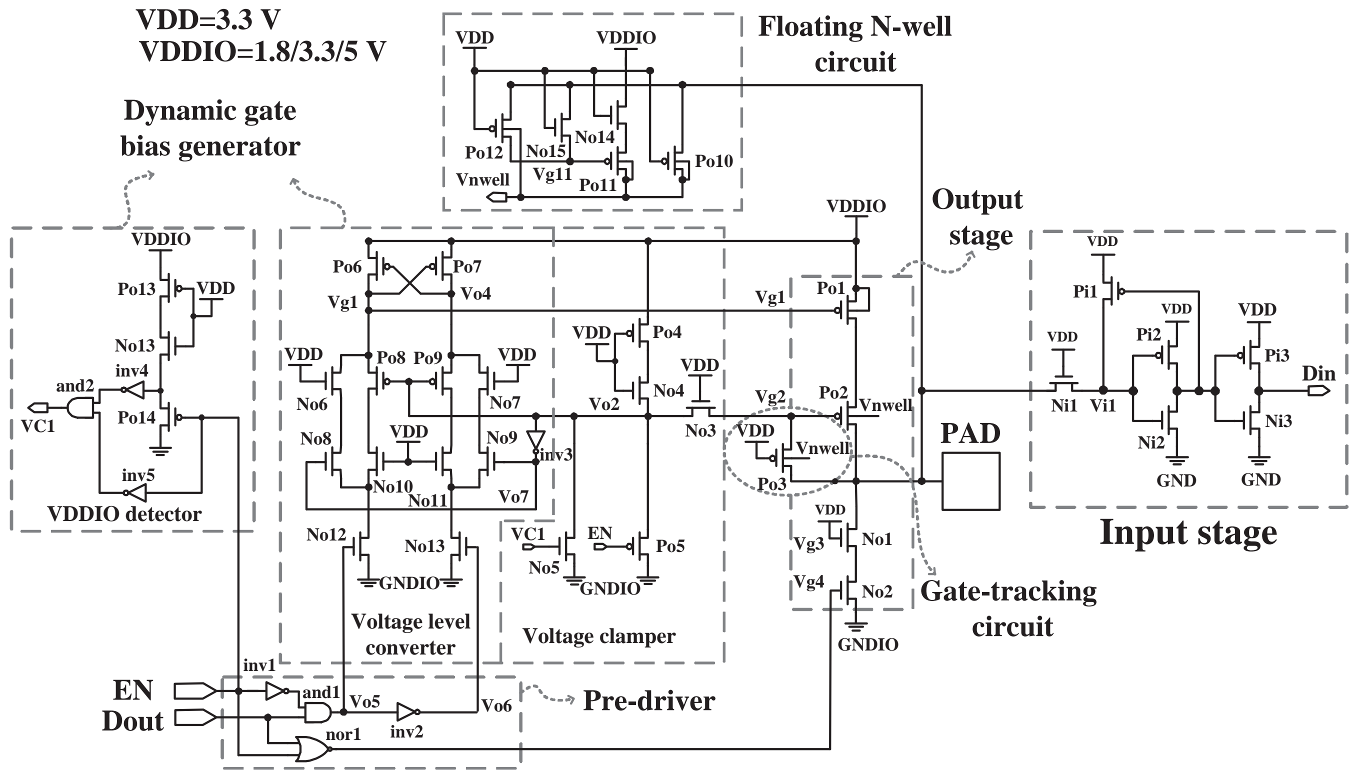


Fig. 6. Schematic of the proposed 5.0/3.3/1.8 V tolerant I/O buffer.

age level of 0 V and VDD from the Pre-driver. Then, it converts the complementary signals to Vo2+$|V_{th_Po8}|$ and VDDIO for VDDIO = 5.0 V. V_{th_Po8} is the threshold voltage of PMOS Po8. For VDDIO = 3.3/1.8 V, it outputs the complementary signals from 0 V to VDDIO. The VDDIO detector can detect the voltage level of VDDIO and provide a detection signal VC1 for the voltage clamper. VC1 will be biased at 0/3.3/3.3 V for VDDIO = 5.0/3.3/1.8 V, respectively. The voltage clamper is to provide a required DC voltage for the voltage level converter and for Vg2.

In the transmitting mode, EN is coupled to 0 V. Thus, the output signal of VDDIO detector, VC1, is determined by the output of the inverter inv4. When VDDIO = 5.0 V, the input of inv4 is pulled up to $\sim$3.3 V through Po13 and No13 such that VC1 is at 0 V. Because EN and VC1 are both biased to 0 V, Po5 in the Voltage clamper is turned on and No5 is off. Thus, Vo2 will be biased to 1.91 V by Po4, No4, and Po5. Vo7 is then pulled to 0 V such that No8 and No9 in the Voltage level converter are turned off. If Dout = 0 V, Vo5 will be at 0 V as well such that No12 is off and No13 is on. Therefore, Vo4 is discharged to the voltage of 2.22 V by Po9 and Vg1 is pulled to VDDIO (= 5.0 V). With Vg1 at 5.0 V, Vg2 (= Vo2) at 1.91 V, and Vg4 at 3.3 V, V_{PAD} will be pulled to 0 V. That is, the signal of logic 0 is transmitted. Besides, the gate-oxide reliability for the Output stage will be ensured. If Dout = 3.3 V, Vg1 will be at 2.22 V, Vg2 will be at 1.91 V, and Vg4 will be at 0 V. Thus, V_{PAD} is pulled up to 5.0 V and logic 1 is transmitted. When VDDIO = 3.3/1.8 V, Po13 in the VDDIO detector will be turned off such that VC1 is 3.3 V. Then, Vo2 and Vg2 is discharged to 0 V through No5 in the Voltage clamper such that Vo7 is pulled to 3.3 V. It turns on the NMOS No8 and No9. Thus, Vg1 will be pulled down to 0 V through No6 and No8 when Dout = 3.3 V. When Vg1 and Vg2 are pulled to 0 V, the stacked PMOS can be turned on even if the low VDDIO (= 1.8 V) is given. On the contrary, Vg1 will be charged to VDDIO (= 3.3/1.8 V) for Dout = 0 V. Thus, logic 0 could be transmitted.

In the receiving mode, EN is biased at 3.3 V. Vo5 in the Pre-driver will be pulled to 0 V because the output of inv1 is at 0 V. Thus, Vg1 is coupled to VDDIO (= 5.0/3.3/1.8 V) such that Po1 is turned off. Besides, Vg4 is pulled to 0 V by EN at 3.3 V such that No2 is turned off as well. Moreover, Vg2 will be charged to 5.0 V through the Gate-tracking circuit (Po3) when V_{PAD} = 5.0 V to avoid the leakage. No3 is to isolate the high voltage (5.0 V) at Vg2 such that the gate-oxide overstress at the internal devices is avoided. When V_{PAD} = 3.3/1.8 V, Po3 is off such that Vg2 would be determined by the Dynamic gate bias generator. Because EN is biased at 3.3 V, VC1 is biased at 0 V. Thus, No5 and Po5 in the Voltage clamper would be turned off. Vo2 will then be charged to $\sim$3.3 V for VDDIO = 5.0/3.3 V and be charged to 1.8 V for VDDIO =1.8 V by Po4 and No4. Therefore, Vg2 is biased at $\sim$3.3/$\sim$3.3/1.8 V for VDDIO = 5.0/3.3/1.8 V in the receiving mode. With Vg2 $>$ 1.7 V for VDDIO = 5.0 V, the gate-oxide overstress on Po2 is avoided.

III. Implementation and Measurement

The proposed 5.0/3.3/1.8 V tolerant I/O buffer is carried out by using a typical 0.35 μm 2P4M CMOS process. In order

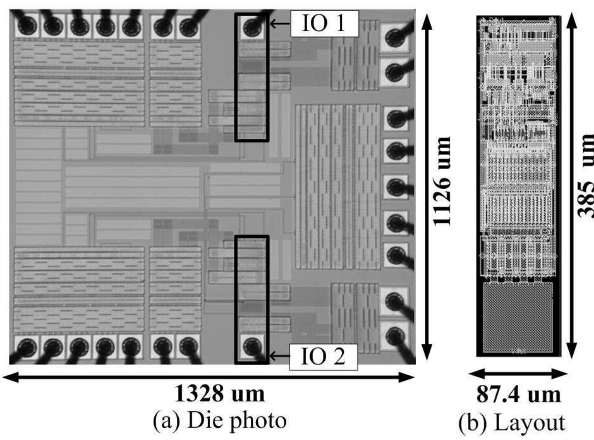


Fig. 7. Layout and die photo of the proposed I/O buffer.

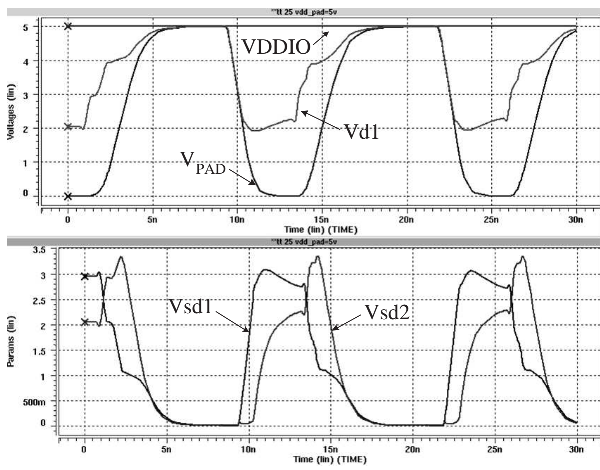


Fig. 8. The simulated transient source-drain voltages of Po1 and Po2 in the transmitting mode when VDDIO = 5 V.

to reduce the process and manufacture cost, only poly 1 is used and no thick-oxide devices are employed. Fig. 7 shows the die photo and the layout of the proposed design. Two proposed I/O buffers are included in the same die for testing consideration. Referring to Fig. 7, IO2 is implemented for the purpose of testing. Vg1, Vg2 and Vnwell of IO2 are respectively output for measurement and observation. Moreover, guard rings are drawn for avoiding latch up problems. The area of a proposed wide-range 5.0/3.3/1.8 V I/O buffer is 385 $\times$ 87.4 μm.

Fig. 8 shows the simulated drain voltage of Po1 (Vd1) and the source-drain voltages of Po1 and Po2 (Vsd1 and Vsd2) when an 80 MHz signal is transmitted. It reveals that Vsd1 and Vsd2 are both smaller than the constrained voltage in the 3.3 V 0.35 μm CMOS technology. Fig. 9-11 shows the measured Vg1, Vg2, Dout, and V_{PAD} at 1 MHz on silicon in the transmitting mode for VDDIO = 5.0/3.3/1.8 V, respectively. The proposed I/O buffer can transmit the signals with 5.0/3.3/1.8 V. For VDDIO = 5.0 V, Vg1 is biased at 2.22/5.0 V for transmitting logic 1/0, respectively, as shown in Fig. 9. Moreover, Vg2 is biased at 1.91 V such that the gate-oxide reliability for Po2 is confirmed. For VDDIO = 3.3/1.8 V, Vg2 stays at 0 V and Vg1 is biased between 0 V and 3.3/1.8 V for transmitting logic 1 and logic 0, respectively, as shown

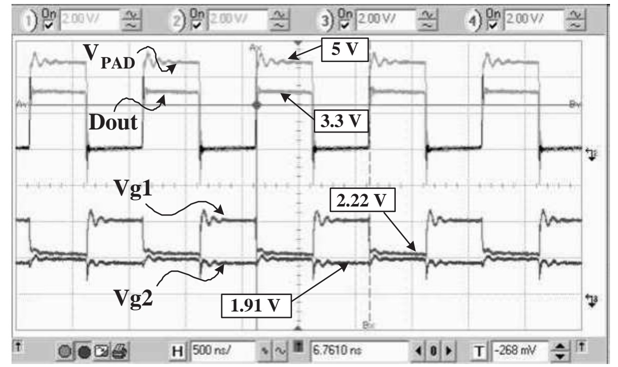


Fig. 9. Measured Vg1, Vg2, Dout, and V_{PAD} at 1 MHz in the transmitting mode when VDDIO = 5 V.

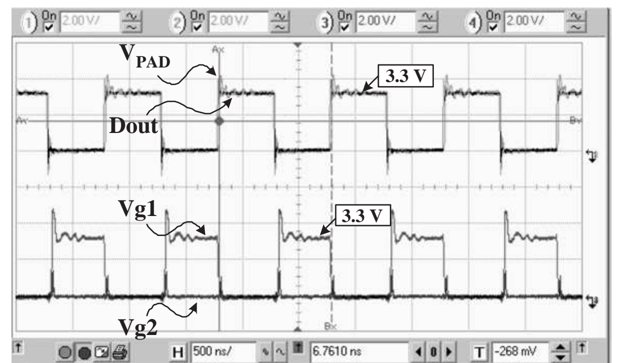


Fig. 10. Measured Vg1, Vg2, Dout, and V_{PAD} at 1 MHz in the transmitting mode when VDDIO = 3.3 V.

in Fig. 10-11.

Fig. 12-14 shows Vg1, Vg2, Vnwell, and V_{PAD} in the receiving mode for VDDIO = 5.0/3.3/1.8 V when 100 KHz 5.0 V signals are biased at the PAD. Referring to Fig. 12-14, Vg1 is biased at VDDIO to turn Po1 off. For VDDIO = 5.0/3.3 V, Vnwell is pulled high when the input signal at the PAD (V_{PAD}) is at 5.0 V to turn off the leakage current path through the parasitic diode, as shown in Fig. 12-13. For VDDIO = 1.8 V, Vnwell is discharged to 1.8 V. Thus, the body effect in Po2 can be removed and the driving capability for transmitting logic 1 with 1.8-V VDDIO in the transmitting mode can be improved, as mentioned in Section 2. Besides,

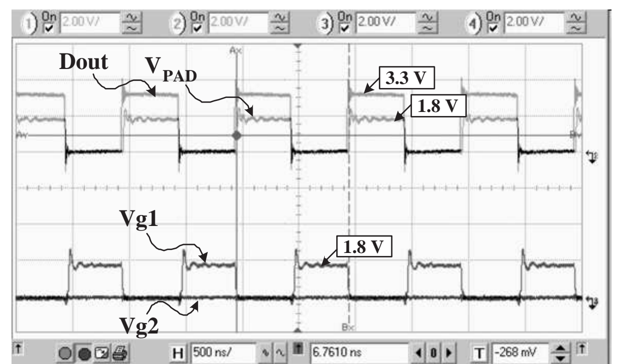


Fig. 11. Measured Vg1, Vg2, Dout, and V_{PAD} at 1 MHz in the transmitting mode when VDDIO = 1.8 V.

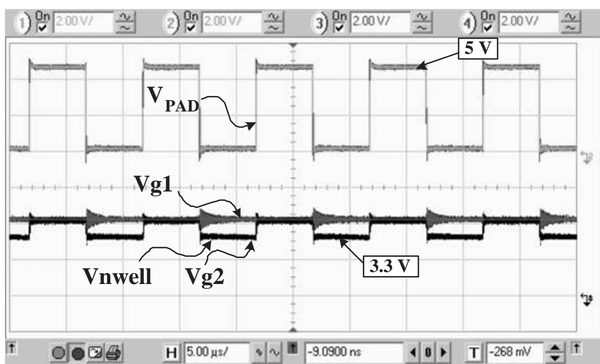


Fig. 12. Measured Vg1, Vg2, Vnwell, and V_{PAD} in the receiving mode when VDDIO = 5 V.

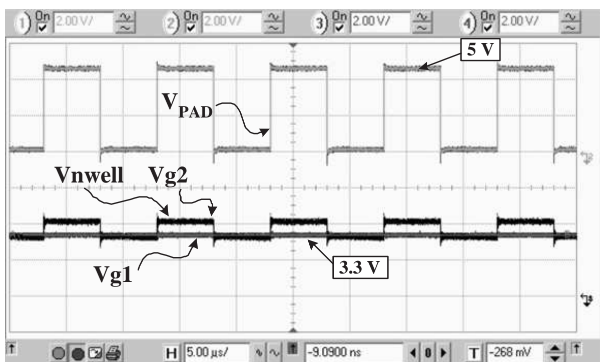


Fig. 13. Measured Vg1, Vg2, Vnwell, and V_{PAD} in the receiving mode when VDDIO = 3.3 V.

in order to remove another undesirable leakage current path, Vg2 is pulled high by the Gate-tracking circuit due to the V_{PAD} at a voltage level of 5.0 V, as shown in Fig. 12-14. Referring to Fig. 15-17, the maximum speed of the proposed I/O buffer is 80/120/84 Mbps with a 29 pF load (consisting of a loaded capacitor of 20 pF and the input capacitor of the probe of 9 pF) for VDDIO = 5.0/3.3/1.8 V in the transmitting mode, respectively. Fig. 18-20 show the 1 MHz input signals of the proposed I/O buffer in the receiving mode. For V_{PAD} = 5.0/3.3/1.8 V, Din with voltage level of 3.3 V is obtained successfully.

Moreover, the function of the proposed circuit is also verified on silicon at two extreme temperatures, 125°C and -20°C. The temperature test is measured using the thermo stream (TP 0400A-2B21-2). The measured gate voltages, Vg1 and Vg2, still meet the requirements addressed in Section II to avoid the gate-oxide overstress. The Floating N-well output signal Vnwell and Vg2 can be also pulled high in the receiving mode to remove the leakage current paths. The maximum speed of the output signals at the extreme temperatures are revealed in Table I. The output frequency at -20°C is measured faster than 125°C. For VDDIO = 3.3 V, the measured output speed is limited by the specifications of the pulse generator (Model number: PM5716), which can only provide a 90 Mbps data rate. Notably, the load of this measurement is changed to 33 pF because the measurement instrument is different.

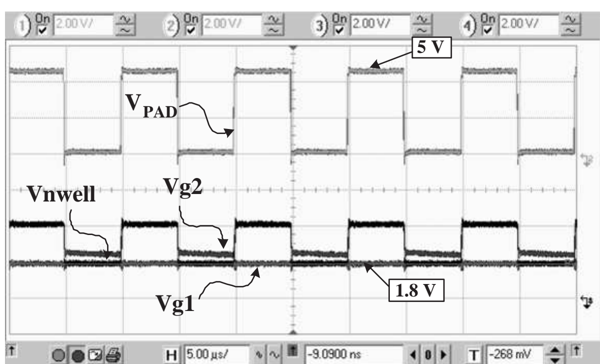


Fig. 14. Measured Vg1, Vg2, Vnwell, and V_{PAD} in the receiving mode when VDDIO = 1.8 V.

VDDIO	5.0 V	3.3 V	1.8 V
At 125°C	76 Mbps	90 Mbps	74 Mbps
At -20°C	84 Mbps	90 Mbps	88 Mbps

TABLE I

MEASURED MAXIMUM OUTPUT SPEED AT THE EXTREME TEMPERATURES FOR A GIVEN 33 PF LOAD (THE PROBE LOAD OF 13 PF PLUS THE CAPACITANCE LOAD OF 20 PF).

Fig. 21 reveals the measured eye diagram of the output signal in the transmitting mode at 20 Mbps. The sampling window for VDDIO = 5.0/3.3/1.8 V are 44.86/46.80/36.21 ns, respectively. For VDDIO = 1.8 V, the sampling window is limited by the slow rise time due to the degraded driving ability of the stacked PMOS output stage and the extremely low supply voltage operation.

Besides, the proposed circuit is verified on silicon for 336 hours (2 weeks) prolonged operation.

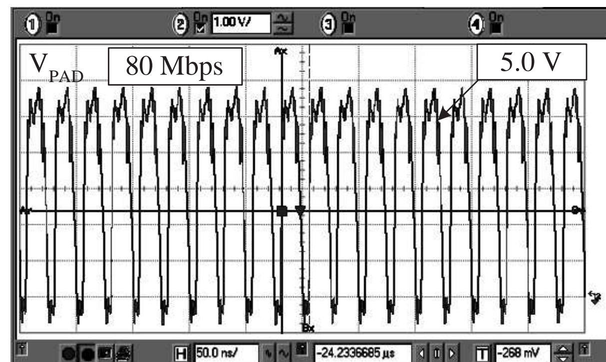


Fig. 15. Measured output signal of proposed I/O buffer with a 29 pF load when VDDIO = 5 V.

IV. DISCUSSION

A. Portability of the process

As we mentioned in Section II, the proposed wide-range I/O buffer ensures the reliability by providing the appropriate gate voltages for the output stage. In order to ensure the reliability, Vgs (Vgd) and Vds should be less than the constraint voltage (VDD) for VDDIO = VDDH. By using the

	Process	Transmitted signal level	Received signal level	Output stage	Devices	Year
[1]	0.13 μm CMOS	VDD	VDDH	Single PMOS/ stacked NMOS	only thin-oxide	2004
IO1 in [7]	0.25 μm CMOS	VDD	VDDH/VDD	Single PMOS/ stacked NMOS	only thin-oxide	2006
IO2 in [7]	0.25 μm CMOS	VDD	VDDH/VDD	Single PMOS/ stacked NMOS	only thin-oxide	2006
[11]	0.13 μm CMOS	VDDH	none	Stacked PMOS/ stacked NMOS	thick-/ thin-oxide	2007
ours	0.35 μm CMOS	VDDH/ VDD/VDDL	VDDH/ VDD/VDDL	Stacked PMOS/ stacked NMOS	only thin-oxide	2008

Note: [1]The VDDH/VDD in [1] are 2.5/1.0 V, respectively.
[2]The VDDH/VDD in [7] and [10] are 5.0/2.5 V, respectively.
[3]The VDDH/VDD in [11] are 3.3/1.0 V, respectively. And only the output buffer was presented in [11].

TABLE II

COMPARISON WITH SEVERAL PRIOR WORKS.

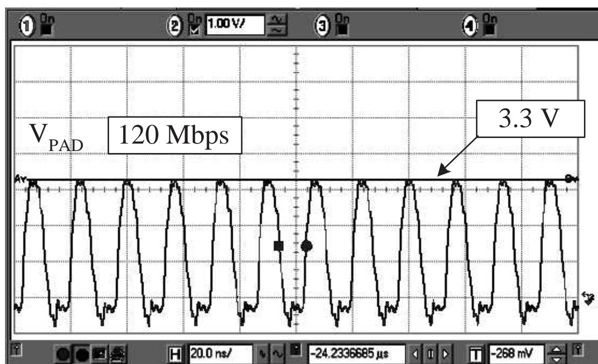


Fig. 16. Measured output signal of proposed I/O buffer with a 29 pF load when VDDIO = 3.3 V.

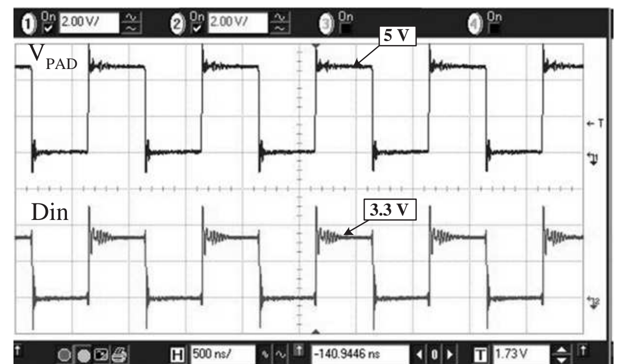


Fig. 18. Measured V_{PAD} and Din in the receiving mode when VDDIO = 5 V.

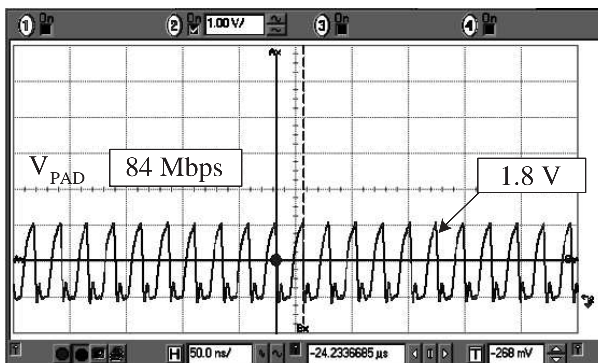


Fig. 17. Measured output signal of proposed I/O buffer with a 29 pF load when VDDIO = 1.8 V.

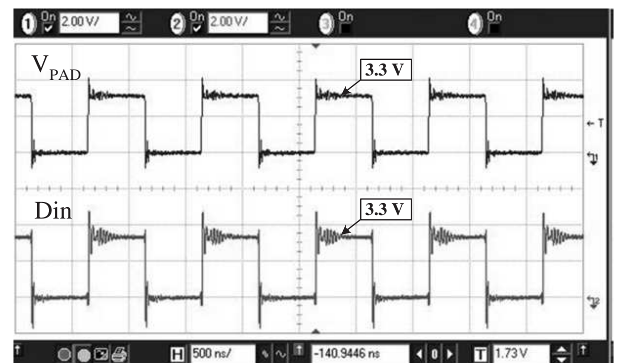


Fig. 19. Measured V_{PAD} and Din in the receiving mode when VDDIO = 3.3 V.

stacked PMOS and the stacked NMOS in the output stage, Vg1 and Vg2 should be biased at a limited voltage, which is larger than VDDH-VDD when logic 1 is transmitted. In this situation, |Vgs| and |Vgd| of Po1 and Po2 are VDDH-VDD, which should be smaller than VDD. It implies that VDDH $<$ 2$\times$VDD. Similarly, Vg1 = VDDH and Vg2 $>$ VDDH-VDD are provided when logic 0 is transmitted and logic 0 is received. Thus, |Vgs1| = 0 V, |Vgd1| = VDDH-(VDDH-VDD) = VDD, |Vgs2| = 0 V, and |Vgd2| = VDDH-VDD are resulted by assuming the source voltage of Po2 (Vs2) is very close to Vg2 (= VDDH - VDD). It implies that |Vgd2| = VDDH-VDD $<$ VDD and thus VDDH $<$ 2$\times$VDD. Therefore, the proposed wide-range I/O buffer will work correctly as long as VDD $<$ VDDH $<$ 2 $\times$ VDD is guaranteed. Therefore, the structure of the proposed design can be implemented in advanced processes if the above constraint is satisfied. For example, the proposed design could be carried out using 90 nm CMOS process and operate at the typical voltage of 1.0 V (=VDD). At the same time, it can communicate with a chip of 0.18 μm CMOS process which operates at a supply voltage

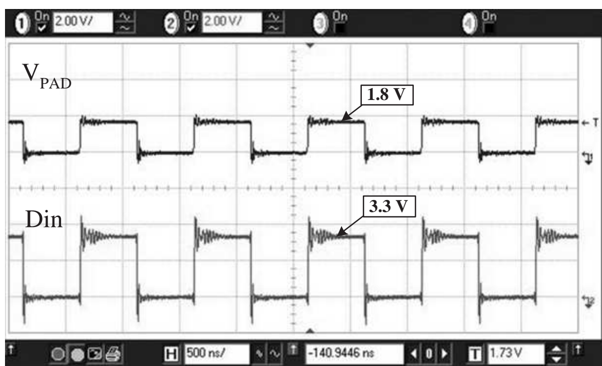


Fig. 20. Measured V_{PAD} and Din in the receiving mode when VDDIO = 1.8 V.

of 1.8 V (VDDH) and another chip of 65 nm CMOS process which operates at supply voltage of 0.6 V (VDDL). Because low VDDL results in a low operating frequency, the voltage level of VDDL would be constrained by the required frequency requirement for the system.

B. Reliability

Time-dependent dielectric breakdown (TDDB) is one of the major failure mechanisms in VLSI circuits [13]. Gate-oxide breakdown and hot-carrier degradation are both the TDDB issues [7]. Gate-oxide breakdown would be induced by the oxide stress voltage over the tolerant voltage. The situation can even be accumulated with the time period when the oxide overstress voltage is present [13], [14]. Hence, the defect caused by DC stress is more serious than AC stress (transient stress) [7]. Thus, most of the mixed-voltage I/O buffer designs only consider the DC stress [3]- [10]. Besides, the devices in a mature process can endure Vgs and Vgd in the transient state 16% (=$\frac{2.2V-1.9V}{1.9V}$, where 2.2 V is the tolerant AC stress and 1.9 V is the tolerant DC stress [15]) higher than the normal operating voltage in the static state [15]. Thus, the overshoot caused by the ringing at Vg1 and Vg2, as shown in Fig. 9, is in the tolerant range of reliability.

In addition, the hot-carrier degradation occurs when the transistors are operated in the saturation region with the drain-source voltages (Vds) larger than the normal operating voltage (VDD) [7], [15]. Thus, Vds should be less than VDD in the transient state to avoid the hot-carrier degradation, as shown in Fig. 8. However, a problem of Vds larger than VDD on the NMOS in the output stage has been reported recently [16]. When the I/O buffer operates at the transition from the mode of receiving the logic 1 (= VDDH = 5.0 V) to another mode of transmitting logic 0 (0 V), Vds on the output NMOS might be larger than VDD during the transition time. It would induce the hot-carrier degradation. The problem can be avoided by adding a tracking circuit to pull down V_{PAD} before the operating mode transition (from receiving VDDH to transmitting 0 V) is completed [16].

C. Package

The package and the bond wire of the chip would cause a parasitic inductance, which might induce the ringing at the output signal V_{PAD}. The overshoot and undershoot then appears due to the ringing, which might threat the gate-oxide reliability. The proposed I/O buffer is simulated with a loading inductance of 12 nH for the parasitic consideration on the bond wire. Based on the post-layout simulation results, V_{PAD} possess 14.72% undershoot and 1.82% overshoot with a 12 nH inductive load and a 20 pF capacitive load. They are under the tolerant AC stress of 16%. Moreover, 12 nH is large enough to cover the normal wire bond package, which usually induces a parasitic inductance only from 0.569 nH to 2.845 nH [17].

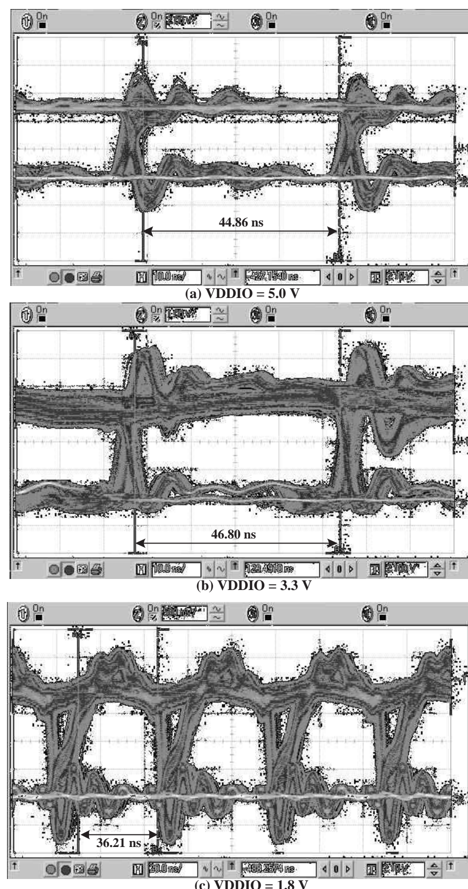


Fig. 21. The measured eye diagrams of the output signal V_{PAD} at 20 Mbps data rate.

D. ESD issue

ESD protection is an important issue in I/O buffer design. In traditional I/O buffers, the parasitic diode of the PMOS in the output stage can provide a discharge path for the ESD current. However, the parasitic diode connected to the I/O PAD and VDDIO does not exist due to the floating N-well circuit in the mixed-voltage-tolerant I/O buffer. Thus, the ESD capability in the mixed-voltage-tolerant I/O buffer is poorer than that in the traditional I/O buffers for the same area condition [18]-[20]. In order to retain enough ESD capability, the proposed I/O buffer possesses the worst-case HBM ESD robustness of 3.3465 KV in the ND-mode. The penalty is the large area for the W/L ratio of NMOS and PMOS to be 250 um/ 0.4 um and 500 um / 0.4 um, respectively.

V. Conclusion

This paper proposes a 5.0/3.3/1.8 V tolerant I/O buffer. By using an extra supply voltage, the proposed I/O buffer can transmit and receive the signals with voltage levels of 5/3.3/1.8 V. Because the thick-oxide devices which can sustain higher gate voltage are not used, the stacked PMOS and the stacked NMOS are employed simultaneously at the Output stage to avoid the gate-oxide overstress. Furthermore, the dynamic gate bias generator is proposed to provide appropriate control voltages for the gate of the stacked PMOS for the gate-oxide reliability. By controlling the gate voltages, the driving strength of the stacked PMOS is enhanced with VDDIO at 1.8 V. Besides, the Gate-tracking and Floating N-well circuits are included to remove the undesirable leakage current paths. The proposed design can be carried out using any technologies by satisfying the requirement of $\text{VDD} < \text{VDDH} < 2 \times \text{VDD}$, which must be taken into account carefully in sub-100 nm technologies. The comparison with several prior works is revealed in Table II. The proposed I/O buffer is the only one design which can transmit and receive the signal with voltage level of VDDH/VDD/VDDL.

VI. Acknowledgment

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