A Single-Chip CMOS IF-band Converter Design for DVB-T Receivers

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Abstract

This paper describes a CMOS single chip IF-band converter (IFC) which is applied in the analog front end circuitry of DVB-T receivers. The proposed IFC is composed of a down-conversion mixer, an automatic gain controller (AGC), and an anti-aliasing filter (AAF). The down-conversion mixer uses a current folded-mirror technique which converts a 36 MHz intermediate frequency (IF) input into a 4.5 MHz baseband signal. The AGC loop applies a novel digital VGA (variable gain amplifier) basing on a g_m-boosting DVGA (digital VGA). A total of three tunable gain stages are cascaded to provide a 70 dB dynamic range. A temperature-compensated 6th order transconductance-C (Gm-C) filter with digitally tunable bandwidth (6, 7, 8 MHz) is used to constitute the proposed anti-aliasing filter (AAF). Moreover, a temperature-compensated circuitry is used to neutralize the AAF's bandwidth drifting caused by the temperature variation.

Key words: Mixer, Frequency converter, Conversion gain, DVB-T, Wireless network

1 Introduction

The function of a DVB-T (terrestrial digital video broadcasting) receiver analog front end is to convert an input signal from the radio frequency (RF) tuner

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into a bit stream for following OFDM (orthogonal frequency division multiplexing) demodulation processing. The analog front end circuitry consists of a radio frequency tuner, a down-conversion mixer, an AGC, an AAF, and an analog to digital converter, as shown in Fig. 1. The radio frequency tuner selects a desired channel and converts the received signal into a 36 MHz IF signal. The down-conversion mixer then converts the 36 MHz IF signal into a 4.5 MHz baseband signal. The AGC block is used to ensure that the amplitude of the received signal is kept in a constant level which is large enough for the following circuitry. The DVGA possesses a 70 dB dynamic tuning range with a 0.3 dB gain error and 95 MHz bandwidth. The AAF is used to remove the adjacent-channel coupled noise generated by the mixer to avoid inter-channel interferences and then passes the desired signal to the analog to digital converter (ADC) [1]. The proposed IFC integerates all of the down-conversion mixer, the AGC, and the AAF into a single chip. Physical measurements on silicon justify the performance of our design with conversion gain = -24 dB, IIP3 = -2 dBm.

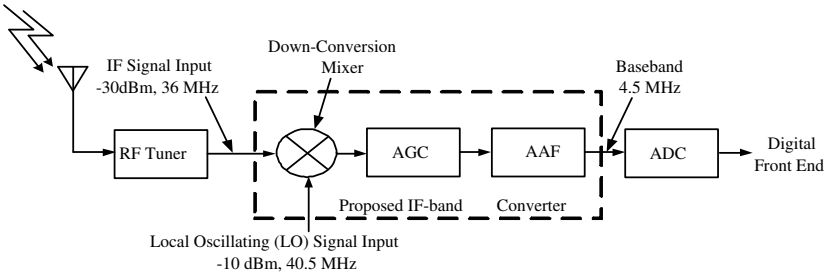

Fig. 1. DVB-T receiver analog front end

2 Subcircuits of IFC: Mixer, AGC, and AAF

2.1 Down-Conversion Mixer

There are three basic active mixers using the concept of balancing: unbalanced mixer, single balanced mixer, and double balanced mixer. The unbalanced mixer has a problem that the frequency components at the radio frequency input will appear at the output. It is called radio frequency feedthrough. Similarly, the frequency components at the local oscillator frequency input will also propagate through in the single balanced mixer designs. It is called local oscillation feedthrough. Neither radio frequency feedthrough nor local oscillation feedthrough is welcomed in any receiver [2]. Hence, we choose the double balanced mixer as the basic structure of our mixer.

Fig. 2 shows a current folded-mirror mixer which is a double balanced mixer

structure to implement the desired DVB-T down-conversion mixer. M1 and M2 convert the IF voltage into a current signal. M3 $\sim$ M6, and two R_{E2} resistors consist of two current mirrors to bias M7 $\sim$ M10. The mixer attains the mixed waves by a local oscillator signal with a large amplitude to drive M7 $\sim$ M10 such that the IF currents in M4 and M6 can be changed. According to [4], the conversion gain G_c of the double balanced mixer is as follows,

$$\begin{aligned} G_c &= \frac{V_{out}}{V_{IF}} \\ &= \frac{2}{\pi} \times \frac{m \cdot g_{m_{3,5}} g_{m_{4,6}} Rc^2}{1 + g_{m_{3,5}} R_{E2}} \frac{2R_T}{1 + 2R_s g_{m_{1,2}}} \times G_d \\ &= \frac{2}{\pi} \times g_{m_c} R_T \times G_d, \end{aligned} \tag{1}$$

where $m = \frac{i_{d3,5}}{i_{d4,6}}$, $g_{m_1} \sim g_{m_6}$ are the transconductances of M1 $\sim$ M6, respectively. G_d is the voltage gain of the output differential amplifier. A source degeneration resistor R_s is inserted between the sources of M1 and M2 in Fig. 2 to increase the mixer's linearity, i.e., IIP3. Notably, a large R_s can improve the linearity with the loss of the gain of the mixer. Moreover, since DVB-T is a wide band broadcasting system, the proposed mixer does not use LC parallel resonant circuitry. The reason is that the required high quality factor and narrow band are not suitable to be directly applied in SOC (System-on-Chip) designs. Although the proposed mixer without any LC resonant circuitry possesses a low conversion gain, the following output differential amplifier stage can provide a high gain to compensate the gain loss, the AAF stage is able to remove the unwanted signals.

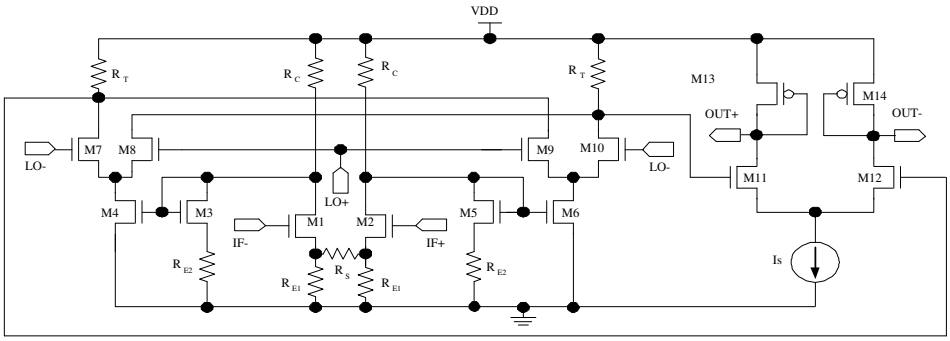

Fig. 2. Current folded-mirror mixer circuitry

2.2 Wideband Digital VGA Design

If AGC designs are classified by feedback signals provided by baseband digital signal processing (DSP) units, there are two types: analog-controlled loop and

digital-controlled loop [5]. Notably, the former needs a digital to analog converter (DAC) to convert the digital feedback signals from the DSP into analog signals. Hence, the digital-controlled loop obviously has the edge. However, the digital VGA in the prior digital-controlled loop-based AGCs encounters different design problems. CDN (current division network) proposed in [5] possesses low bandwidth ($\leq$ 18 MHz). By contrast, though the DDP (degeneration differential pair) approach in [6] resolved the bandwidth difficulty, it requires a lot of resistors to attain the gain-tuning effect which in turn consumes large chip area and produces thermal noise problems. We, thus, propose a novel VGA to resolve these problems in the following context.

2.2.1 Variable gain amplifier in the automatic gain control loop

Since it is highly difficult to use a single VGA to realize a very wide dynamic range of gain tuning, we utilize 3 stages of individual DVGAs to attain the required 70 dB dynamic range, wide bandwidth, and decibel linearity. As shown in Fig. 3, the range of the first DVGA is 0 to 30 dB with a 10-dB gain step; the second stage is aimed at 0 to 10 dB range with a 2-dB gain step; and the last stage is -30 to 0 dB with a 10-dB gain step. The ratio of the range to the gain step in each stage determines the number of gain blocks required therein. If the number of gain blocks in a single VGA is increased, the decibel linearity will be likely to be decreased. After lots of detailed simulations, 3 to 5 is found to be a good option of the number of gain blocks in each DVGA stage.

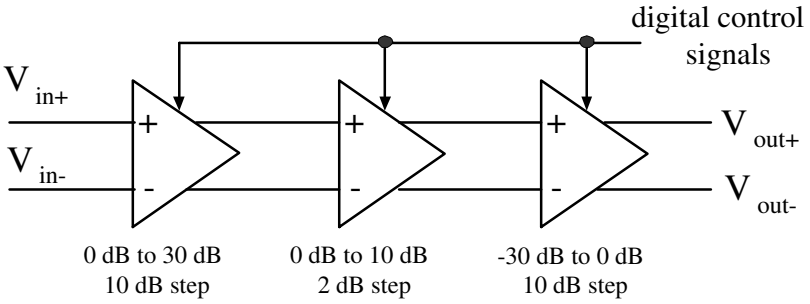

Fig. 3. Architecture of the AGC

2.2.2 Schematic of the digital variable gain amplifier

Referring to Fig. 4, the schematic of the proposed DVGA is revealed, where V_{in+} and V_{in-} are differential inputs, V_{o+} and V_{o-} are a pair of differential outputs, and D_i and $\overline{\mathrm{D}}_i$, $i = 1 \ldots N$, are digital control signals. The input stage of the DVGA is a fully differential degeneration amplifier. The gain blocks controlled by D_i and $\overline{\mathrm{D}}_i$, $i = 1 \ldots N$, are used to change the summation currents, I_{o+} and I_{o-}, such that the overall gain can be adjusted by the digital

signals. Besides, a common mode feedback (CMFB) circuitry is employed to stabilize the common-mode voltage of the amplifier.

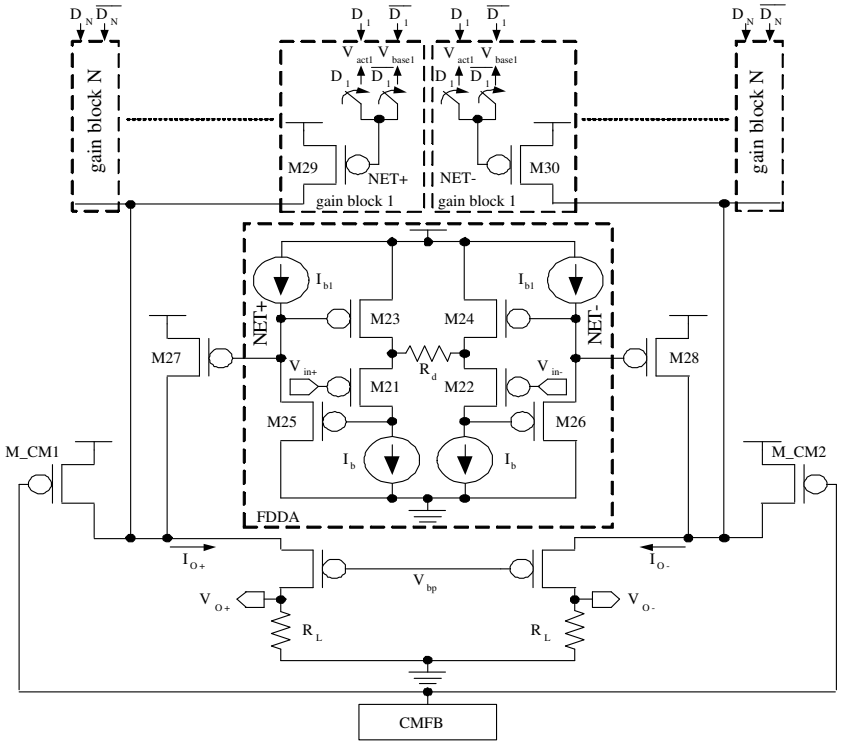

Fig. 4. Schematic of the DVGA

Fig. 5 is the simplified schematic of a fully differential degeneration amplifier. The transconductance and the gain of the amplifier is summarized as follows.

$$g_m\text{diff} = \frac{g_{m21}}{1 + g_{m21} \cdot \frac{R_d}{2}}, \tag{2}$$

$$A_v = \frac{R_L}{\frac{R_d}{2} + \frac{1}{g_{m21}}}, \tag{3}$$

where g_{m21} is the transconductance of M21 and M22. Obviously, the voltage gain is increased with g_{m21}. It implies that a g_m-boosting circuit will be helpful in this regard. Hence, a g_m-boosting circuit [7], [8] in Fig. 6 is used to increase the gain. The boosted transconductance is derived to be

$$g_m = \frac{I_3}{V_{in}} = g_{m21} \cdot (1 + g_{m23} R_{AL}), \tag{4}$$

where g_{m23} is the transconductance of M23, and R_{AL} is the equivalent impedance looking into the current sink, I_b. The overall fully differential degeneration

amplifier with the g_m-boosting circuit is given in Fig. 7. Thus, the gain is enhanced to be

$$A_v = F \cdot \frac{R_L}{\frac{R_d}{2}}, \tag{5}$$

where F is the current ratio from M23 to M27.

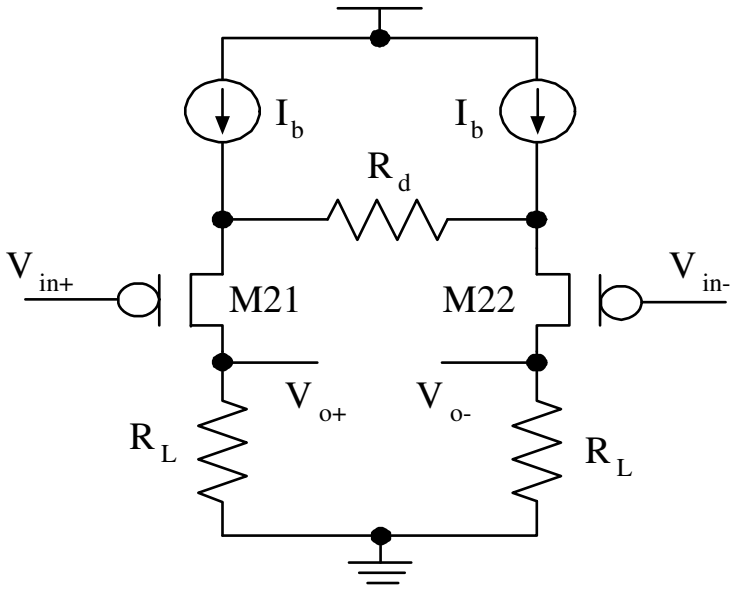

Fig. 5. Simplified schematic of the DVGA

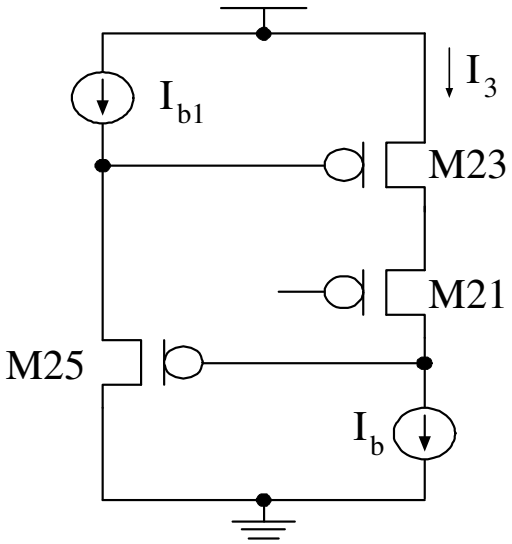

Fig. 6. g_m-boosting circuit

According to Eqn. (5), the gain can be adjusted by two parameters: the resistance ratio and the current mirror gain. However, since the resistors will cause

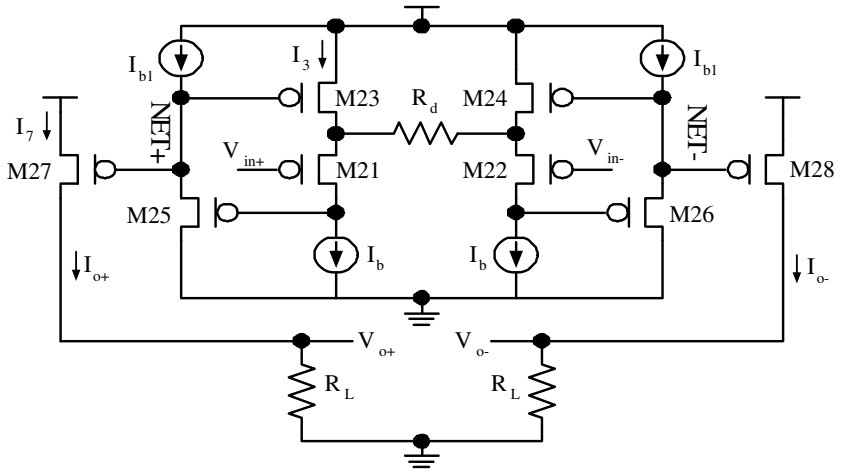

Fig. 7. Fully differential degeneration amplifier with the g_m-boosting circuit

large chip area consumption and unwanted thermal heat problem, we tend to use the variation of current mirror gain to achieve the gain tuning function. In other words, different current sources in the gain blocks as shown in Fig. 4 provide a variety of current ratio compared to I_3. The digital control signals, D_i and $\overline{\mathrm{D}}_i$, $i = 1 \ldots N$, are used to determine the ON/OFF of the current source in each gain block such that the overall gain can be adjusted.

A common mode feedback circuit is required to stabilize the common mode voltage of the fully differential degeneration amplifier. The average of I_{o+} and I_{o-} is mirrored to input of the common mode feedback circuitry in Fig. 8, where V_{oCM} denotes the common mode voltage. Thus, the following derivation can be concluded.

$$\begin{aligned} I_{o+} + I_{o-} &= [\frac{V_{oCM}}{R_L} + i_{act+}] + [\frac{V_{oCM}}{R_L} - i_{act-}] \\ &= 2 \cdot \frac{V_{oCM}}{R_L} \\ \frac{I_{o+} + I_{o-}}{2} &= \frac{V_{oCM}}{R_L}, \end{aligned} \tag{6}$$

where i_{act+} and i_{act-} represent the total current supplied by all of the gain blocks. Then, by the feedback loop in Fig. 8, the V_{ref} can be determined.

$$V_{oCM} = \left(\frac{I_{o+} + I_{o-}}{2} + I_{CM} \right) \cdot R_L = V_{\mathrm{ref}}, \tag{7}$$

where I_{CM} is the current via PMOS M_CM. By mirroring the I_{CM} to the branches of M_CM1 and M_CM2 in Fig. 4, the common voltage is fixed to be V_{ref}.

Undoubtedly, the V_{ref} plays a critical role in the success of the entire design.

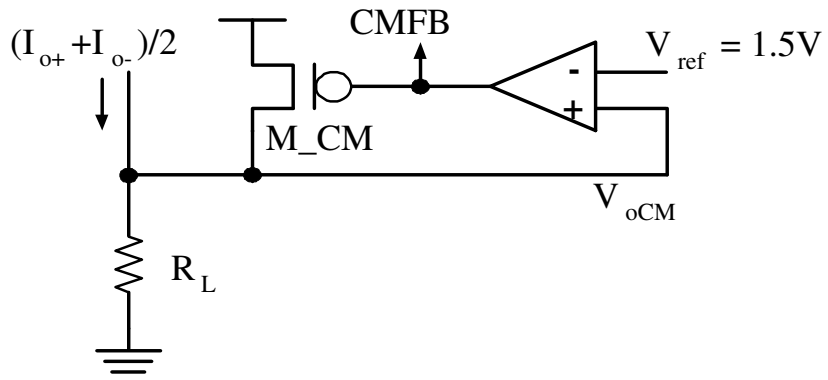

Fig. 8. CMFB circuitry

We utilize a step-down regulator to reject the noise coupled in power supplies to the bandgap bias which provides V_{ref} in Fig. 8.

2.3 Gm-C Anti-Aliasing Filter Design

2.3.1 Anti-aliasing filter

Traditional RC-based filters with passive elements can not be directly applied in SOC (System-on-Chip) designs due to large area cost. Although operation amplifiers can be used to replace large passive elements, e.g., inductors and capacitors, they are limited for high-frequency usages. By contrast, transconductance amplifiers have the following advantages : the transconductance varying with bias voltages, operating in a wide frequency range, high input impedance, and high output impedance. Besides, they can be used as large resistors given proper configurations. Hence, the Gm-C filter based on transconductance amplifiers is better than the operation amplifier-C filter regarding applications in the SOC designs, [9], [10], [11].

A 6th order Gm-C AAF is proposed in Fig. 9 which is basically a 6th order passive LC ladder filter [12]. In order to carry out the feasibility, the passive inductors are replaced with active inductors, while the resistors are replaced with active Gm elements.

Referring to Fig. 10, which is the architecture of Nauta's transconductor [9]. Assume that all inverters in Fig. 10 are identical. The V-I transfer function of the transconductor is as follows.

$$\begin{aligned} I_{od} &= I_{o1} - I_{o2} \\ &= V_{id} \cdot (V_{DD} - V_{thn} + V_{thp}) \cdot \sqrt{\beta_n \cdot \beta_p} \\ &= V_{id} \cdot g_{m_N}, \end{aligned} \tag{8}$$

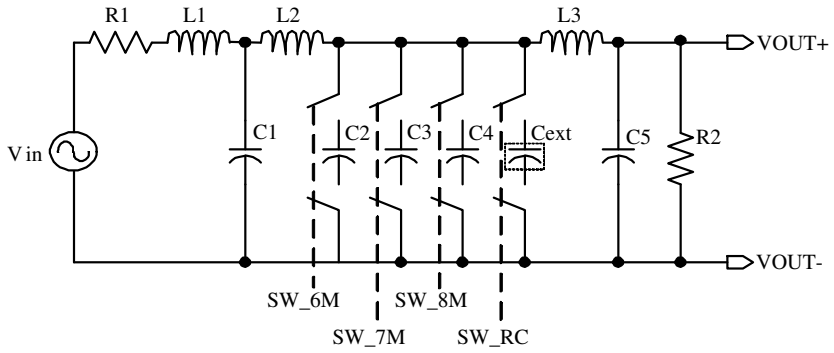

Fig. 9. 6th order passive LC ladder filter

where V_{id} is the differential input voltage, V_{thn} and V_{thp} are the threshold voltages of NMOS and PMOS transistors, respectively, β_n and β_p are the transconductance parameters of NMOS and PMOS transistors, respectively, and g_{m_N} is the equivalent transconductance of Nauta's transconductor. The transconductor can be denoted as a single element.

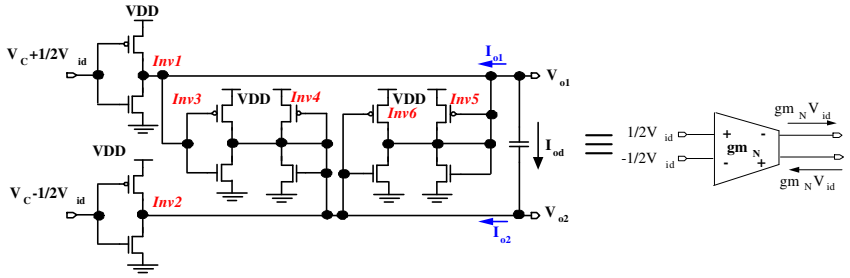

Fig. 10. Nauta's symmetric transconductor

Passive inductors usually occupy large area on chip, which is not acceptable in SOC designs. Hence, we utilize the symmetrical floating gyrator in Fig. 11 instead, which is equivalent to an inductor [13]. The equivalent inductance, thus, is derived as follows.

$$L_{eq} = \frac{V}{I} = \frac{C_L}{{g_{m_N}}^2}, \tag{9}$$

The resistor can also be replaced with the symmetric transconductor in Fig. 10. Fig. 12 shows the equivalent circuit of the resistor.

$$R_{eq} = \frac{V}{I} = \frac{V}{g_{m_N} \cdot V} = \frac{1}{g_{m_N}} \tag{10}$$

The DVB-T specifications [1] require three different baseband bandwidths: 6, 7, and 8 MHz. Therefore, the cut-off frequencies thereof are set to 7.5, 8.0, and 8.5 MHz, respectively. In order to meet the requirements, the digital controlled

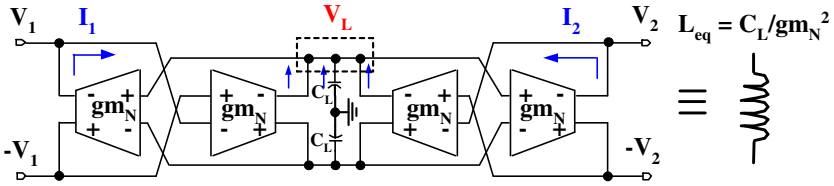

Fig. 11. Symmetrical floating gyrator which is equivalent to an inductor

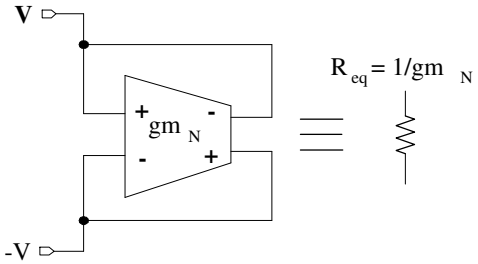

Fig. 12. Equivalent circuit of the resistor

switches, SW_6M, SW_7M, SW_8M in Fig. 9, are used in the AAF circuit such that the bandwidth of the output signal can be selected. Notably, SW_RC is added to select an external RC filter for the purpose of testing.

2.3.2 High PSRR regulator

The Gm-C filter needs a stable bias to resist the variations of power supply voltage and temperature. Fig. 13 shows a high PSRR (power supply rejection ratio) regulator which provides a stable voltage to all of the AAF sub-circuits. Besides, a voltage divider composed of resistors supplies 1.5 V voltage to the AGC as the common mode voltage such that the following analog to digital converter can attain maximum input signal swing. The post-layout simulations prove that when the power supply voltage varies within ±15 %, the output voltage drift of the regulator is reduced to be less than ±4 %.

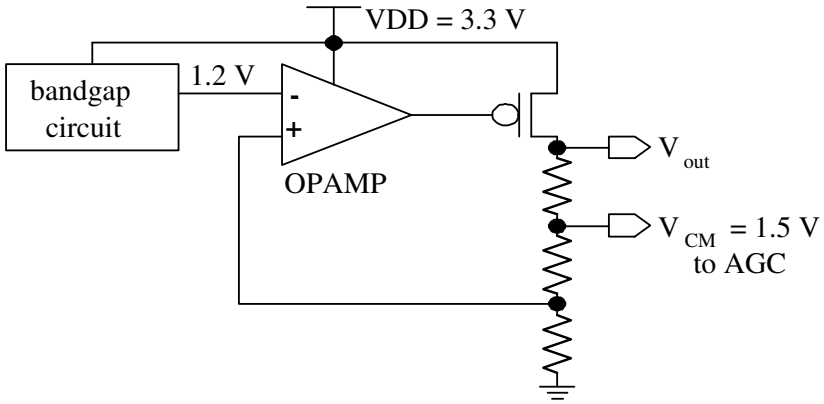

Fig. 13. High PSRR regulator

2.3.3 Temperature-compensated transconductor

The g_{m_N} of the Nauta's symmetric transconductor varies with the temperature drifting, because there is no protection or compensation devices in the circuit. Consequently, the filtering bandwidth will be drifting, and unwanted noise might appear. Hence, a modified Nauta's symmetric transconductor structure as shown in Fig. 14 is employed. The NMOS transistors (M41 $\sim$ M46), namely foot switches, are inserted between the GND and the pull-down NMOS in each inverter as a tail current control mechanism. If V_{bias} provides a stable voltage to fix the bias current, the g_{m_N} will be kept at a constant to reduce the variation of the filtering bandwidth. The V_{bias} voltage in Fig. 14 is generated by a temperature-compensated circuit shown in Fig. 15. Assume that M51 $\sim$ M52 and M53 $\sim$ M55 are two identical pairs, and Q2 has an emitter area n times larger than that of Q1. Given that $V_x = V_y$, the current I_{PTAT} is proportional to the absolution temperature (PTAT) by

$$I_{PTAT} = \frac{V_T \ln n}{R_b}, \tag{11}$$

where V_T is the thermal voltage with a positive temperature coefficient. Thus, V_{bias} is derived to be,

$$V_{bias} = \sqrt{\frac{2I_{PTAT}L_{eff}}{KP \cdot W_{eff}}} + V_{thn}, \tag{12}$$

where W_{eff} and L_{eff}, respectively, denote the effective channel width and length, KP and V_{thn} are the transconductance parameters and the threshold voltage of M56, respectively. The temperature coefficient of V_{bias} is obtain as follow,

$$\begin{aligned} TC_{V_{bias}} &= \frac{1}{V_{bias}} \frac{\partial V_{bias}}{\partial T} \\ &= (\frac{2I_{PTAT}L_{eff}}{KP \cdot W_{eff}})^{\frac{1}{2}} \cdot (TC_{I_{PTAT}} - TC_{KP}) \\ &\quad \cdot \frac{1}{2V_{bias}} + V_{thn}TC_{V_{thn}}, \end{aligned} \tag{13}$$

where $TC_{I_{PTAT}} = \frac{1}{I_{PTAT}} \frac{\partial I_{PTAT}}{\partial T}$, $TC_{KP} = \frac{1}{KP} \frac{\partial KP}{\partial T}$, and $TC_{V_{thn}} = \frac{1}{V_{thn}} \frac{\partial V_{thn}}{\partial T}$, which are the temperature coefficients of I_{PTAT}, KP and V_{thn}, respectively. According to [3], KP and V_{thn} exhibits a negative temperature coefficient. Hence, the value of I_{PTAT} (or R_b) and the size of M56 can be appropriately tuned such that the sum of the three terms in Eqn. (13) gives a zero temperature coefficient.

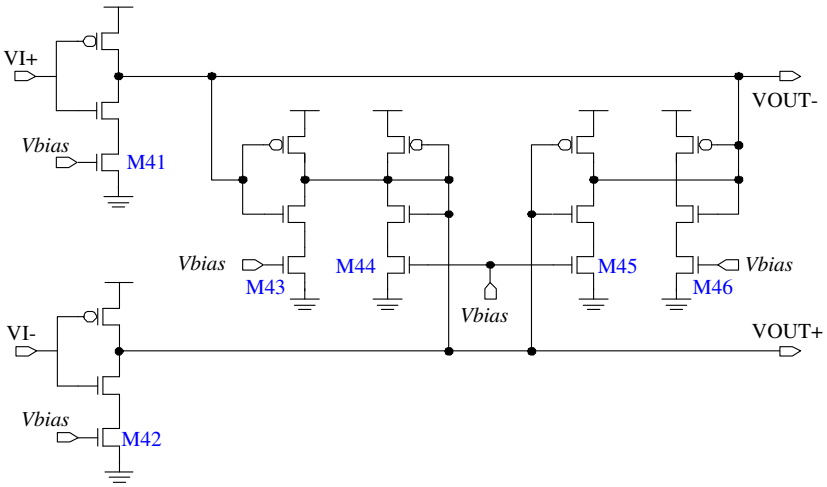

Fig. 14. Modified Nauta's symmetric transconductor

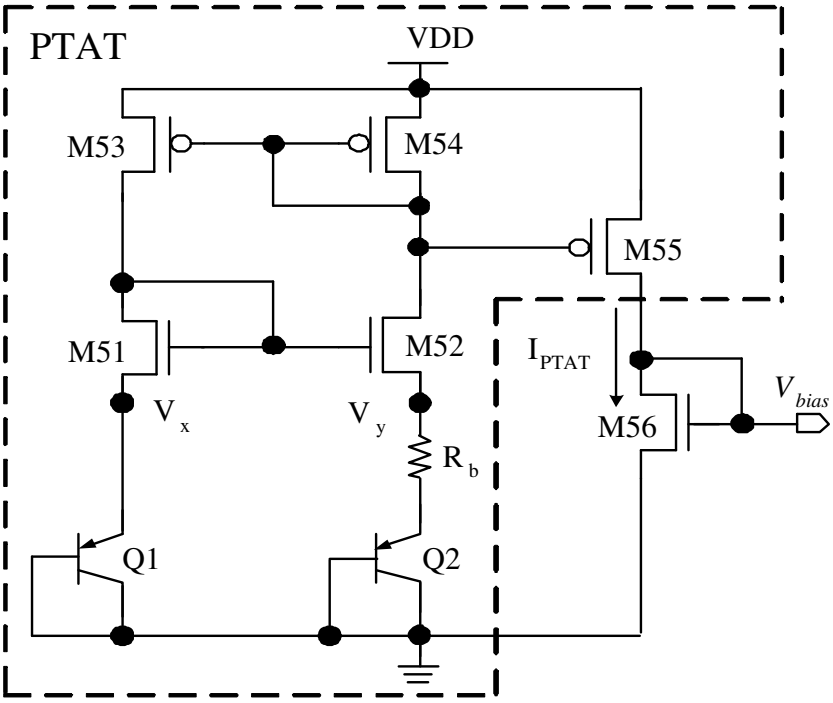

Fig. 15. Temperature-compensated circuit

3 Simulation, Implementation and Measurement

3.1 Simulation

In order to verify the performance of the proposed IFC, TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process is adopted to carry out the proposed design. Table 1 summarizes the specifications of the proposed IFC.

3.1.1 Down-conversion mixer

The operating conditions of the down-conversion mixer is summarized in Table 2. The characteristics of the down-conversion mixer are tabulated in Table 3.

3.1.2 Automatic gain controller

The worst-case (SS model, VDD = 2.97 V, 75^{o}C) post-layout simulations of the bandwidth and the gain error of the AGC are revealed, respectively, in Fig. 16 and Fig. 17, given all of the process, voltage, and temperature corners. The maximum dynamic gain range at $f_{3\mathrm{dB}}$ = 95 MHz is [-30, +40] dB. The gain error is no more than 0.3 dB. The overall design characteristics of the proposed DVGA are tabulated in Table 4.

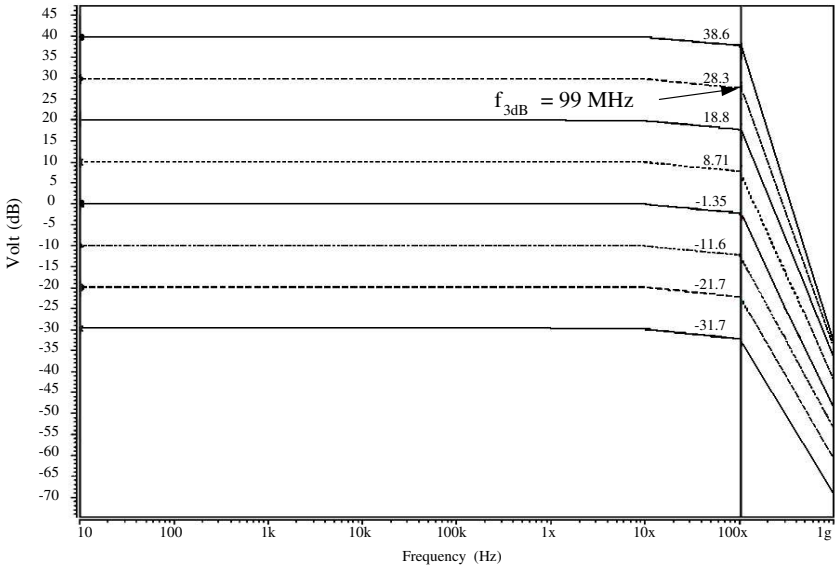

Fig. 16. Gain response of the proposed DVGA by post-layout simulations

3.1.3 Anti-aliasing filter

Fig. 18 shows the post-layout simulations of the frequency response of our AAF given 6 MHz baseband bandwidth at TT model, VDD = 3.3 V, 25^{o}C. Given the 6 MHz baseband bandwidth with a 7.5 MHz cut-off frequency, TT model and all of the process, and voltage corner simulation results are revealed in Fig. 19. The accuracy of the cut-off bandwidth is 3.28% in the worst case. The power consumption is 33.58 mW.

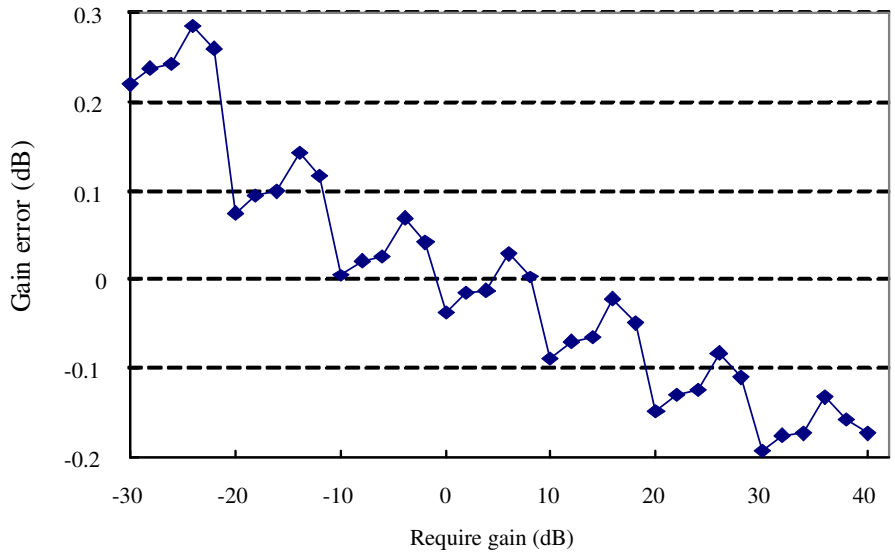

Fig. 17. Gain error of the DVGA by post-layout simulations

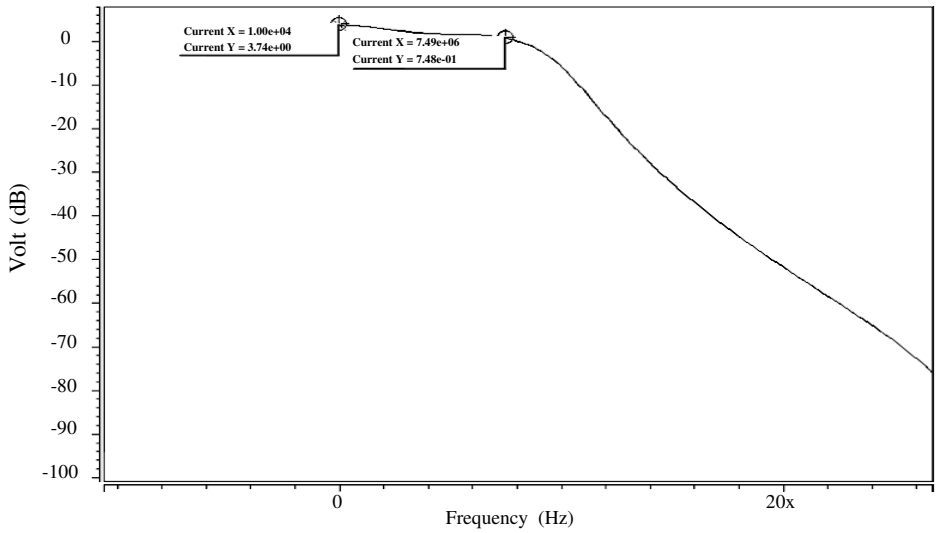

Fig. 18. Post-layout simulation of 6 MHz baseband bandwidth, at TT model, VDD = 3.3 V, 25^{o}C

3.1.4 Integrated simulation

Finally, the down-conversion mixer, the AGC, and the AAF are integrated to carry out a full-scale simulation. Fig. 20 shows the simulations of the conversion gain, where point "A" is a -20 dBm, 36 MHz signal, point "B" is the mixer's output signal. Hence, the conversion gain is -7.9 dBm. The IIP3 and P_{1dB} plots are shown in Fig. 21 and Fig. 22, respectively, to justify the decibel linearity of the proposed design. The characteristics of the proposed mixed-signal converter are summarized in Table 5.

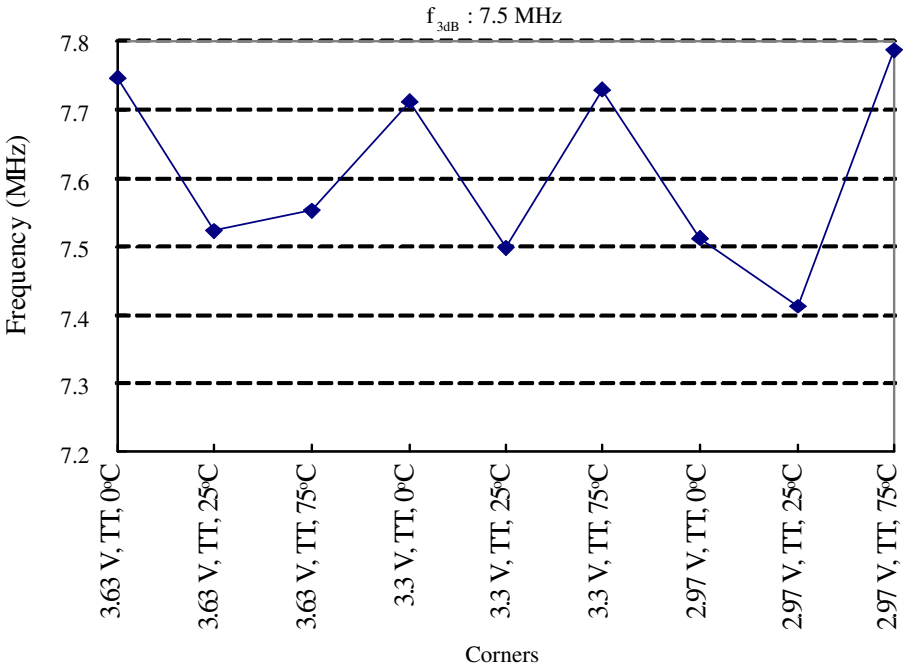

Fig. 19. Post-layout simulation of 6 MHz data bandwidth (all PVT corners)

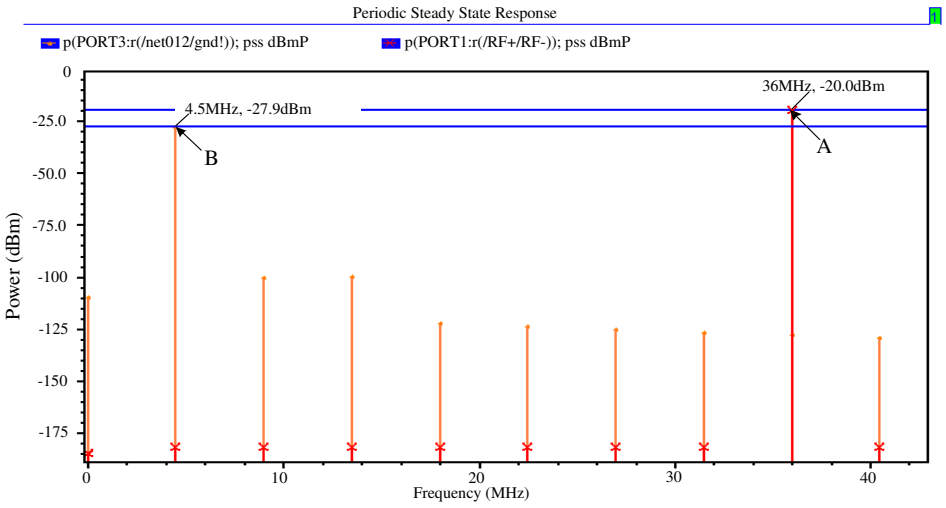

Fig. 20. Conversion gain of the peoposed IFC

3.2 Implementation and Measurement

The IFC chip implemented by the 0.35 μm 2P4M CMOS process is shown in Fig. 23. Agilent infiniium oscilloscope 600 MHz 4GSa/s, HP 89441A DC-2650 MHz vector signal analyzer, HP 8563E spectrum analyzer, HP E4433B ESG-D series signal generator, and HP 8656B signal generator are used to perform chip testing and measurement. A -20 dBm, 36 MHz and a 0 dBm, 40.5 MHz sine waves are input to the IF and the LO ports, respectively. Fig. 24 demon-

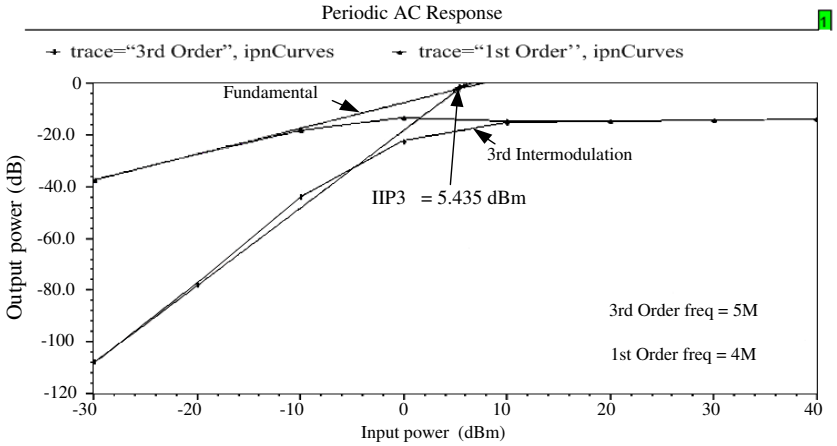

Fig. 21. IIP3 plots

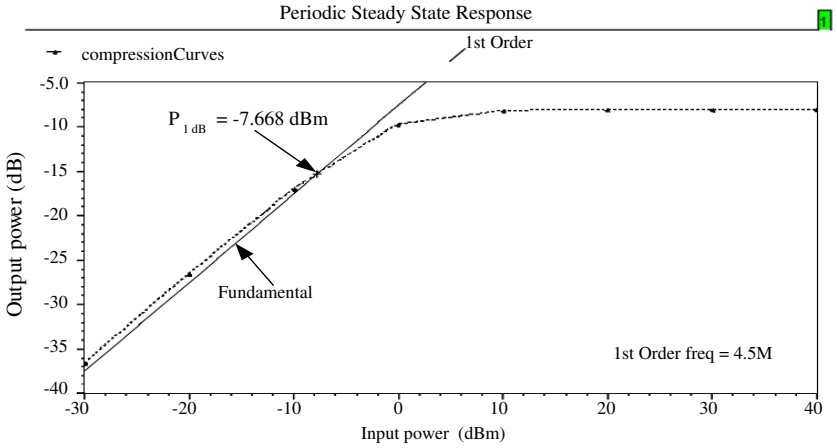

Fig. 22. P_{1dB} plot

strates the measurement waveform and spectrum of the output where a 4.5 MHz tone is present. The measurement result of the IIP3 is shown in Fig. 25, which uses two separate tones separated by 0.5 MHz apart. Fig. 26 shows the measurement frequency response given a 6 MHz baseband bandwidth (7.5 MHz cut-off frequency). The measurement conditions and the measurement results of the proposed IFC are summarized in Table 6 and Table 7, respectively.

4 Conclusion

We have proposed a CMOS single chip IF band converter for DVB-T receivers. The proposed IFC converts a 36 MHz IF input into a 4.5 MHz baseband signal. The down-conversion mixer adopts the current folded-mirror architecture to provide a superior performance in conversion gain and linearity. The AGC

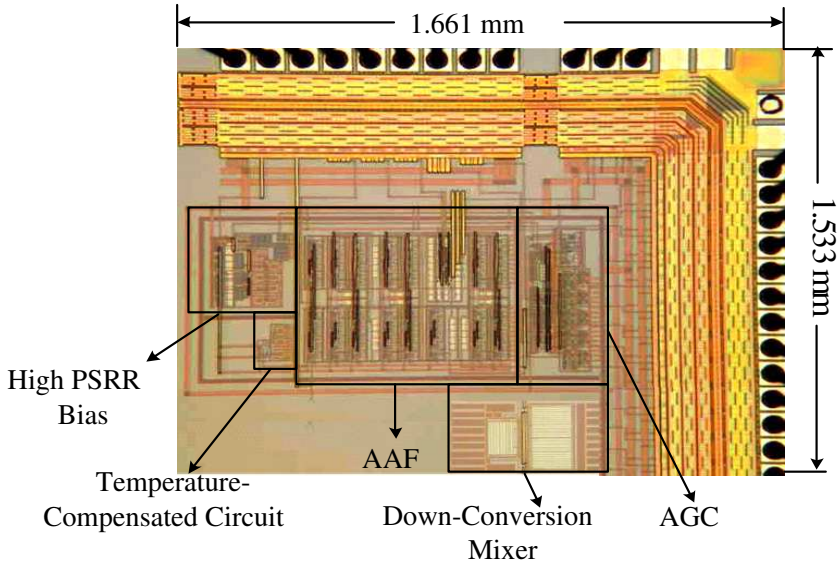

Fig. 23. Die photo of the proposed IFC

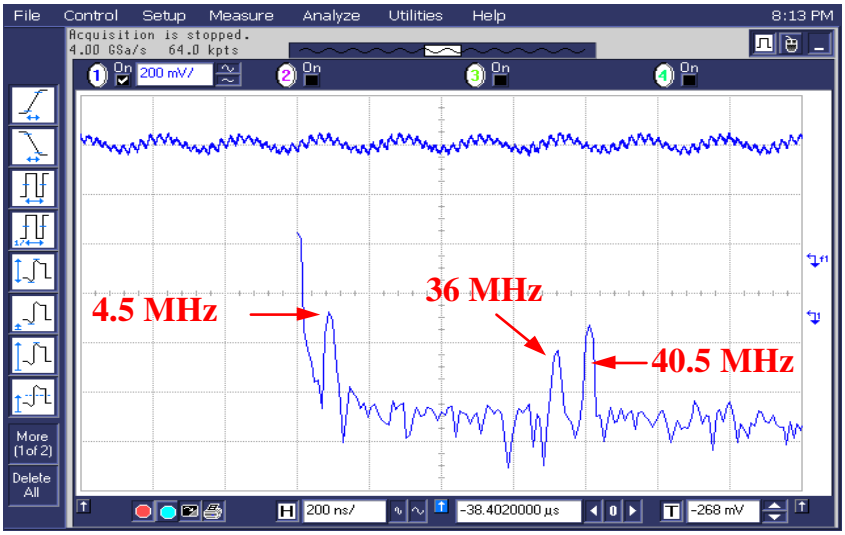

Fig. 24. Measurement spectrum of the output

based on a DVGA composed of a plurality of gain blocks and a fully differential degeneration amplifier. The gain tuning required by DVB-T receivers can be carried out by digital signals selecting proper gain blocks. The AAF employs the modified Nauta's symmetric transconductor to suppress the *gm* and filtering channel bandwidth variations because of temperature drifting.

5 Acknowledgement

This research was partially supported by National Science Council under grant NSC94-2213-E-110-022 and NSC94-2213-E-110-024. Furthermore, the authors

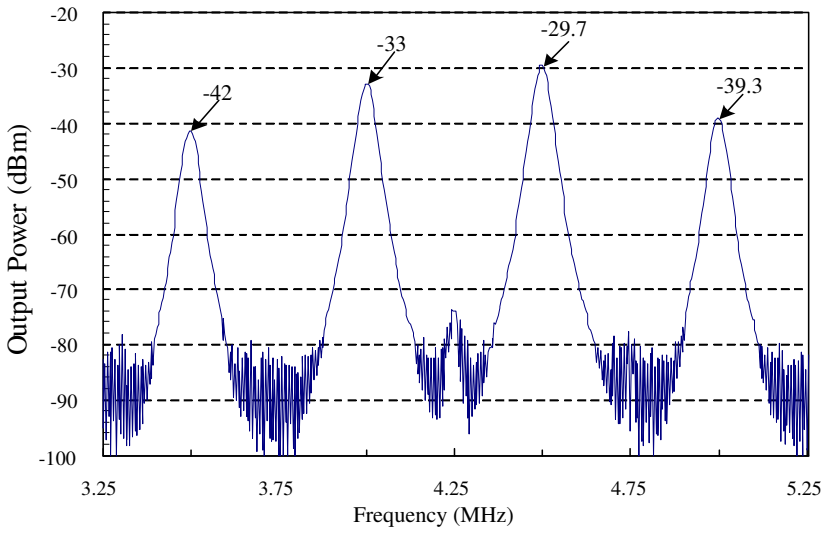

Fig. 25. Measurement spectrum for calculating the IIP3

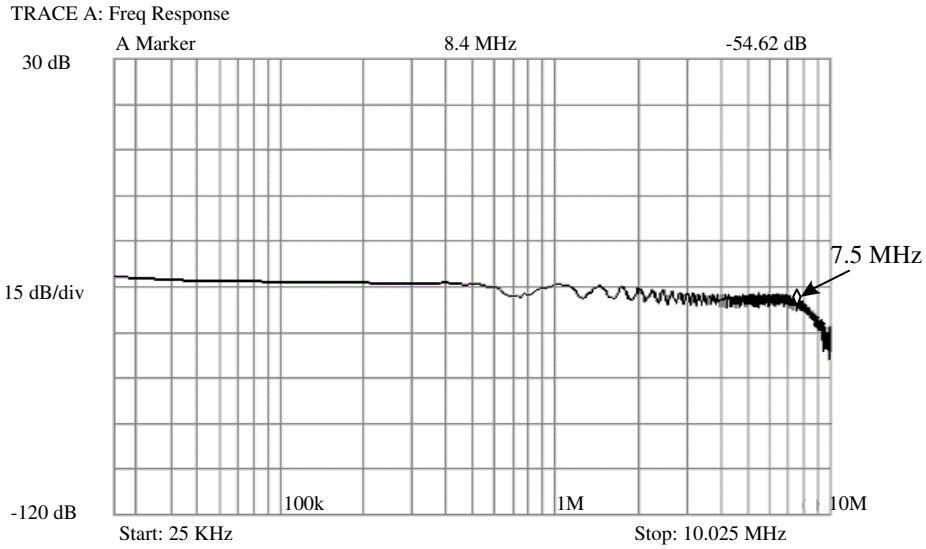

Fig. 26. Measurement frequency response given a 6 MHz baseband bandwidth (7.5 MHz cut-off frequency)

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Figure Captions

Tables

Table 1
Specifications of the proposed IFC

Parameter	Specification
Conversion gain without DVGA's gain	$>$ -10dB
Conversion gain with max. DVGA's gain	$>$ 30 dB
Noise figure	$<$ 15 dB
IIP3	$>$ 0 dBm
P_{1dB}	$>$ -10 dBm
AGC control range	-30 $\sim$ 40 dB
Channel bandwidth	6, 7, 8 MHz (digitally tunable)

Table 2
Summary of the mixer's operating conditions

	Values
VDD	3.3 V
IF frequency	36 MHz
IF power	-20 dBm
LO frequency	40.5 MHz
LO power	0 dBm

Table 3
Characteristics of the down-conversion mixer

Conversion gain	-6.7 dB
IIP3	5.915 dBm
Noise figure	12 dB

Table 4
Characteristics of the proposed DVGA design

Bandwidth	95 MHz
Dynamic range	70 dB
Gain step	2 dB
Gain accuracy	< 0.3 dB
IIP3	-1.962 dBm
Power	32.7 mW@95 MHz

Table 5
Characteristics of the proposed IFC

Conversion gain	-7.9 dB
IIP3	5.435 dBm
P_{1dB}	-7.668 dBm
Power consumption	75.5 mW
(Down-conversion Mixer+AGC+AAF)	

(Note : The gain of the DVGA is set to 0 dB.)

Table 6
Measurement conditions of the proposed IFC

VDD	3.3 V
IF frequency	36 MHz
IF power	-20 dBm
LO frequency	40.5 MHz
LO power	0 dBm

Table 7
Measurement results of the proposed IFC

Conversion gain without DVGA's gain	-9 dB
Conversion gain with max. DVGA's gain	31 dB
Noise figure	18 dB
IIP3	1.2 dBm
P_{1dB}	-8 dBm
IF isolation	39 dB
LO isolation	42 dB
Power consumption	115.5 mW
Die size	1.661×1.533 mm^2