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70 dB DYNAMIC RANGE CMOS WIDEBAND DIGITAL VARIABLE GAIN AMPLIFIER FOR AGC IN DVB-T/H RECEIVERS *

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Abstract. This paper presents a novel variable gain amplifier (VGA) design which is applied in the automatic gain control (AGC) loop of DVB-T/H receivers. The VGA composed of three cascaded tunable gain stages to provide a 70 dB dynamic range with 2 dB gain steps. Each gain stage is based on a digital variable gain amplifier (DVGA) which is composed of a plurality of gain blocks (GBs) and a fully differential degeneration amplifier (FDDA). The GBs are digitally controlled current mirrors. A common-mode feedback (CMFB) circuitry is used to stabilize the FDDA by providing a stable common mode voltage. Physical measurements on silicon show that the gain error is merely 0.55 dB given a 70 dB tuning range.
Key words: automatic, control, variable, gain, amplifier.

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1. Introduction

The AGC plays critical roles in many applications, e.g., hearing aids, hard disk drives, and particularly portable communication systems. As long as a receiver is required in a wireless system, the signal strength will be likely depend on the distance between the receiver and the transmitter which may cause receiver overloading [3]. The task of the AGC loop is to adjust the gain depending on the received signal automatically such that the strength of the signal transmitted to the signal processing units in baseband modules appear to be close to a constant level no matter what the distance between the receiver and the transmitter is. It is particularly critical in the wireless DVB-T/H receiver to ensure the correctness of the orthogonal frequency division multiplexing (OFDM) demodulation therein.

The standard for digital terrestrial television broadcasting was finalized by the DVB consortium in 1997 [5], which has been known as DVB-T in many countries. The DVB-H is a standard derived from DVB-T for handheld devices. Since DVB-T and DVB-H are very much alike in the physical layer, the AGC loops would be the same, which is why we use “DVB-T/H” to denote that the proposed design can be used in these two standards. DVB-T/H has been deemed as one of the most outstanding standards for the next-generation digital TV [7], [9]. DVB-T/H adopts the coded OFDM modulation scheme with a powerful FEC (forward error correction) code to overcome the serious multipath interference in the terrestrial transmission. The OFDM is a multi-carrier modulation that has been adopted in many modern wireless communication standards thanks to its ability to overcome the multipath frequency-selective fading [13].

The AGC is expected to provide a stable signal level for the following ADC (analog-to-digital converter) as well as the OFDM demodulator. Hence, two important requirements for the AGC in the DVB-T/H receivers besides the gain step are the decibel linearity and the bandwidth. Besides, one long ignored problem in the design of AGC is the peak current overshoot occurring at the change of the gain, which in turn causes power waste and hazards. A novel digital VGA based on a g_m-boosting DVGA is proposed in this work. A current-selecting gain control approach is also presented to suppress the overshoot when the gain is changed. The proposed digital VGA was realized in a 0.35 μm 2P4M CMOS technology. The measurement on silicon show that it possesses a 70 dB dynamic tuning range with a 0.55 dB gain error.

2. Wideband digital VGA design

If AGC designs are classified by feedback signals provided by baseband DSP (digital signal processing) units, there are basically two types : analog-controlled loop and digital-controlled loop, as shown in Fig. 1. Notably, the former needs a DAC (digital-to-analog converter) to convert the digital feedback signals from the

DSP into analog signals. Hence, the digital-controlled loop obviously has the edge. However, the digital VGA in the prior digital-controlled loop-based AGCs encounters different design problems. Current division network (CDN) proposed in [2] and [3] possesses low bandwidth ($\leqq$ 18 MHz). By contrast, though the degeneration differential pair (DDP) approach in [10] resolved the bandwidth difficulty, it requires a lot of resistors to attain the gain-tuning effect which in turn consumes large chip area and produces thermal noise problems.

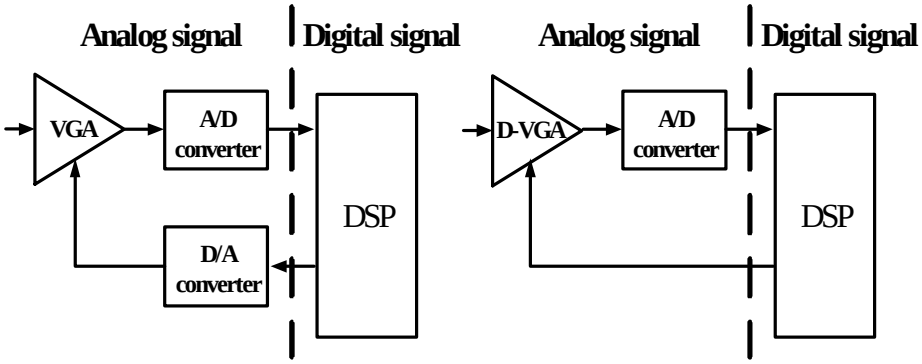

Figure 1. Two types of AGC loops.

2.1 VGA in the AGC loop

Since it is highly difficult to use a single VGA to realize a very wide dynamic range of gain tuning, we propose to utilize 3 stages of individual DVGAs to attain the wide tuning range, wide bandwidth, and decibel linearity. As shown in Fig. 2, the range of the first DVGA is 0 to 30 dB with a 10-dB gain step; the second stage is aimed at 0 to 10 dB range with a 2-dB gain step; and the last stage is -30 to 0 dB with a 10-dB gain step.

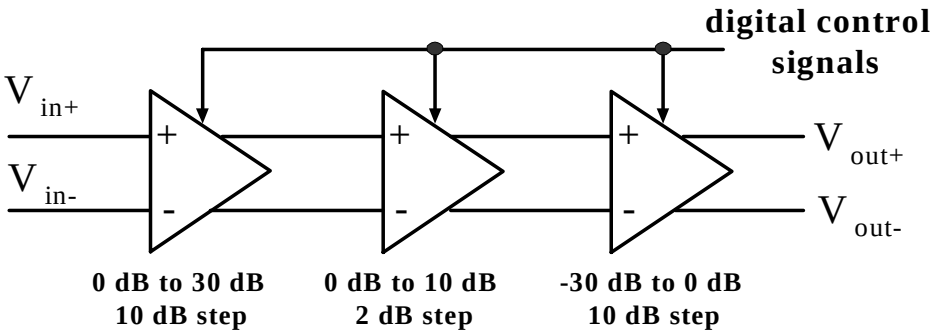

Figure 2. Architecture of the proposed DVGA.

The ratio of the range to the gain step in each stage determines the number of gain blocks required therein. Meanwhile, the gain block which will be disclosed later is composed of digital-controlled current source and switches. If the number of gain blocks in a single VGA is increased, the decibel linearity will be likely to be decreased. After detailed simulations, 3 to 5 are found to be a better option to be the number of gain blocks in each stage.

2.2 Schematic of DVGA

Referring to Fig. 3, the schematic of the proposed DVGA is revealed, where V_{in+} and V_{in-} are differential inputs, V_{o+} and V_{o-} are a pair of differential outputs, and D_i and $\overline{D_i}$, i = 1**…**N, are digital control signals. The input stage of the DVGA is a FDDA shown in Fig. 4 which controls the basic gain of the DVGA. The digital control signals, D_i and $\overline{D_i}$, i = 1**…**N, are used to determine the ON/OFF of the current sources in each gain block, i.e., to change the summation currents, I_{o+} and I_{o-}, such that the overall gain can be adjusted. Besides, a CMFB is employed to stabilize the common-mode voltage of the amplifier.

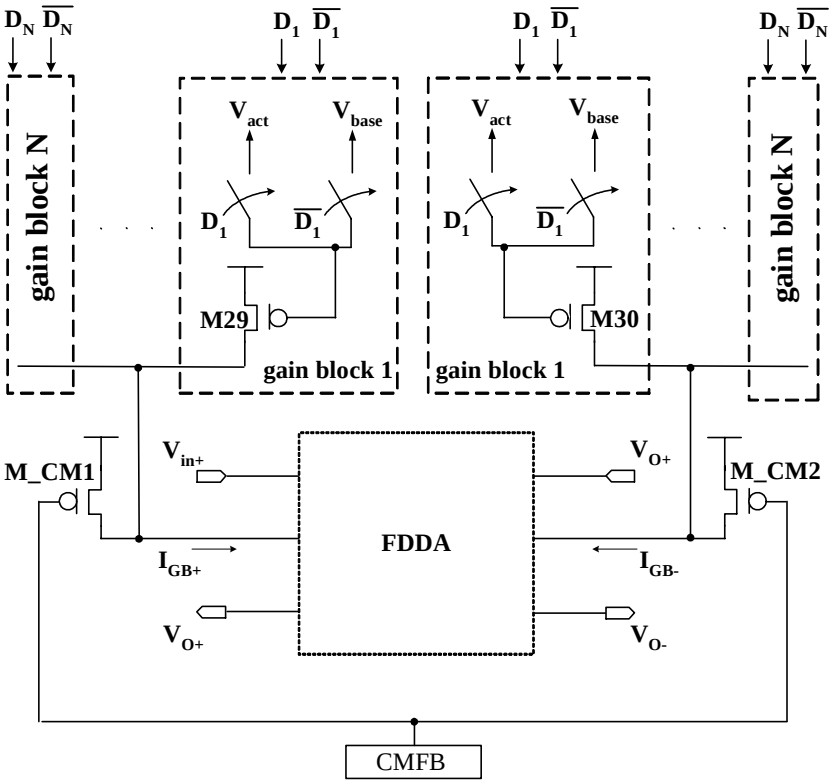

Figure 3. Proposed DVGA with current selecting.

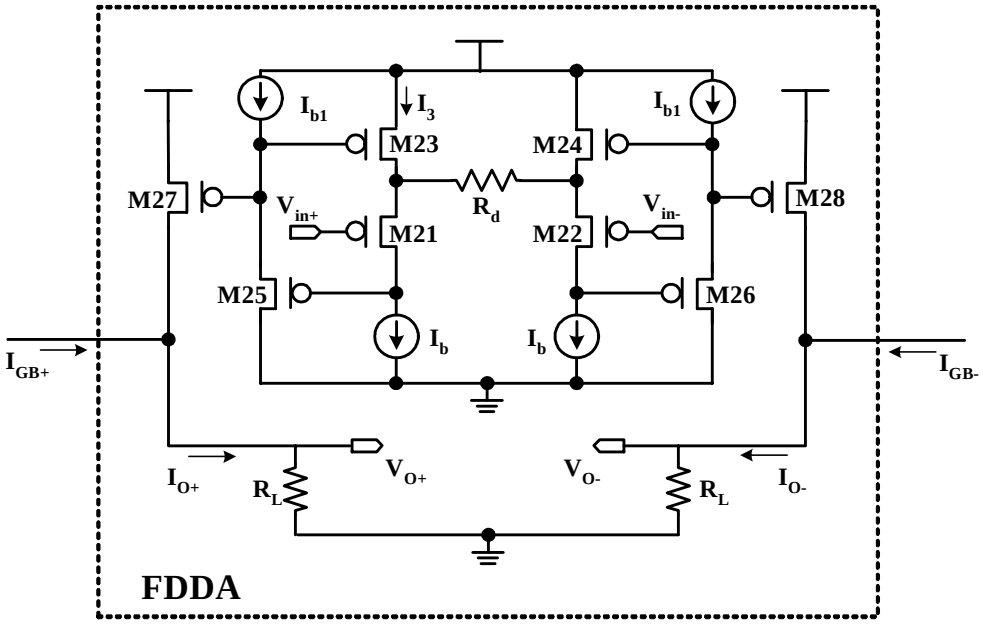

Figure 4. The FDDA in proposed DVGA.

2.2.1 Gain analysis

Fig. 5 is the simplified schematic of the FDDA and the tail current sources.

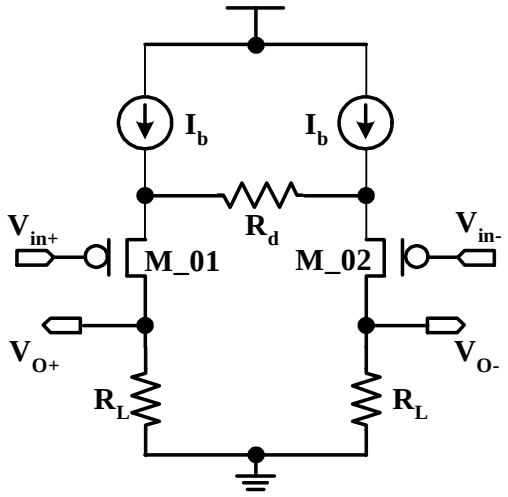

Figure 5. Simplified schematic of the FDDA and the tail current sources.

The transconductance and the gain of the amplifier is summarized as follows.

$$g_{m_{diff}} = \frac{g_m}{1 + g_m \cdot \frac{R_d}{2}}, \tag{1}$$

$$A_v = \frac{R_L}{\frac{R_d}{2} + \frac{1}{g_m}}, \tag{2}$$

where g_m is the transconductance of M_01 and M_02. Obviously, the voltage gain is increased with g_m. It implies that a g_m -boosting circuit will be helpful in this regard.

Hence, a g_m -boosting circuit [11] in Fig. 6 is used to increase the gain [8]. The boosted transconductance is derived to be $g_m = g_{m_{M\_B1}} \cdot (1 + g_{m_{M\_B3}} R_{AL})$, where $g_{m_{M\_B1}}$ and $g_{m_{M\_B1}}$ are the transconductance of M_B1 and M_B3, respectively, and R_{AL} is the equivalent impedance looking into the current sink, I_{bB}.

By a similar configuration, both the V_{in+} and V_{in-}sides in the FDDA are found to be the same as the g_m-boosting configuration as shown in Fig. 6. Therefore, the overall fully differential degeneration amplifier with the g_m -boosting circuit is given in Fig. 4. Thus, the gain is enhanced to be

$$A_v = F \cdot \frac{R_L}{\frac{R_d}{2}}, \tag{3}$$

where F is the current ratio of I_7 to I_3.

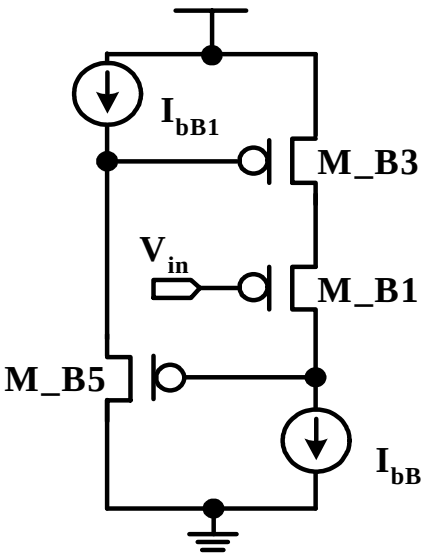

Figure 6. g_m-boosting circuit.

2.2.1 Gain tuning control

According to Eqn. (3), the gain can be adjusted by two parameters : the resistance ratio [9], R_L/R_d, and the current mirror gain [10], I_7/I_3. However, since the resistors will occupy large chip area consumption and introduce unwanted thermal heat problem, we tend to change the current mirror gain to achieve the gain tuning function. In other words, different current sources in the gain blocks as shown in Fig. 3 provides a variety of current ratio compared to I_3 in 4. The digital control signals, D_i and $\overline{D_i}$, i = 1…N,, are used to determine the ON/OFF of the current source in each gain block such that the overall gain can be adjusted.

However, owing to the fact that $V_o = I_o \cdot R_L$, where V_o is either V_{o+} or V_{o-}, I_o is either I_{o+} or I_{o-}, a current spike of I_o causes an overshoot of V_o when the states of MOS-based switches in GBs are flipped to adjust the gain. An example is illustrated in Fig. 7. Such an overshoot might cause gain error besides power waste. Hence, we propose to divide the generated current in each gain block into two partitions : I_{base} and I_{act}. Referring to the Fig. 8, the corresponding gate drives to generate the I_{base} and I_{act} are V_{base} and V_{act}, respectively. If a gain block is not chosen, the gate drive is switched to V_{base} such that a smaller I_{base} is fed to the output current. By contrast, when it is selected, the gate drive is switched to V_{act} such that a bigger I_{act} is supplied. In short, every gain block will supply at least its own I_{base} to avoid the switching overshoot regardless of being activated. Fig. 9 shows the cancellation of the overshoot by this modification.

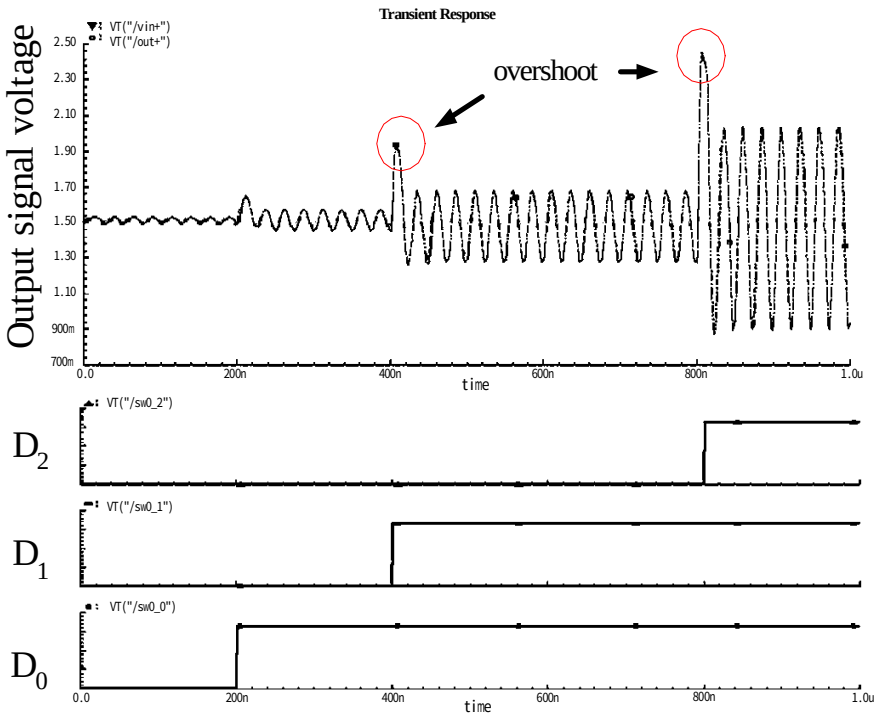

Figure 7. Overshoot syndrome at the gain tuning.

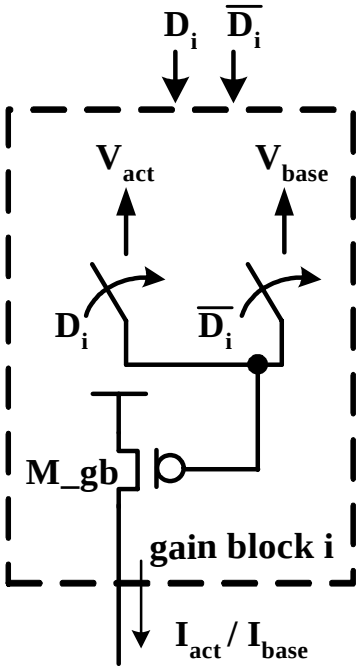

Figure 8. Gain block in proposed DVGA.

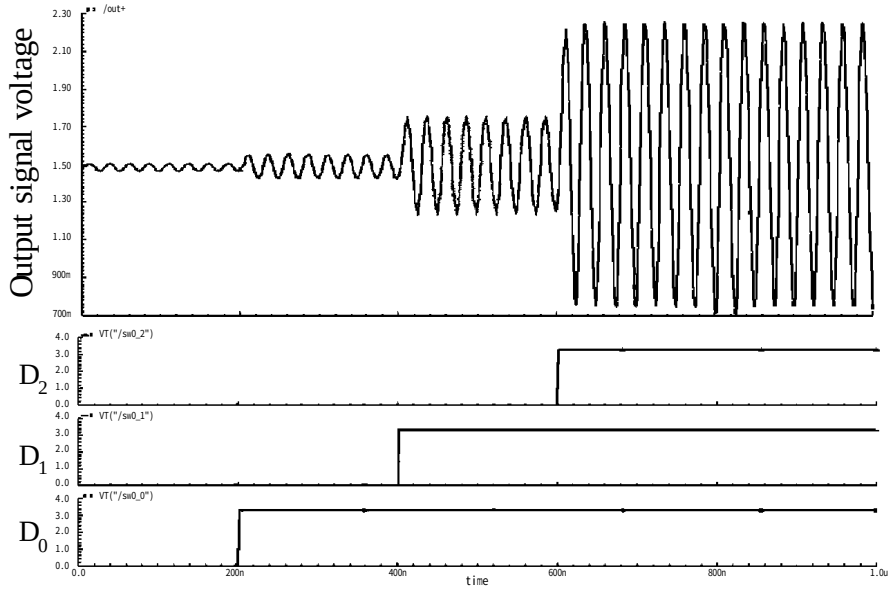

Figure 9. Cancellation of overshoot.

2.2.3 CMFB

A CMFB is required to stabilize the common mode voltage of the fully differential degeneration amplifier [6]. Fig. 10 shows the simplified CMFB circuit in proposed

design, which is the “CMFB” block shown in Fig. 3. Notably, it is an independent circuit block, though the resistance of R_L is identical to that of those R_L s in Fig. 4. Because the VGA is fully differential, there must be a bias circuit, as shown in Fig. 11, to generate the common mode output current ((I_{o+} + I_{o+} / 2)), which is called the average current. The average current is then fed into the CMFB, where V_{oCM} denotes the common mode voltage. Thus, the following derivation can be concluded.

$$I_{o+} + I_{o-} = \left[\frac{V_{oCM}}{R_L} + i_{act+}\right] + \left[\frac{V_{oCM}}{R_L} - i_{act-}\right] = 2 \cdot \frac{V_{oCM}}{R_L},$$

$$\frac{I_{o+} + I_{o-}}{2} = \frac{V_{oCM}}{R_L}, \tag{4}$$

where i_{act+} and i_{act-} represent the total current supplied by all of the gain blocks. Then, by the feedback loop in Fig. 10, the V_{ref} can be determined by the following equation,

$$V_{oCM} = \left(\frac{I_{o+} + I_{o-}}{2} + I_{CM}\right) \cdot R_L = V_{ref}, \tag{5}$$

where I_{CM} is the current via PMOS M_CM. By mirroring the I_{CM} to the branches of M_CM1 and M_CM2 in Fig. 3, the common voltage is fixed to be V_{ref}

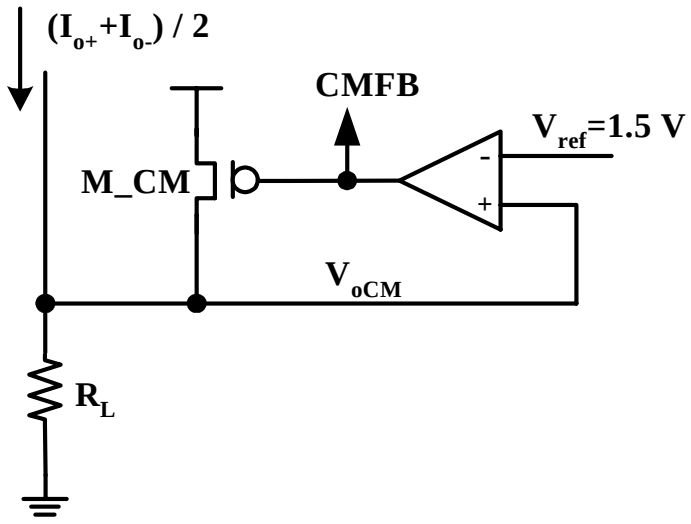

Figure 10. CMFB circuitry.

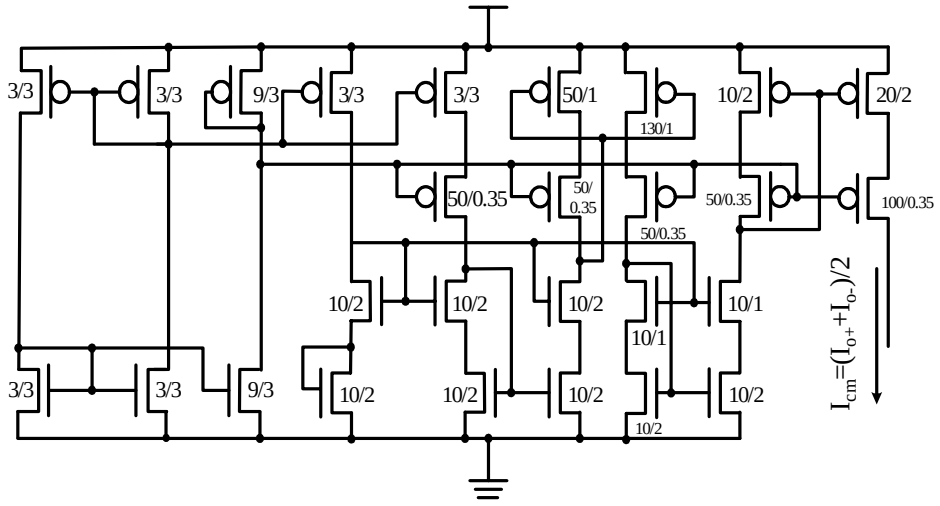

Figure 11. The bias circuit to generate the average current.

Undoubtfully, the V_{ref} plays a critical role in the success of the entire design. We utilize a step-down regulator to reject the noise coupled in power supplies.

3. Simulation and Implementation

TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process is used to carry out the proposed design. The worst-case (FF model, VDD = 3.63 V, 0°C) post-layout simulations of the bandwidth and the gain error are revealed, respectively, in Fig. 12 and Fig. 13, given all of the PVT (process, supply voltage, temperature) corners. The IIP3 plot is shown in Fig. 14 to justify the decibel linearity of the proposed design.

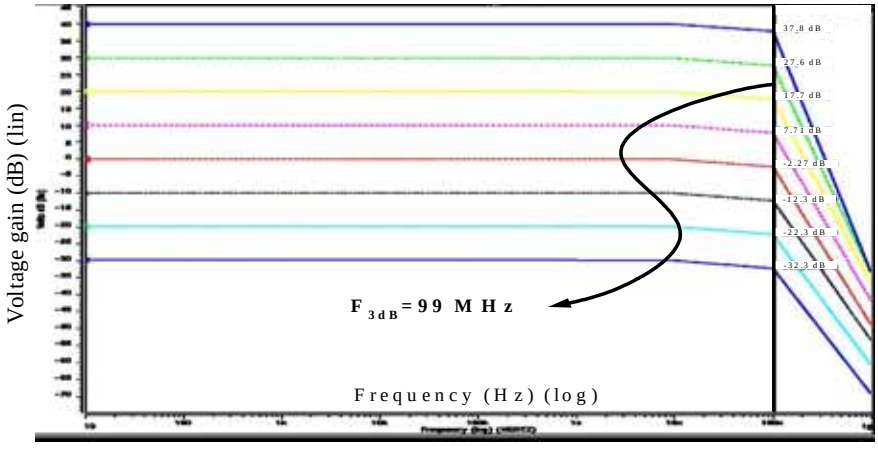

Figure 12. Gain response by post-layout simulations.

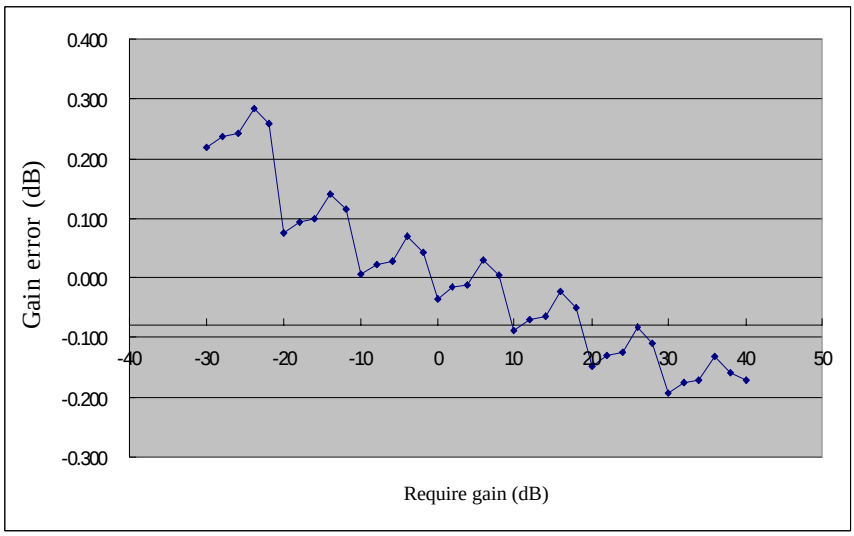

Figure 13. Gain error by post-layout simulations.

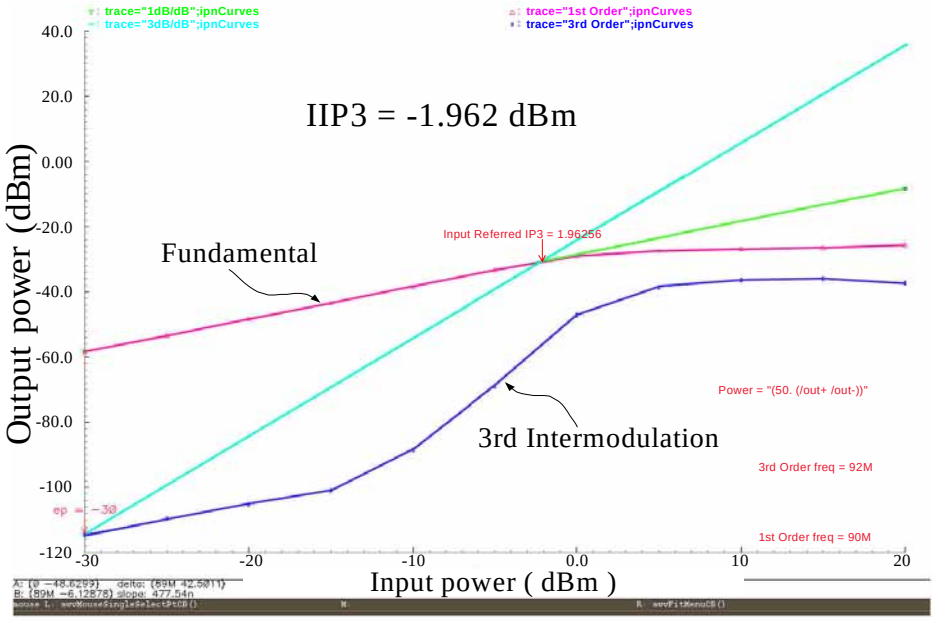

Figure 14. IIP3 plot.

Fig. 15 shows the die photo of the proposed design. The measurement is performed by Agilent 54831B oscilloscope and Agilent 33250A function generator.

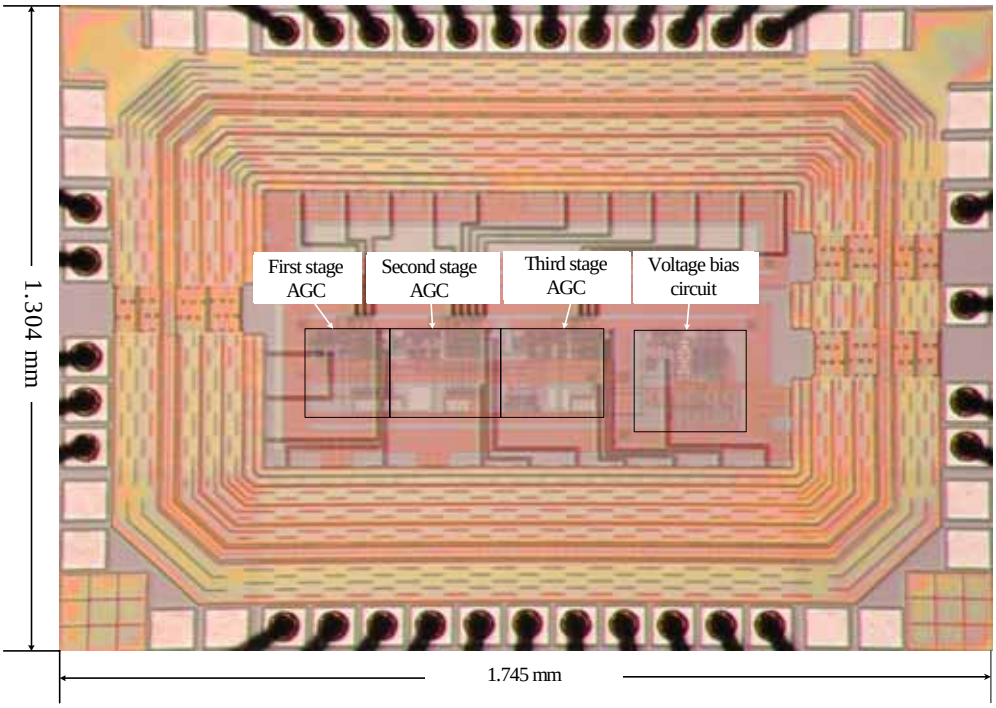

Figure 15. Die photo of the proposed designt.

The measured dynamic range is [-30, 40] dB with gain step of 2 dB. The measurement results of the proposed design are summarized in Table I. Fig. 16 shows the partial plot of the measured gain versus the required gain. Fig. 17 shows the measured gain error, where the maximum is 0.9 dB. However, if the gain offset where is 0.35 dB is taken into consideration to be calibrated, the maximum gain error is reduced to 0.55 dB. The measured power dissipation is 31 mW. The comparison of the proposed design with several prior designs is summarized in Table II. Notably, although Sanz *et al.* [12] claimed that their VGA possesses gain error less than 0.3 dB, the gain error in their work had a has 3 dB between maximum and minimum gain setting. It is obvious that the proposed design provides the widest gain tuning range with small area and no gain transition overshoot.

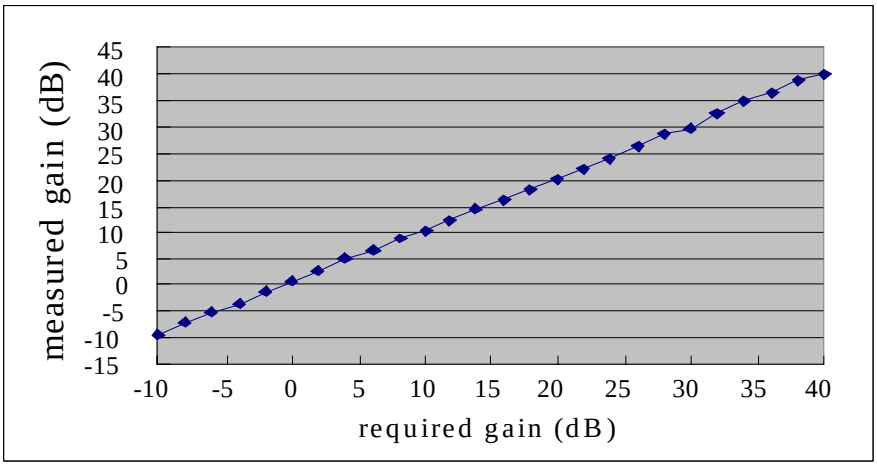

Figure 16. Partial plot of the measured gain vs. the required gaint.

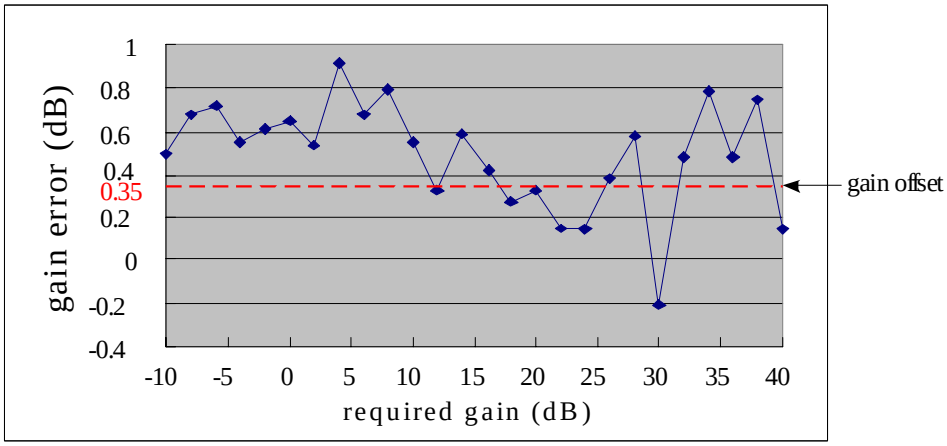

Figure 17. Gain error of the proposed design.

Dynamic range	70 dB
Gain step	2 dB
Gain error	< 0.55dB dB
standby power	31 mW
Core area	0.913 X 0.385 mm^2
Die area	1.745 X 1.304 mm^2

Table 1. Measurement results of the proposed design.

	[3]	[4]	[1]	[12]	ours
CMOS process (μm)	1.2	2	0.35	0.35	0.35
Dynamic range (dB)	2.5	30	16	36	70
Gain control interval (dB)	[-12.5, 12.5]	[-7, 23]	[0, 16]	[-8, 28]	[-30, 40]
Gain error (dB)	0.5	0.4	N/A	0.3	0.55
Area (mm^2)	0.44	1.86	0.0024	0.03	0.3
Standby power (mW)	2.3	N/A	2.1	8	31
Resolution (bits)	6	6	4	3	6
Bandwidth (MHz)	4.1	4.1	100	52	99

Table 2. Comparison with the prior design.

4. Conclusion

We have proposed a novel digital AGC based on a DVGA composed of a plurality of GBs and a fully differential degeneration amplifier. The gain tuning required by DVB-T/H receivers can be carried out by digital signals selecting proper GBs. The measurement results justify the advantages of the proposed design in terms of small area, small overshoot without any loss of bandwidth, gain step and gain error. Besides, the decibel linearity is also verified.

5. Acknowledgement

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