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Power-Aware Design of An 8-Bit Pipelining ANT-Based CLA Using Data Transition Detection

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Abstract. A high speed and low-power 8-bit carry-lookahead adder (CLA) using two-phase all-N-transistor (ANT) blocks which are arranged in a PLA design style with power-aware pipelining is presented. The pull-up charging and pull-down discharging of the transistor arrays of the PLA are accelerated by inserting two feedback MOS transistors between the evaluation NMOS blocks and the outputs. The analysis of the area (transistor count) tradeoff is also provided in this work. The output of the addition of two 8-bit binary numbers is done in two cycles. The proposed power-aware pipelining design methodology using a simple data transition detection circuit takes advantage of shutting down the processing stages with identical inputs in two consecutive cycles. The data transition detection circuit is used to monitor the state switching of input data. Not only is it proved to be also suitable for long adders, the power consumption is drastically reduced by at most 50% at every process corner.

Keywords: power-aware, ANT, data transition detection, CLA, pipeline

1. Introduction

Fast adders are key elements in digital circuits, including multipliers [1], and DSP chips [2]. Many efforts have been focused on the improvement of adder designs [5, 7–9]. CMOS dynamic logic has been recognized as one of the promising options to challenge the GHz operations or even higher for the adder design, [3–4]. Other logics suffer from a variety of different difficulties which were addressed in [7]. However, the major penalty of these prior GHz logic circuits is the high power consumption which is not a tolerable price to pay in recent mobile technologies. These circuits also unavoidably consume large power even if they are in a stand-by condition. We, hence, propose a power-aware PLA-like structure to improve our high-speed all-N-transistor (ANT) function block [7, 9, 10]. An 8-bit CLA using ANTs which are arranged in the power-aware PLA-like structure and asynchronously triggered is implemented to verify the power reduction as well as the preservation of high speed. A simple but effective data transition detection (DTD) circuit is proposed to resolve the power consumption problem. The major advantage of the power-aware design methodology is that it is robust regardless of long data words, e.g., 64-bit binary data.

A physical 8-bit ANT-based CLA using the proposed power-aware DTD is fabricated on silicon. Physical measurements verify that the reduction of the power dissipation is far less than that of prior works.

2. Power-Aware High-Speed 8-bit CLA

Although the N-block dynamic logic intrinsically possesses high speed [4], it is not good enough for

the operation in the gigahertz range. The reasons are: firstly, the slopes of the clock's edges must be gentle, and secondly, the number of stacks in the evaluation N-block severely affects the size of all of the transistors in the unit.

2.1. All-N-Transistor (ANT) Function Unit

Hence, a modified dynamic logic, ANT [10], has been proposed as shown in Fig. 1. The feature of this modification is the feedback transistor pair, P3 and N3, between the evaluation block and the output.

1). When $clk = 0$, P1 is on and the gate of P2 is precharged to be V_{dd}. Then, P2 is off and N4 is off. This makes the output to stay at the previous state.
2). When $clk = 1$ and the N-block is evaluated to be "pass", the charge at node A should be ground through the N-block and N1 theoretically. Note that N4 is on and N2 is also on at the beginning. If the previous state of output is high, then N3 will be turned on via N4. This means that N3 provides another fast discharging path for the charge at node A. When the voltage at node A is dropped below the threshold voltage of PMOS, P2 and P3 start to be on. The output will then be charged to V_{dd} via paths P2 and P3-N4.
3). When $clk = 1$ and the previous state of the output is low and the N-block is evaluated to be "pass," the voltage at node A starts to drop. When $V_A - V_{dd} > V_{tp}$, where V_{tp} is the threshold voltage of P3, P3 will be turned on such that the gate of N3 will be charged to be V_{dd}. Not only the charge at node A will be discharged faster, but also the output will be charged to high via P2 and N4.
4). When $clk = 1$ and the N-block is evaluated to be "stop", the charge at node A should be kept if the previous state of output is low. There will be no discharging path for node A because N3 will be off via N4. If the previous state is high, the output will be ground via N4 and N2 before the voltage at node A starts to drop.

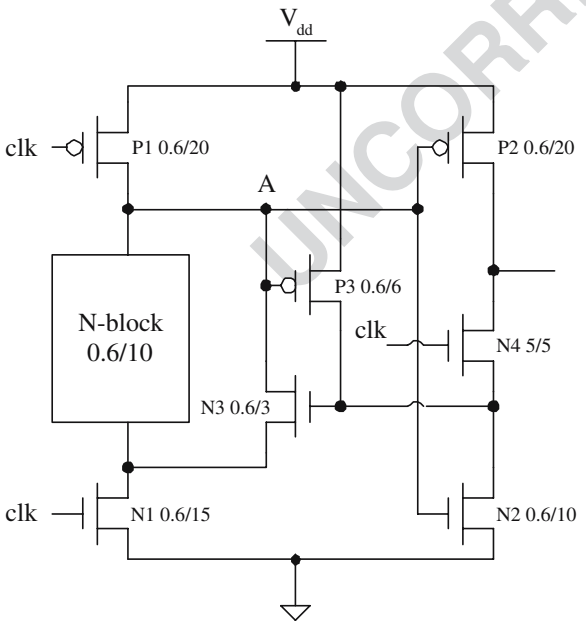

Figure 1. ANT logic.

Summarized from 2 and 3 in the above, the output will be high when the N-block is evaluated "pass", i.e., "1", during $clk = 1$. By 4, the output will be low when the N-block is evaluated "stop", i.e., "0", during $clk = 1$. The function of ANT logic block, thus, is conclusively correct and non-inverting. Restated, P3 and N3, respectively, provide an extra charging path and an extra discharging path such that the speed of the evaluation can be accelerated.

In addition to the previous discharging path problem, one of the reasons why other high-speed logic cannot run correctly given clocks with short rise time or fall time is that the size of each transistor cannot be tuned properly. Both [3] and [4] intrinsically possess this shortcoming. The sizing problem of the transistors in the ANT besides those in the N-block drastically affect the speed. We have been proceeded several simulations to find out the best figure of merit for the sizing of each transistor in Fig. 1 using TSMC 0.25 μm 1P5M CMOS technology.

2.2. PLA-Styled 8-Bit CLA Design

The formulation of a 8-bit CLA is represented by the following equations:

$$\begin{aligned} S_i &= C_{i-1} \oplus P_i \\ C_i &= G_{i-1} + P_{i-1}G_{i-2} + P_{i-1}P_{i-2}G_{i-3} \\ &\quad + \ldots + P_{i-1}P_{i-2}\ldots P_1P_0C_0 \end{aligned} \quad (1)$$

where $A_i, B_i, i = 0...7$, are inputs, and P_i, G_i are *propagate* and *generate* signals, respectively, $P_i = A_i \bigoplus B_i$, $G_i = A_i \cdot B_i$.

If the P_is and G_is are produced by combinatorial logic function blocks before they are fed into the

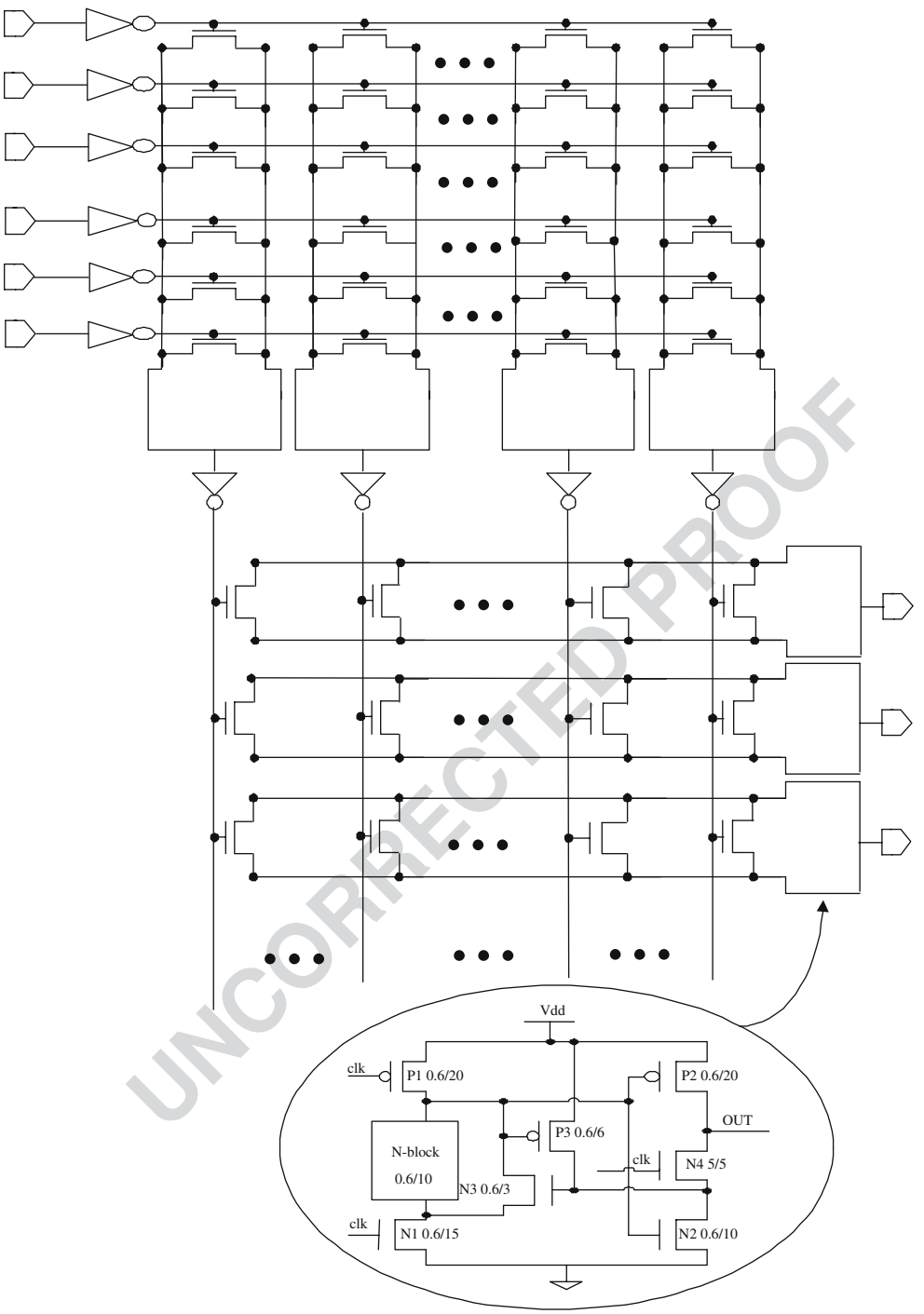

Figure 2. PLA-styled CLA.

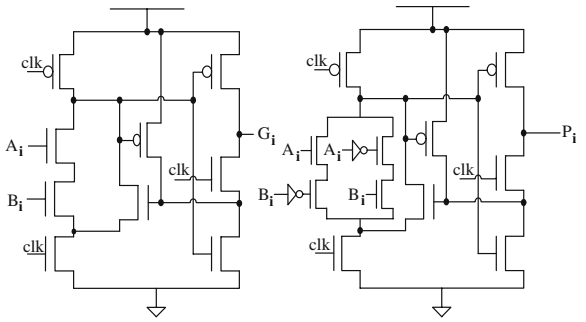

Figure 3. GP block.

function blocks for S_is and C_is, then Eq. (1) implies that a two-level AND-OR logic function block is a possible solution to achieve high speed operations. Thus, the PLA-styled design is suitable for such a function block. A conceptual PLA-styled design for CLA is shown in Fig. 2. A typical PLA consists of an AND array and an OR array. It is well known that the series NMOS in the evaluation block of NAND or AND gates will produce long discharging delays which subsequently slow down the entire circuit. We can take advantage of the non-inverting feature of the ANT logic to utilize a NOT-OR-NOT-OR configuration instead of the typical AND-OR style, where the two OR planes are made of ANT logic blocks. Meanwhile, it can also minimize the series transistor count in the evaluation block. The OR array is made of the ANT logic with a predefined

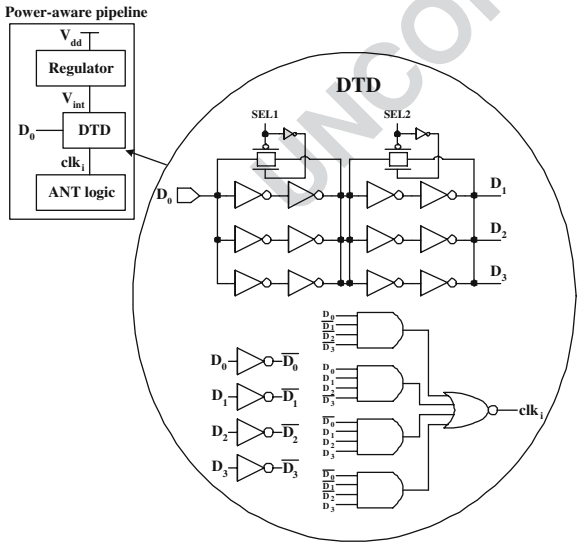

Figure 4. Power-aware circuitry.

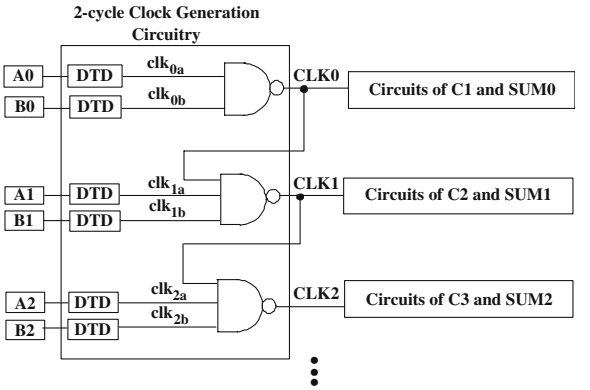

Figure 5. Block diagram of the proposed CLA.

evaluation block. The inputs to the first OR array is the inverted P_i s (propagate) and G_i s (generate) signals which are also produced by other ANT logic units as shown in Fig. 3. Note that we define the propagate signals in a different way from the traditional $P_i = A_i + B_i$ because the $P_i = A_i \bigoplus B_i$ can be reused to generate the sum term, i.e., S_i.

2.3. *Speed and Area Analysis*

Speed The critical path of an adder resides on the generation of carry signals, i.e., C_8 in the 8-bit adder. After the binary data are ready, the generation of P_is and G_is by using the ANT logic takes the high half of a full cycle. That is, the results of GP blocks will be ready when the *clk* is low. The inverted P_is and G_is will then be fed into the first OR plane of the ANT-

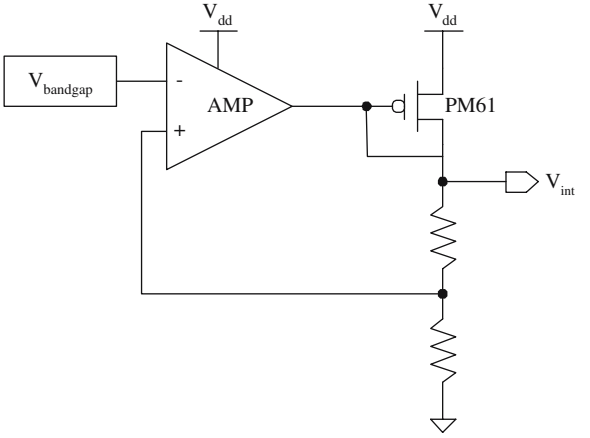

Figure 6. Regulator in the power-aware circuitry.

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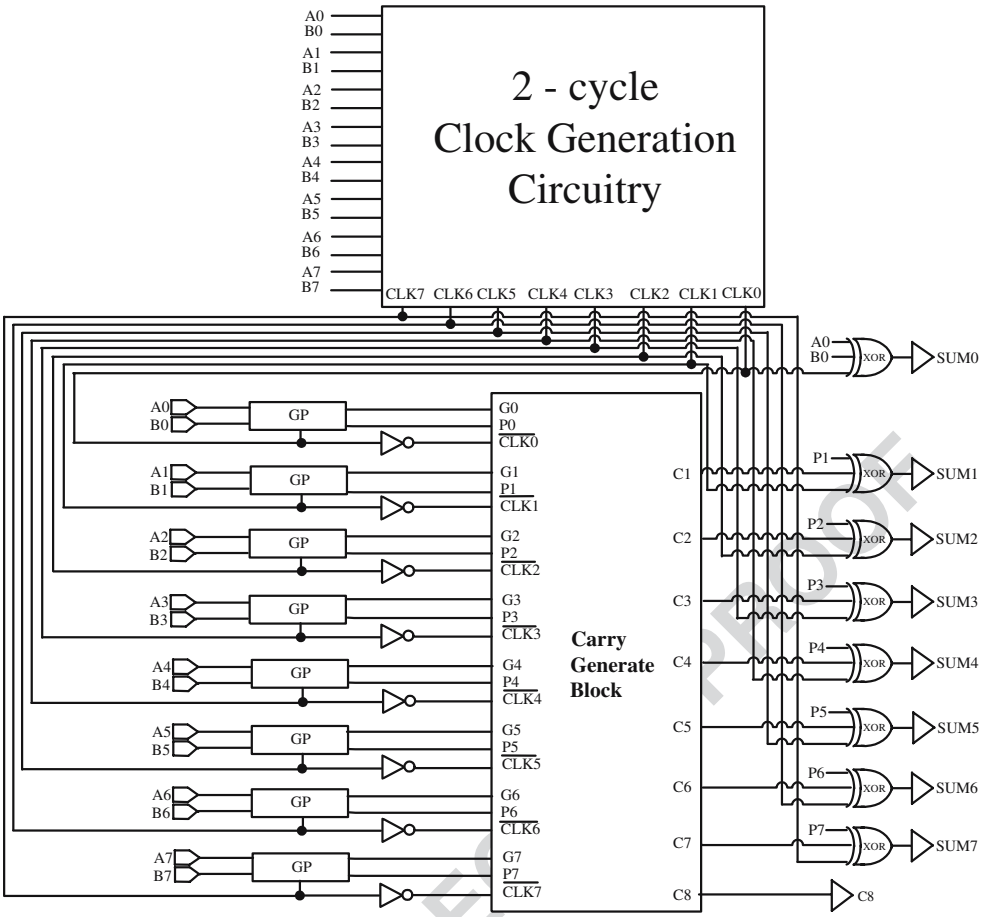

Figure 7. Schematic of the proposed CLA.

based PLA. The inverted outputs of the first OR plane will be presented to the second OR at the high half of the second cycle. The final C_is results then are ready in the low half of the second cycle. Right after the generation of every C_is, they are inverted and fed into the S_is function blocks. Another half cycle then is required to produce all of the S_is. The final result will be latched after two cycles.

Area As for the transistor count of the PLA-styled implementation for CLA using ANT logic, though an analytic form has been derived in [10], the buffers required for the system clock tree and the propagation of intermediate signals was ignored. The analysis of the cost of the buffers is as follows.

Clock Tree and Buffers To avoid any degradation resulted from signal propagation, buffers are re-

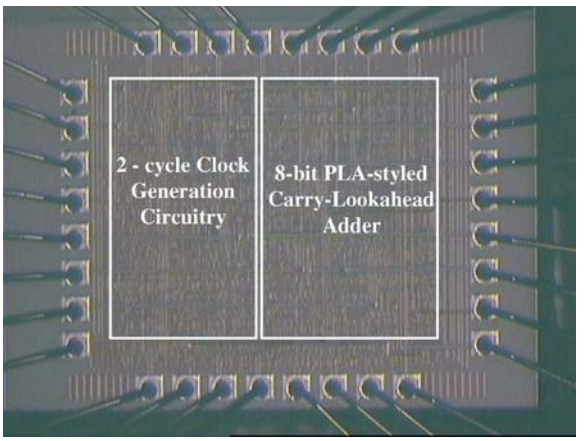

Figure 8. Die photo of the proposed CLA.

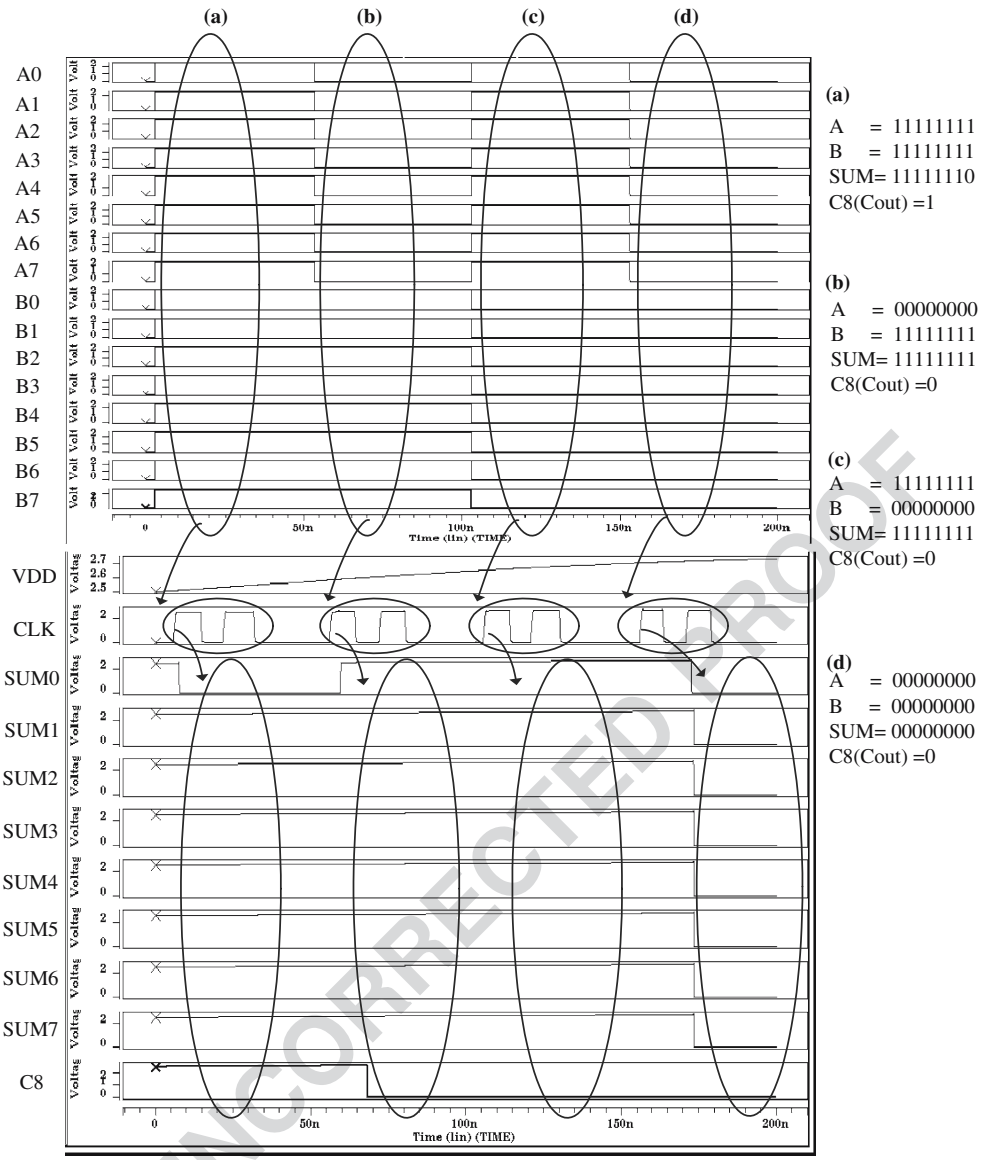

Figure 9. Post-layout simulation result.

quired at the output of each C_{i+1}, S_i, G_i, and P_i, $\forall i = 1, \ldots, n$, and the clock tree for the system clock. The total is $B_t = 12 \times 5n$, since there are a total of 12 transistors in a single buffer.

In summary, the number of the total transistors required to implement an n-bit CLA with PLA-styled design using ANT logic is

$$T_{ANT\ total}(n) = \frac{1}{6}(n+1)(n+2)(n+3) + 5n(n+1) + 50n + 3 + 60n \quad (2)$$

2.4. *Data Transition Detection (DTD)*

A simple thought to improve the power efficiency is to "deny" the current fed into those function units of which the input data are identical between two consecutive operation cycles. The dynamic power, hence, of CMOS logic elements will be drastically reduced. Take the ANT block shown in Fig. 1 as an example. Assume the N-block is composed of two cascaded NMOS transistors to constitute an AND gate. The probability of the data inputs of two

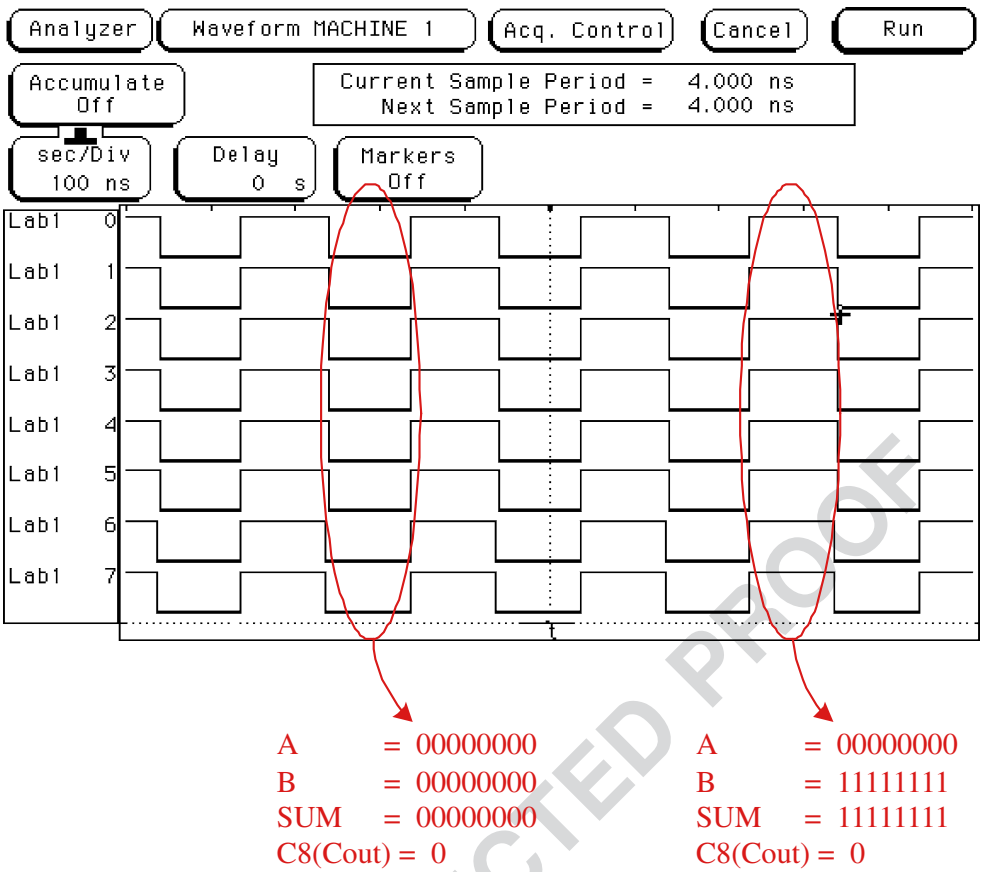

Figure 10. Waveforms of physical measurement by Agilent 1660C.

consecutive operation cycles is 25% which implies a significant portion of power consumption. Hence, a monitoring circuitry, called data transition detector (DTD), as shown in Fig. 4 is proposed to resolve the low power demand.

The DTD design is based on an important observation, which is that the state switching of either A_i or B_i will cause a series of state switches with regard to P_j, G_j, and C_j, $\forall j \geq i$. Hence, an early state transition detection of lower bits can be used to determine whether the computation of higher bits is required or not. It carries out the monitoring mechanism and triggers the addition operations asynchronously depending on the comparison of the previous operands and the current operands. The DTD is composed of three blocks: three stages of delay

Table 1. Characteristics of the proposed power-aware 8-bit adder.

	Proposed CLA
Highest data rate	500 MHz
Area	1.360×1.180 mm^2
Transistor count	3,988

Table 2. Power reduction by using the power-aware DTD circuitry (given random input vectors, system clock=200 MHz).

Data rate (MHz)	[10] (mW)	Ours simulated (μW)	Ours measured (μW)
50	35	17.4	23.0
20	35	9.7	10.5
10	35	4.9	7.7

chains to generate phase-shifted data pulses, a two-cycle generation circuitry, and a voltage regulator.

As shown in Fig. 4, the D_0 is propagated through three delay stages which individually comprises four cascaded inverters to generate D_1, D_2, and D_3. The delay stages can be controlled by the control signals, *SEL1* and *SEL2*, to adjust the delay time of the delay chains. D_i, $i = 0, \ldots, 3$, are inverted respectively to generate $\overline{D_i}$, $i = 0, \ldots, 3$. Since what the 8-bit PLA-styled CLA needs to complete an addition operation is 2 cycles, we conclude that $(D_3D_2D_1D_0)$ = 0001, 0111, 1110, 1000, are the states required to generate two consecutive clock cycles for the required addition. Hence, the individual two-cycle generation circuitry for each ANT logic, e.g., *CLK0* for C1 and SUM0, is carried out as shown in Fig. 5.

However, the most critical part of the proposed DTD is the sensitivity of the strobe duration with respect to the power variation. One of the most efficient approach to avoid the unstable power supply is to employ step-down bandgap-referenced voltage regulators to supply a temperature independent reference voltage to the rest of the circuitry [6]. Referring to Fig. 6, the regulator is composed of AMP, PM61, and a resistor string. The generated internal voltage for the DTD is a very stable $V_{int} = V_{dd} - V_{thp}$, where V_{thp} is the threshold voltage of PM61.

Area Overhead A single DTD is composed of a three-stage buffer (12 transistors), four four-input AND gates (32 transistors), four inverters (eight transistors), six transmission gates (24 transistors), and an NOR gate (eight transistors). In brief, there are a total of 84 transistors in a single DTD. For an n-bit adder, we need $2n \times 84$ to carry out the DTDs. Besides, in a two-cycle clock generation circuitry, a total of n NAND gates and $(n-1)$ OR gates are required for the n-bit adder. $4n + 6(n-1)$ MOSs, thus, must be taken into account. Hence, the area overhead caused by the proposed power-aware design is concluded as follows.

$$T_{DTD}(n) = 168n + 10n - 6kc05 \qquad (3)$$

Notably, the cost ratio of the DTD is defined as $CR(n) = \frac{T_{DTD}(n)}{T_{ANT\ total}(n)}$. Hence,

$$\lim_{n-\infty} CR(n) = \lim_{n-\infty} \frac{T_{DTD}(n)}{T_{ANT\ total}(n)} = 0, \qquad (4)$$

According to Eqs. (2) and (3), it implies that the proposed power-aware design is particularly suitable for long adders.

3. Simulations and Measurement

The block diagram of the proposed 8-bit power-aware PLA-styled ANT-based CLA has been shown in Fig. 5. By contrast, the detailed schematic and diephoto of the CLA implemented by TSMC 0.25 μm 1P5M CMOS process are revealed in Figs. 7 and 8, respectively. An example of the output waveform of 8-bit power-aware PLA-styled CLA using ANT logic is shown in Fig. 9 which illustrates that the result of an addition appears after two cycles given that the V_{dd} is coupled with a 1 MHz sine wave noise possessing 10% V_{dd} amplitude. Fig. 10 shows the output waveforms of the addition of "00000000" and "00000000 ", and the addition of "00000000 " and "11111111 ", respectively. The measurement is carried out by using Agilent 1660CP logic analyzer. The characteristics of the proposed power-aware CLA is summarized in Table 1.

To reveal the power-saving advantage of the proposed power-aware design, two 8-bit adders are, respectively, implemented by the approach of [10] and the proposed design using the same CMOS process. The power reduction of the power-aware design is summarized in Table 2, where random test vectors are used to test these circuits.

4. Conclusion

We propose a power-aware high speed PLA-styled ANT logic design for the adders' implementation. A novel but simple DTD circuit is used to monitor the switching activity of input data such that the unnecessary power consumption is avoided. Not only the correctness of the function given a fast clock is preserved, but also the power dissipation is reduced.

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