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Microelectronics Journal 38 (2007) 716–721

Microelectronics Journal

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An 80 MHz PLL with 72.7 ps peak-to-peak jitter

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Received 20 July 2006; received in revised form 10 April 2007; accepted 10 April 2007
Available online 7 June 2007

Abstract

This paper presents a design of a 72.7 ps peak-to-peak (p2p) jitter, 80 MHz, phase-locked loop (PLL) circuit for digital video broadcasting over terrestrial (DVB-T) receivers. A step-down voltage regulator is utilized to suppress the coupled supply noise. A zero offset charge pump is employed to eliminate the static phase offset caused by the charge offset when the PLL is in lock. The measurement results on silicon using the TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process show that the proposed PLL achieves as low as 72.7 ps p2p jitter on silicon when the output frequency is 80 MHz and the power consumption is merely 10.5 mW given a 3.3 V power supply.

Keywords: Phase-locked loops; Jitter; Supply noise; Regulator

1. Introduction

The standard for digital terrestrial television (DTTV) broadcasting was finalized by the digital video broadcasting (DVB) consortium in 1997, which has been known as digital video broadcasting over terrestrial (DVB-T) in many countries [1]. The DVB-T utilizes the coded orthogonal frequency division multiplexing (COFDM) modulation, which is that the television signals (usually in MPEG-2 format) are encoded for the error correction and modulated by the orthogonal frequency division multiplexing (OFDM) scheme. The OFDM scheme can alleviate the problem of multi-path fading effect and have the advantage of good spectral efficiency. A DVB-T receiver should be capable of transforming the radio-frequency (RF) signal into an MPEG transport stream. That is, the RF signal is down-converted into a baseband signal through an analog-to-digital conversion. The frequency of the baseband signal was suggested to be sampled at 18.28 MHz and quantized by a 10-bit analog-to-digital converter (ADC) in the prior work [2]. However, the performance would be much better if the sampling rate of the ADC is raised. The reason is that the sampling error can be reduced. We, thus, select 80 MHz as the ADC sampling rate, since it is around four times of the prior 18.28 MHz sampling rate. Therefore, a phase-locked loop (PLL) is required to generate such an 80 MHz clock with a low jitter, since the jitter of the clock will result in a serious sampling uncertainty. The jitter at the output of the PLL might be caused by a variety of sources. It was shown that the contribution of device noise and thermal noise to the jitter is typically much less than that caused by the supply noise and substrate noise [3]. In this work, we employ several techniques to reduce the supply noise and other non-ideal effects in the PLL.

2. Low-jitter PLL architecture

Fig. 1 is the block diagram of the proposed PLL. The supply noise is the major noise source which will impose irregular fluctuations upon the voltage-controlled oscillator (VCO) and the charge pump. The step-down voltage regulator is then utilized to provide a stable supply voltage

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doi:10.1016/j.mejo.2007.04.016

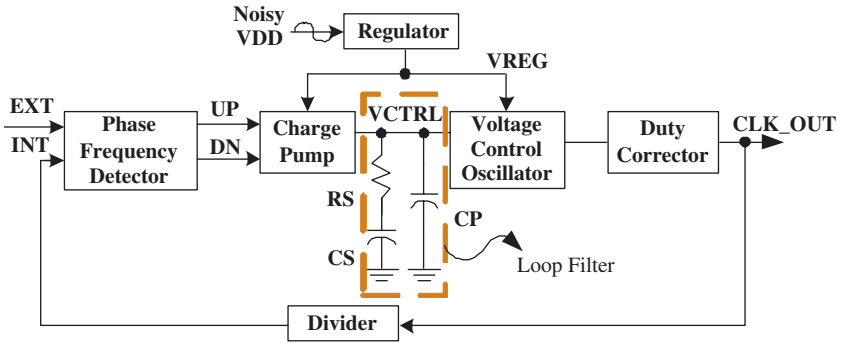

Fig. 1. Block diagram of the proposed PLL.

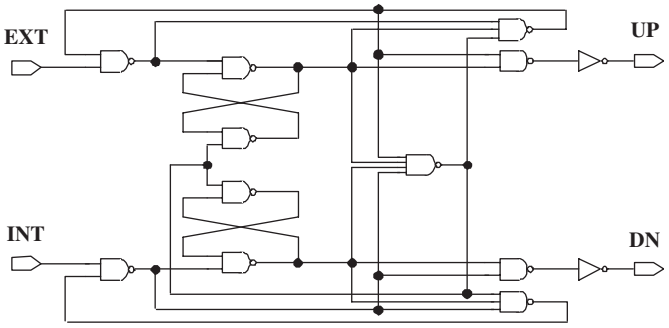

Fig. 2. Bang-bang-type PFD.

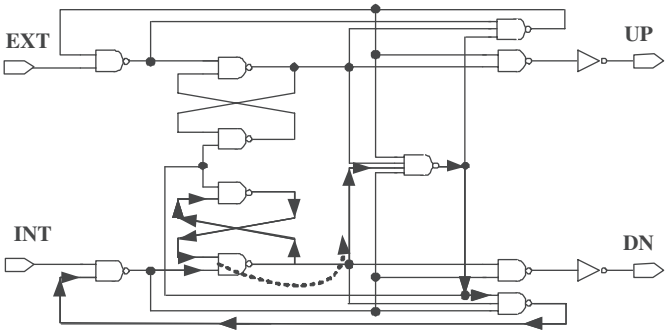

Fig. 3. Critical delay path of the bang-bang-type PFD.

for the VCO and the charge pump to reduce the supply noise. Besides, there are several non-ideal effects that would lead to a large phase noise of the PLL. For instance, the dead zone in the charge pump circuit will result in the accumulation of the random phase error in the VCO. The charge offsets in the charge pump will cause the phase offsets. Referring to Fig. 1, the phase-frequency detector (PFD) should assert the output signals, DN and UP, simultaneously for an equal duration to eliminate the dead zone. Besides, the net charge in the loop filter should not be drifting when the PLL is in lock. Otherwise, these charge offsets will introduce jitter even when the PLL is in lock. We utilize the zero offset charge pump [4] to prevent any net charge transferring from or to the loop filter. The VCO [5] without tail currents is employed to avoid the noise introduced by the mismatch of current mirrors. Meanwhile, we reduce the gain of the VCO to keep the phase noise from being over-amplified.

2.1. Phase-frequency detector (PFD)

The PFD compares the difference of phase and frequency between the external reference clock signal EXT and the feedback clock INT. Fig. 2 is the PFD circuit which is the bang-bang-type PFD [6]. The speed of the PFD is limited by their critical delay path. Fig. 3 shows the critical delay path, which is the path to reset all of the internal nodes in the circuit. The function of reset is to assert output signals, UP and DN, for an equal duration. This duration is required to allow UP and DN signals reaching their logical levels to either turn on or turn off the current source/sink of the charge pump, respectively. Consequently, the PLL is still capable of adjusting phase and frequency even when the phase difference of EXT and INT equals to zero. Furthermore, if the charging current and discharging current are identical in such a scenario, the PLL can be locked in the zero phase offset state [6]. Fig. 4 is the simulation result when the PLL is in lock.

2.2. Zero offset charge pump

Noise and the mismatch between the charging current and the discharging current in the charge pump invoke the phase error. Supply noise occupies a significant portion of noise, which will reduce the charge-pump gain. A step-down regulator is used to suppress the supply noise and provide a stable voltage for the charge pump as well as the supply voltage. Fig. 5 is the schematic of the charge pump, which is the zero offset charge pump [4]. Referring to Fig. 5, two NMOS source coupled pairs are connected by the current mirrors composed of the symmetric load buffers. As mentioned before, the PFD asserts the signals UP and DN as two identical pulses once in every clock cycle when the PLL is locked. When both the UP and DN are asserted, the symmetric loads, PM01,

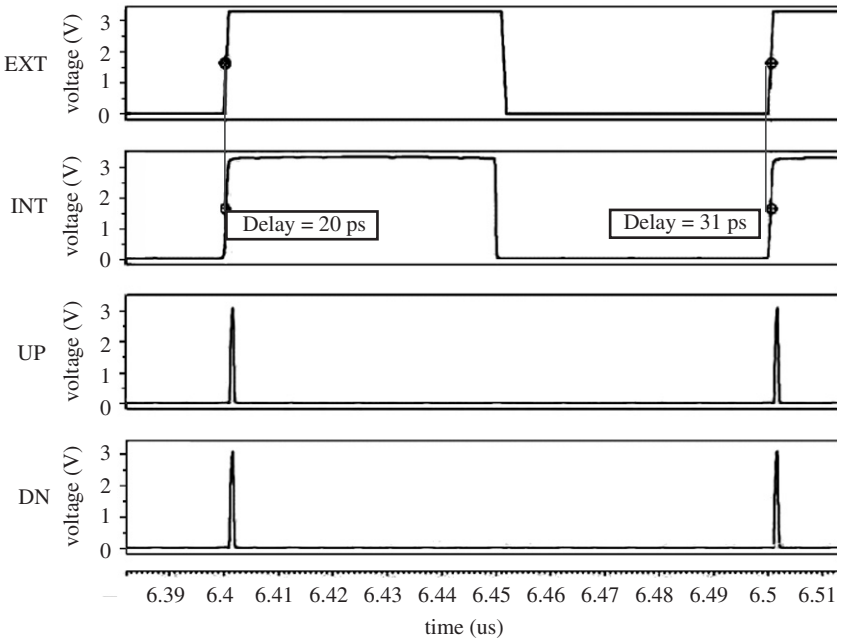

Fig. 4. The simulation waveforms when the PLL is locked.

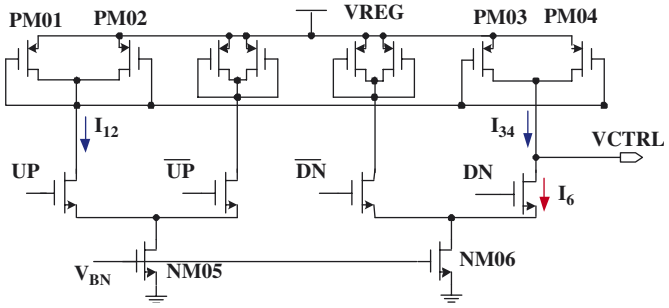

Fig. 5. Schematic of the charge pump.

PM02, PM03, and PM04, operate as a current mirror ($I_{34} = I_{12}$), and the right source coupled pair will sink the same current as that flowing through PM03 and PM04 ($I_6 = I_{34}$). Since the current flowing into the loop filter is identical to that flowing out of the loop filter, these currents are canceled out to make the net charge in the loop filter be a constant. Hence, the zero static phase offset is ensured. Fig. 6 shows the variation of VCTRL when the PLL is locked, where VCTRL is the output signal of the charge pump. The maximum variation in Fig. 6 is less than 10 mV at all PVT (process, supply voltage, temperature) corners.

2.3. Voltage-controlled oscillator

Fig. 7 shows the schematic of the VCO, which is a three-stage no-tail-current VCO [5]. Take a single stage as an example. The differential delay cell consists of the transistors NM11, NM12, and p-type cross-coupled pair formed by PM11 and PM12. NM13 and NM14 control the oscillation frequency of the VCO. The regulator provides the stable supply voltage to the VCO. The no-tail-current VCO is utilized to avoid the mismatch of current mirrors. Moreover, we reduce the gain of the VCO to suppress the jitter of the PLL. Although the reduction of the gain of the VCO decreases the tuning range, it poses no crucial influence on the desired DVB-T receiver applications. Fig. 8 shows the gain of the VCO.

2.4. Regulator

The supply noise can be drastically isolated from the charge pump and the VCO by the regulator. Fig. 9 is the schematic of our regulator. The bandgap circuit generates a stable reference voltage VBGAP which is insensitive to the variation of the temperature and the power supply. This reference voltage VBGAP is fed to the feedback network, which is composed of the operational amplifier OPA and resistors, to generate the desired voltage, VREG.

3. Implementation and measurement

The overall design is implemented by TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process. The die photo of the proposed design is shown as Fig. 10. Fig. 11 shows the worst-case pick-to-pick jitter (p2p jitter) derived from the post-layout simulation, which is 60 ps with the presence of the

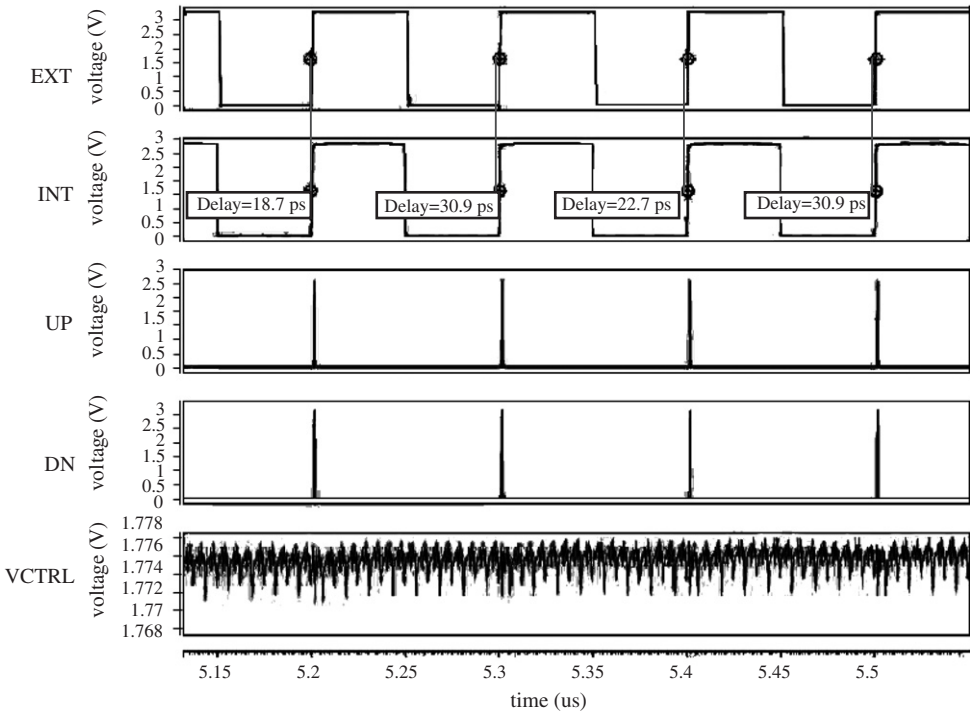

Fig. 6. The simulation waveforms when the PLL is locked.

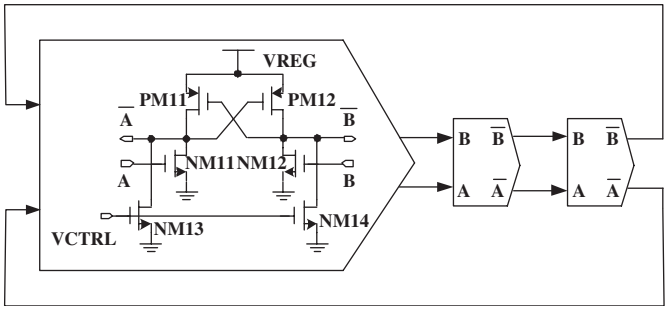

Fig. 7. Schematic of the no-tail-current VCO.

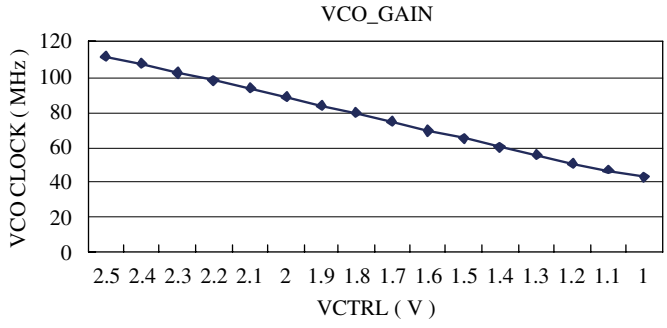

Fig. 8. The gain of the VCO.

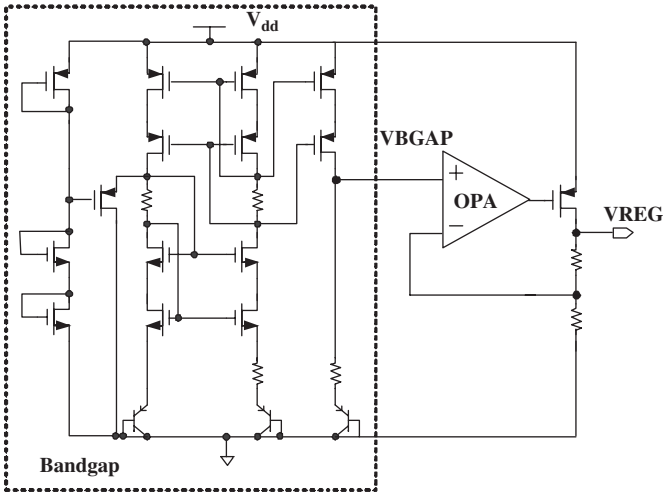

Fig. 9. Schematic of the regulator.

power supply noise. In order to simulate the power supply noise, we impose small 100 KHz, 1 MHz, 10 MHz, and 80 MHz signal sources upon the power supply during the simulations. Each of these sources possesses the amplitude of 10 mV.

Fig. 12 shows the measured p2p jitter and cycle jitter on silicon, which are 72.7 and 17.04 ps, respectively. The measured duty cycle of the generated sine wave is 51.9%. The measurement of the proposed design is performed by Agilent 54831B (oscilloscope), GW GPC-3030D (power supply), and Agilent 33250A (function generator). The overall results of physical measurements on silicon are summarized in Table 1.

The comparison between our design and several prior works is summarized in Table 2. Our design possesses the lowest p2p jitter with the presence of the supply noise.

4. Conclusion

A 72.7 ps p2p jitter 80 MHz PLL design is presented in this paper. The regulator is utilized to reject the power supply noise. The zero charge offset charge pump and the differential VCO contribute to the reduction of the phase errors. The physical measurement of the PLL on silicon

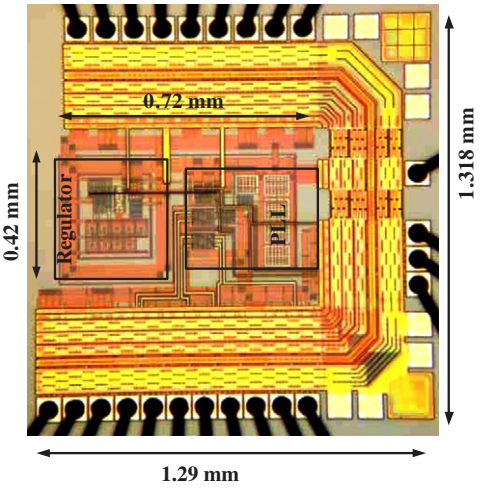

Fig. 10. Die photo of the proposed design.

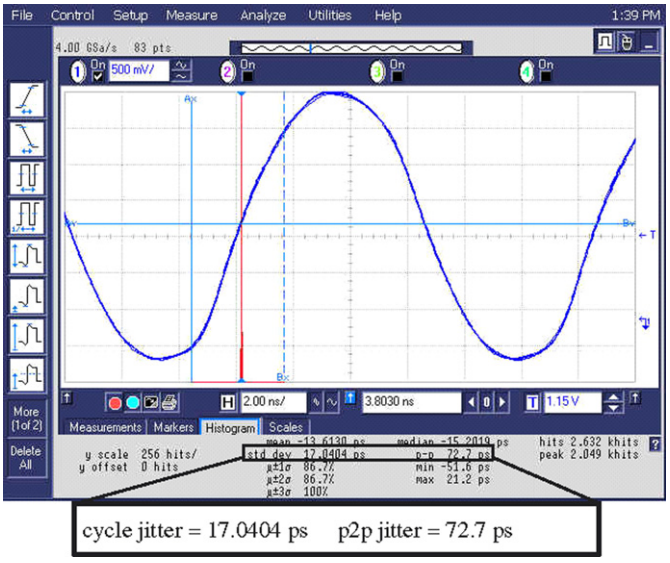

Fig. 12. The measured p2p jitter and cycle jitter of the proposed design.

Table 1
Measurement results of the proposed design

Output frequency	80 MHz
Peak-to-peak jitter	72.7 ps
Cycle jitter	17.04 ps
Power	115 mW[a]
Die size	1.29 × 1.318 mm^2

[a]The power consumption of PADs is included.

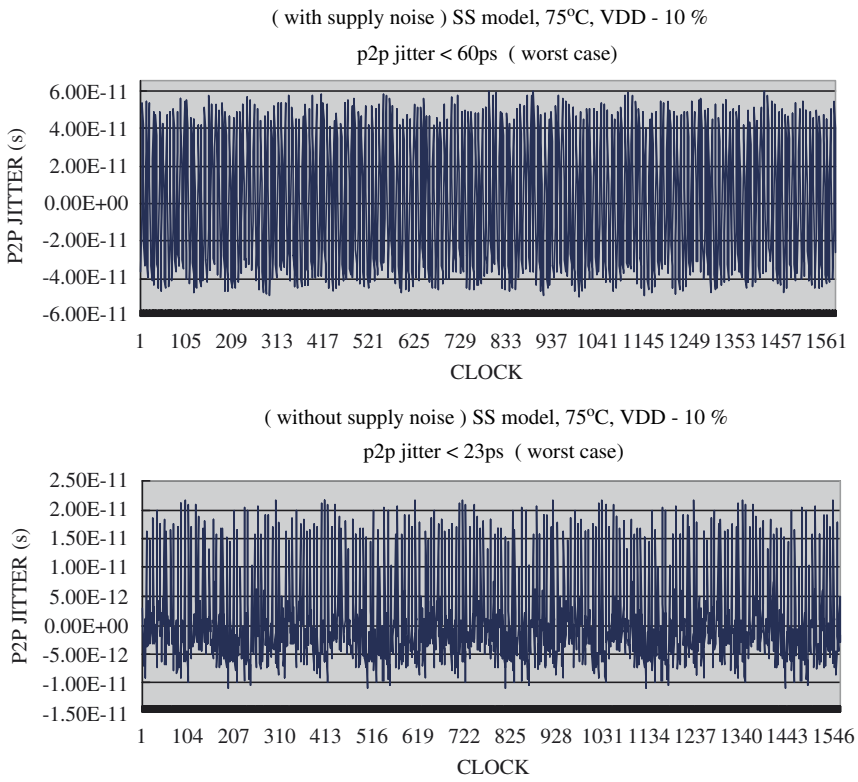

Fig. 11. Peak-to-peak jitter.

Table 2
Comparison with prior designs

	[7]	[4]	[8]	[9]	[10]	Ours
Process (μm)	0.4	0.5	0.17	0.4	0.35	0.35
Output freq. (MHz)	>667	550	250	612	250	80
p2p Jitter (ps)	<250	144	200	80	<100	72.7
Power (mW)	340@400 MHz	9.24	27	N/A	49.5	115
Consumption						
Area (mm^2)	N/A	1.91	N/A	0.665	N/A	1.7

manifests its low jitter, thus making it suitable for the receivers of the DVB-T system.

Acknowledgments

This research was partially supported by National Science Council under Grants NSC94-2213-E-110-024 and NSC94-2213-E-110-022. Furthermore, the authors would like to express their deepest gratitude to CIC (Chip Implementation Center) of NAPL (National Applied Research Laboratories), Taiwan, for their thoughtful chip fabrication service. The authors also like to thank "Aim for Top University Plan" project of NSYSU and MOE, Taiwan, for partially supporting this investigation.

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