A 4-kb Low-Power SRAM Design With Negative Word-Line Scheme

Chua-Chin Wang, *Senior Member, IEEE*, Ching-Li Lee, and Wun-Ji Lin

***Abstract*—The physical implementation of a prototypical 250-MHz CMOS 4-T SRAM is described in this paper. The proposed SRAM cell takes advantage of a negative word-line scheme to minimize the leakage current of the cell access transistors. As a result, the standby power consumption is drastically reduced. The proposed 4-kb 4-T SRAM is measured to consume 0.32 mW in the standby mode, and a 3.8-ns access time in the R/W mode. The highest operating clock rate is measured to be 263 MHz.**

***Index Terms*—Leakage current, negative word-line (NWL), power-delay product, SRAM, 4-T SRAM cell.**

I. Introduction

THE TREND toward portable and small digital equipments or systems is rapidly booming [1]. The demand of low power becomes the key of the VLSI designs rather than high speed. Particularly, embedded SRAMs and caches. The leakage current of the memory will be increased with the capacity such that more power will be consumed even in the standby mode. Many schemes have been mentioned to improve the power consumption of the SRAM. Kawaguchi *et al.* [3] showed a high-speed and low-power memory by dynamically controling n- and p-well bias voltage to $V_{\rm DD}$ and $V_{\rm SS}$, respectively, for selected memory cells. Wang *et al.* [10] indicated that the threshold voltages of the wordline-controlled nMOS transistors of memory cells can be dynamically variable to achieve high-speed and low-power operations. However, these works need to pay the price of a special process or large area overhead. Wang *et al.*, [4], [5], used dual threshold voltage transistors to constitute the memory cells. Low threshold voltage transistors are mainly used in driving bit-line to speed up the R/W operation while high-threshold voltage transistors are used in latching data to reduce leakage current [6]–[8] described a negative word-line (NWL) scheme to prevent memory cell leakage in order to reduce the threshold voltage of the cell access transistor for low-voltage DRAMs. In this paper, we propose a deterministic NWL method to minimize the operating leakage current and to reduce the idle power consumption. Besides, a current-mode sense amplifier is also employed to nullify the loss of the access speed. Last but not least, the proposed SRAM design is carried out by a typical CMOS technology (Taiwan Semiconductor Manufacturing Company 1P6M CMOS process) such that it is fully compatible with CMOS digital design. Therefore, it is easy to be integrated in system-on-chip (SOC) designs.

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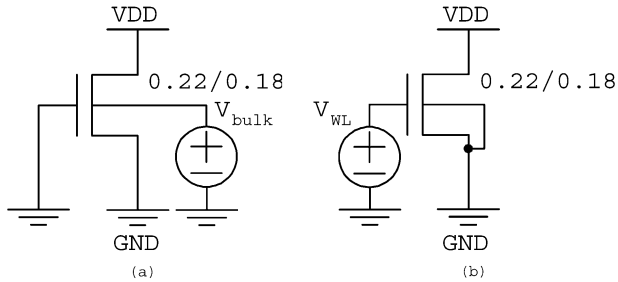


Fig. 1. Simulation circuits of the NB and the NWL schemes.

II. Low-Power 4-T SRAM Design

According to [2], a unified active power consumption of a normal read cycle for CMOS SRAMs is approximately given by

$$P = V_{\rm DD} I_{\rm DD} \tag{1}$$

$$I_{\rm DD} = m i_{\rm act} + (n+m) C_{\rm DE} V_{\rm INT} f + m(n-1) i_{\rm hld} + C_{\rm PT} V_{\rm INT} f + I_{\rm DCP} \tag{2}$$

where P is the total power dissipation, $V_{\rm DD}$ is an external supply voltage, $I_{\rm DD}$ is a current of $V_{\rm DD}$, m is the number of memory cells on an WL, n is the number of the columns of a memory cell array, $i_{\rm act}$ is an effective current of active or selected cells, $i_{\rm hld}$ is an effective data retention current of inactive or nonselected cells, $C_{\rm DE}$ is an output node capacitance of each decoder, $V_{\rm INT}$ is an internal supply voltage, $C_{\rm PT}$ is a total capacitance of CMOS logic and driving circuits in periphery, $I_{\rm DCP}$ is a total static (dc) current of periphery, and f is the operating frequency. Undoubtfully, the data-retention power occupies a great portion of the total power. It will become more significant in nanometer processes.

Besides, a loadless 4-T SRAM cell size is 35% smaller than a 6-T SRAM cell, and the power consumption of the loadless 4-T SRAM cell is 29% lower than the 6-T SRAM cell using 0.18-μm CMOS technology [13]. The stability of the loadless 4-T SRAM cell has also been proven to be no worse than 6-T SRAM cell in [13]. Hence, the loadless 4-T SRAM cell is widely used in microprocessor as embedded cache [14]. In order to save power and reduce the cell area, we select 4-T SRAM cells to construct the SRAM memory. The major goal in this design is to decrease the data retention current of inactive cells, i.e., the leakage current of the cell access transistors. There were two major control schemes to reduce the leakage current of the cell access transistors : negative bulk (NB) bias, and NWL voltage.

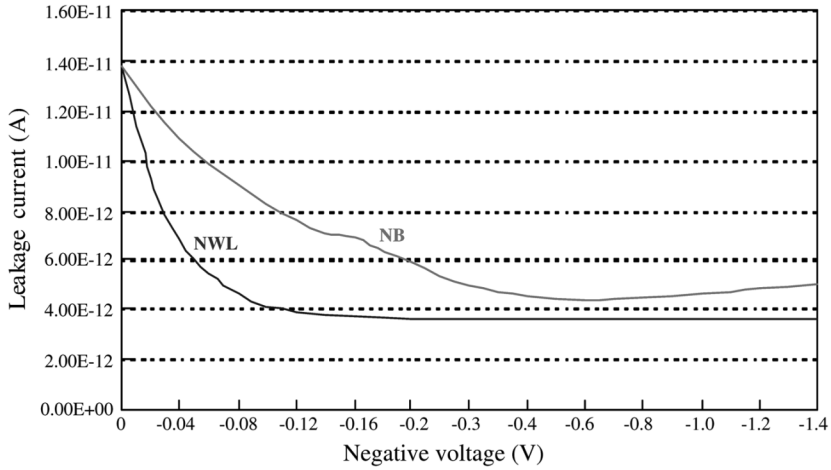


Fig. 2. Leakage current comparison of the NB and the NWL schemes (plotted by the AvanWaves software).

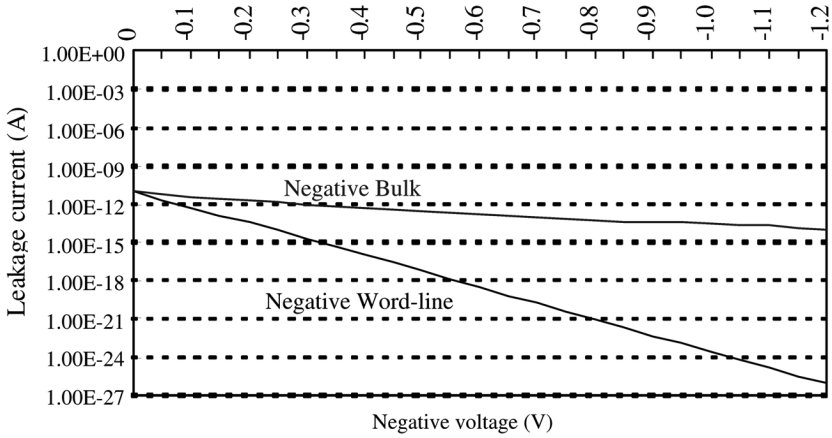


Fig. 3. Leakage current comparison of the NB and the NWL schemes (plotted by the simulated lis files).

A. Leakage Current Comparison of the NB and the NWL Schemes

According to [9], we attain the following $V_{\rm TH}$ formulation:

$$V_{\rm TH} = V_{\rm TH0} + \gamma(\sqrt{\mid 2\phi_F \mid + V_{\rm SB}} - \sqrt{\mid 2\phi_F \mid}) \qquad (3)$$

where $V_{\rm TH0}$ denotes the threshold voltage with a zero bulk bias, ϕ_F is electrostatic potential, γ is the body coefficient, and $V_{\rm SB}$ is the bulk bias. Applying a negative bias to the bulk of nMOS or a positive bias to that of pMOS, the $V_{\rm TH}$ will be increased and the leakage current, on the contrary, will be reduced. Besides, applying a negative bias to the gate of MOS field-effect transistors (MOSFETs), the leakage current also can be reduced. Fig. 1 shows the simulation circuits of the NB and the NWL schemes in order to investigate leakage currents. The leakage current simulations have different results according to the AvanWaves software or the lis file is used. The simulation results of the NB and the NWL schemes when negative voltages $V_{\rm bulk}$ and $V_{\rm WL}$ are varied from -1.4 to 0 V, given Typical, Typical (TT) model, $V_{\rm DD} = 1.8$ V, 25 °C is shown in Fig. 2, which is plotted by the AvanWaves software. It is found that the leakage current of the NWL scheme is smaller than that of the NB scheme. Moreover, in order to attain the minimum leakage current, the NB scheme needs a firmly stable bias ≈ -0.7 V, but the NWL scheme only needs keeping the bias below -0.4 V. Fig. 3 shows an alternative simulation results given different transistor bias of the simulated lis files. It is found that the leakage currents of both schemes decrease with the increase in magnitude of the reverse voltage. Besides, for the NB scheme, a triple-well structure is required to isolate the well voltage of the transistor. Hence, the area required by the design rules if the NB scheme is adopted will be increased very significantly.

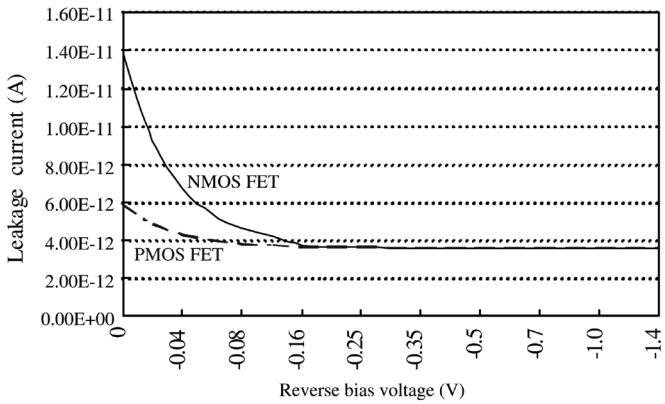


Fig. 4. NWL simulation results of nMOS and pMOS FETs (plotted by the AvanWaves software).

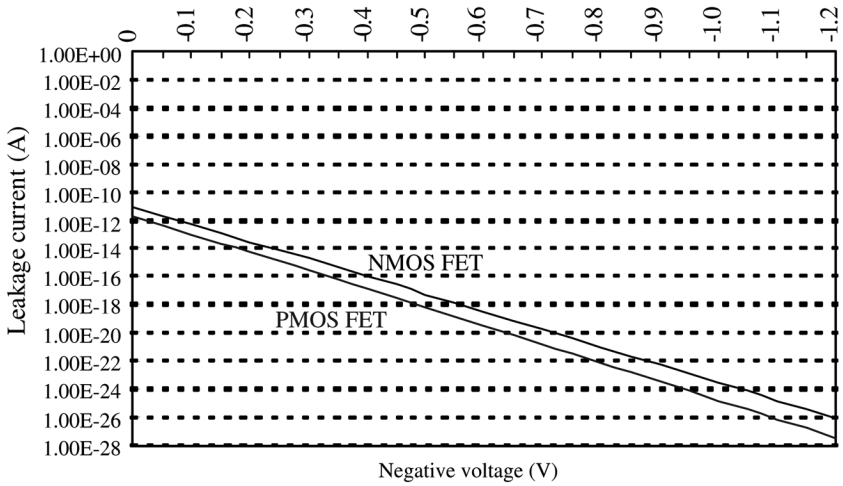


Fig. 5. NWL simulation results of nMOS and pMOS FETs. (plotted by the simulated lis files).

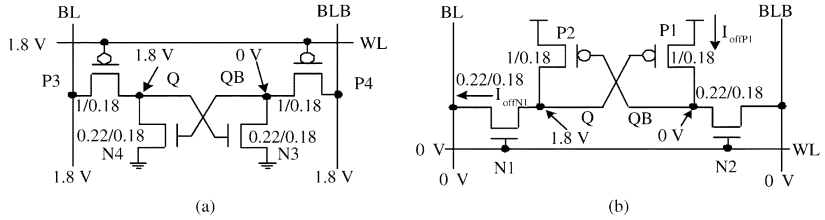


Fig. 6. Two types of the loadless CMOS 4-T SRAM cell.

B. Leakage Current Comparison of nMOS and pMOS FETs

To justify the leakage current of the pMOS FETs, the behavior of nMOS and pMOS FETs using the NWL scheme is simulated. In the simulations, the aspect ratios of the pMOS and the nMOS FETs are 1 μm/0.18 μm and 0.22 μm/0.18 μm, respectively. Moreover, we use the transistor sizes to construct the 4-T SRAM cells. The simulation results given that V_{gs} is reversed and varied from -1.4 to 0 V, given a TT model $V_{\rm ds}$ =1.8 V, 25 °C, is shown in Fig. 4, which is plotted by the AvanWaves software. Fig. 5 shows an alternative simulation results given different transistor bias of the simulated lis files. Both figures are obvious that the leakage current of nMOS FETs is higher than that of pMOS FETs given the identical reverse bias voltage.

C. Power Consumption Comparison of Two Types of Loadless CMOS 4-T SRAM Cell

Fig. 6 shows two types of the loadless CMOS 4-T SRAM cell using a supply voltage of 1.8 V. Fig. 6(a) is a n-latch p-access (NLPA) loadless CMOS 4-T SRAM cell, while Fig. 6(b) is a p-latch n-access (PLNA) loadless CMOS SRAM cell. During standby, one of the two storage nodes (Q and QB) is latched at $V_{\rm DD}$, while the other storage node is latched at 0 V. Referring to the SRAM cell in Fig. 16(b) shown later, the pre-discharged bitline (BL and BLB) voltage must be maintained at the ground (GND) level for stable data retention. The $N1$ and the $P1$ MOSFETs have the same bias condition. According to Fig. 4, the leakage current of $N1$ $(I_{{\rm off}N1})$ is larger than that of $P1$ $(I_{{\rm off}P1})$. Hence, reducing the leakage current of nMOS FET can obtain a better power-saving benefit than that of pMOS FET. We apply, respectively, a normal cutoff voltage (1.8 V for the NLPA SRAM cell, and 0 V for the PLNA SRAM cell) and a reverse bias voltage (2.5 V for the NLPA SRAM cell, and -0.7 V for the PLNA SRAM cell) to the WL transistors of both 4-T SRAM cells in Fig. 6(a) and (b) in order to compare the power-saving of both SRAM cells. Table I shows the simulation results at TT model, $V_{\rm DD}$ =1.8 V and 25 °C. According to Fig. 5, we can estimate and justify the simulation results. It reveals the PLNA SRAM cell can save more power than the NLPA SRAM cell when the NWL scheme is used, since the suppressed current of the NLPA SRAM cell is not in the critical leakage current path. Hence, we adopt the PLNA loadless 4-T SRAM cell to construct the proposed SRAM. Notably, during the standby mode for the PLNA SRAM cell, the 0 storing side voltage will rise due to the leakage current of the off pMOS load is higher than that of the off nMOS access transistor. Fig. 7 shows the voltage variation of Q (state 1) and QB (state 0) in the proposed 4-T cell regarding leakage currents. The final voltage level of QB will go into a steady state, is 1.23 V. Although the state 0 is at a higher voltage level, the read operation from a cell is not

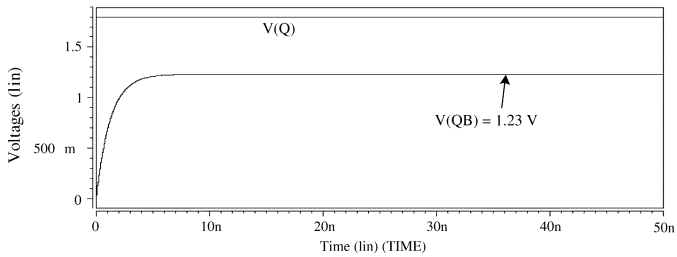


Fig. 7. Voltage variation of Q and QB regarding leakage currents.

TABLE I
COMPARISON OF POWER SAVING

	V_{gs} = 0 V	V_{WL} = 2.5 V for NLPA SRAM cell V_{WL} = -0.7 V for PLNA SRAM cell
NLPA SRAM cell power consumption	23.52 pW	23.34 pW
PLNA SRAM cell power consumption	22.25 pW	3.96 pW

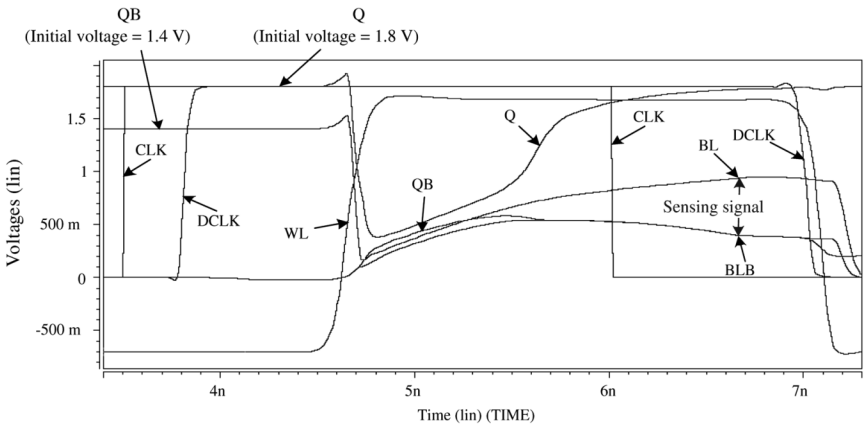


Fig. 8. Read operation given $V(\mathrm{QB}) = 1.4$ V and $V(\mathrm{Q}) = 1.8$ V.

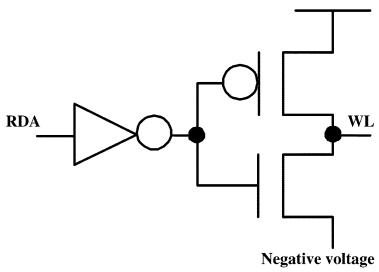


Fig. 9. WL voltage control circuit.

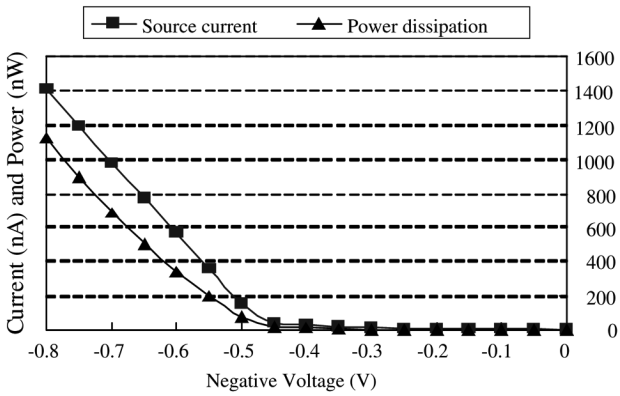


Fig. 10. Source current of the nMOS FET and power dissipation of the negative supply.

affected. Fig. 8 shows the read operation still correctly works even if the voltage level of QB is 1.4 V.

Fig. 9 shows the WL voltage control circuit. When the row decoder address (RDA) are selected (Hi), the WL is pulled up to 1.8 V for read/write operation. Otherwise, the WL is pulled down to negative voltage for the standby mode. Notably, the source and bulk junction of nMOS FET becomes forward biased during the standby mode. A WL control circuit is simulated to justify the power needed by the negative supply. Fig. 10 shows the source current of the nMOS FET and the power dissipation when the negative voltage is varied from −0.8 to 0 V. The power dissipation of the negative supply is 686 nW when the negative voltage is −0.7 V. However, if a small negative voltage (smaller than 0.45 V) is applied, the power dissipation of the negative supply will be reduced much more.

Besides the NWL scheme, we use several approaches to maintain operating speed while save power.

1) The 4-kb memory array is partitioned into four 1-kb banks. A predecoder controls the bank enable signals to reduce the accessing memory capacity, as shown in Fig. 11.
2) The pulse operation [11] is adopted to shorten the memory access time. A duty clock (DCLK) is generated by a pulse generator which detects the rising edge of the clock (CLK) and then generates a pulse with fixed width regardless of the width of the CLK, as shown in Fig. 12. The DCLK gates the bank select signal, predischarge (PD) enable signal, and sensing amplifier enable (SAEN) signal into an SRAM bit slice to avoid any unwanted current when the access operation is finished. Fig. 13 illustrates the operations of the PLNA loadless 4-T CMOS SRAM cell. Fig. 13(b) is the write operation which writes 1 into a cell. Fig. 13(c) is the read operation which reads 0 from a cell.
3) Referring to the SA [12] in Fig. 14, NM21–NM24 consists the current-mode amplifier stage, while NM25, NM26, PM25, and PM26 are the voltage-mode amplifier stage of the SA. The small input impedance of the current-mode amplifier alleviates the loading effect on the bitlines of SRAM cells such that the sensing speed is enhanced. The voltage-mode amplifier is reponsible for boosting the logic levels to full swing. An SAEN signal is used to eliminate unnecessary dc current when the memory in the standby mode or the write operation.

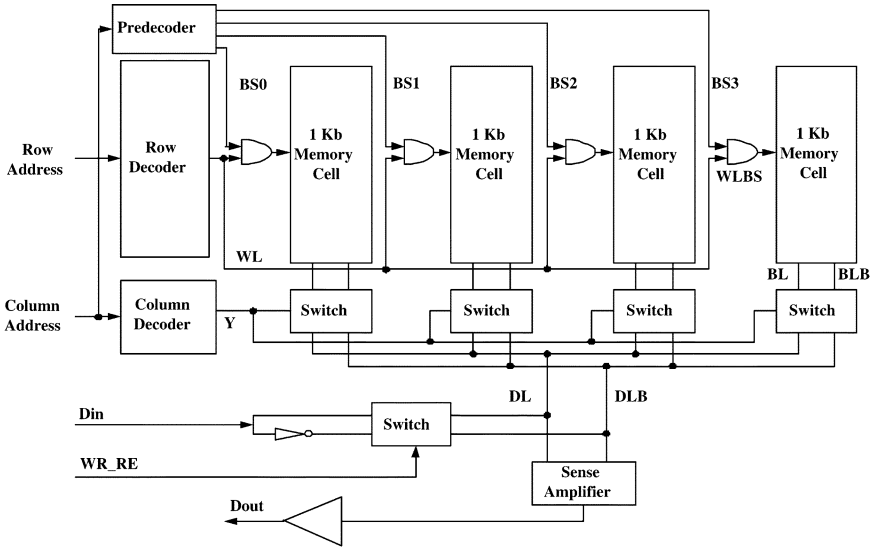


Fig. 11. Architecture of the proposed SRAM.

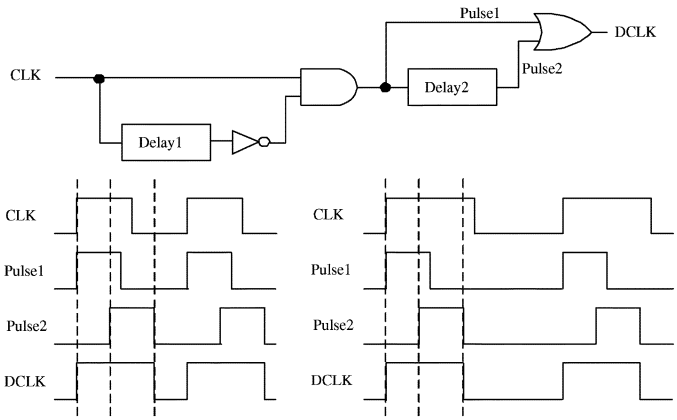


Fig. 12. Fixed-width pulse generator.

III. Simulation, Implementation, and Measurement

A. Simulation

The proposed design is implemented by TSMC (Taiwan Semiconductor Manufacturing Company) 1P6M 0.18 μm CMOS process. The chip area with pads is 781.258×806.63 μm^2. The SRAM cells may have function errors due to MOS size mismatches, pulse noise, or $V_{\rm DD}$/GND noise. In general, we can summarize the dc noise effect by static noise margin (SNM) analysis, and summarize the pulse-noise effect by dynamic noise margin (DNM) analysis. Fig. 15 shows the test circuit for simulating the SNM and the simulation results which is given TT model, 25 °C, VDD = 1.8 V. Fig. 16 shows the SNMs of the proposed 4-T cell and the 6-T cell given TT model, 25 °C, $V_{\rm DD} = 1.8$ V. Both cells use identical size nMOS FETs (0.22 μm/0.18 μm) and identical size pMOS FETs (1 μm/0.18 μm). Fig. 17, then, shows the SNMs of the proposed 4-T cell and the 6-T cell given TT model, 75 °C, $V_{\rm DD} = 1.8$ V. The simulation results reveal that the stability of proposed 4-T cell is the same as that of the 6-T cell in higher temperatures. Fig. 18 shows the SNM of the proposed 4-T cell and the 6-T cell given the worst case (FS model, 0 °C, $V_{\rm DD} = 1.62$ V). At least 200 mV of SNM is required to obtain sufficient yield with megabit scale SRAMs [13]. Although the SNM of the proposed 4-T cell is small than 200 mV at worst case, the SNM of the 6-T cell is the same as that of the proposed 4-T cell. Moreover, the SNM can be improved if the length of nMOS FETs is increased or a dual threshold 4-T cell is adopted [5]. According to the discussion above prove that the stability of the loadless 4-T SRAM cell is no worse than 6-T SRAM cell. Fig. 19 shows the test circuit for analyzing the DNM and the simulation results.

Besides the architecture shown in Fig. 11, the proposed memory also comprises a built-in self test (BIST) circuit as shown in Fig. 20. The post-layout simulations of the chip are tabulated in Table II. The worst-case average power is 0.29 mW in the standby mode. The longest access time is 3.38 ns and access average power is 23.38 mW in R/W mode. The highest operating clock frequency is 250 MHz. Fig. 21 shows the worst-case post-layout simulation result give by TimeMill at 75 °C, SS model, $V_{\rm DD} = 1.6$ V, and $D_{\rm out}$ load is 15 pF. In Fig. 21, we write 0 and 1 to two adjacent memory cells and then read data from these cells. Address latching and data accessing are executed at positive edges of the CLK. WR_RE is the read/write control line of which logic 1 is the write operation, and logic 0 denotes the read operation.

B. Implementation & Measurement

An IMS ATS100 logic master is used to perform chip test and measurement. The maximum operating clock frequency supported by the mentioned instrument is only 100 MHz. The functions of the general (synchronous) mode and BIST mode have been proved by the testing of continuous read/write of row/column addresses. Fig. 22 shows the measured waveform of read/write operations. In Fig. 22, we write 0,1,0,1,1,0,1,0, continuous 0 and continuous 1 to 4 rows and 1 to 4 columns, i.e., 16 adjacent memory cells. Then, read data from these cells. The proposed SRAM still works when the output data fetch delay of the IMS ATS100 logic master be set to 3.80 ns, which indicates the highest operation speed of the proposed design is 263 MHz. Fig. 23 shows that the power consumption of the proposed chip is a function of the clock rate. The curve (1) is the average power consumption for the WL $\rm voltage = 0$ V,

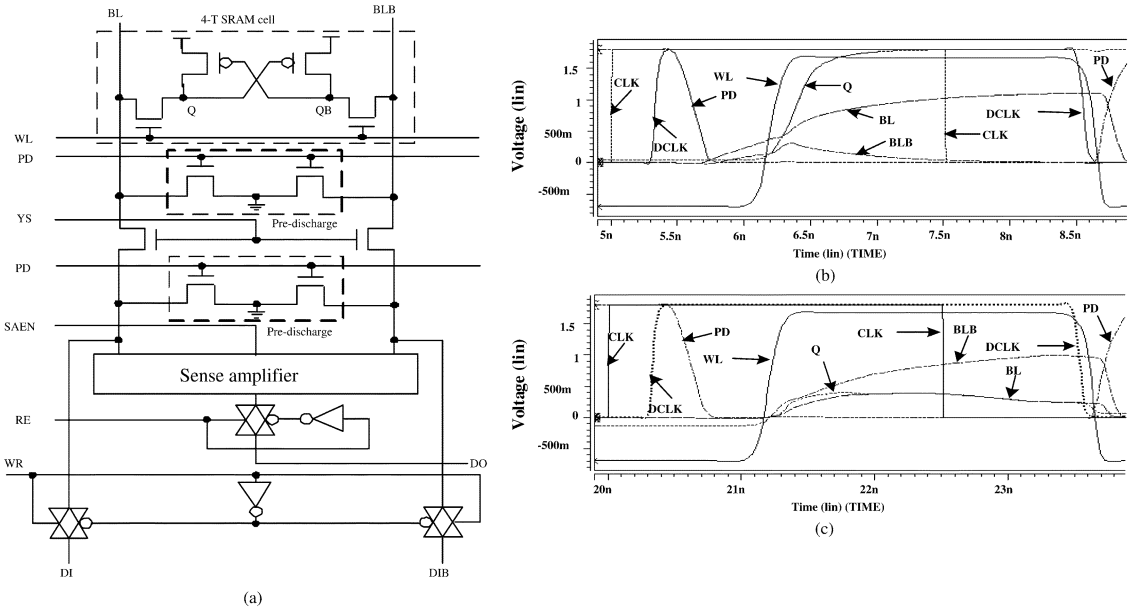


Fig. 13. PLNA loadless 4-T CMOS SRAM cell operations.

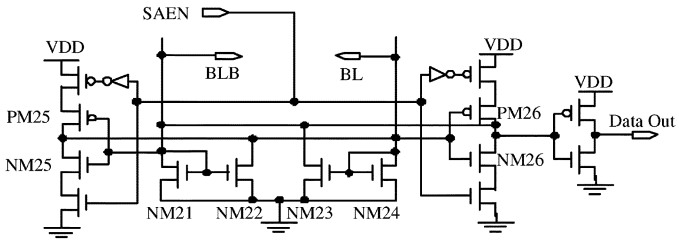
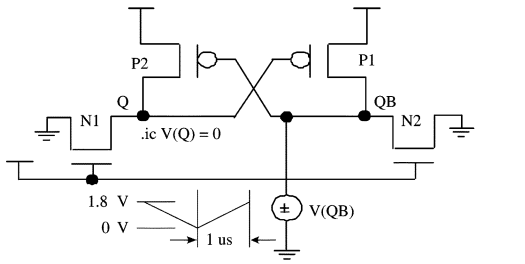


Fig. 14. SA circuit with enable control.



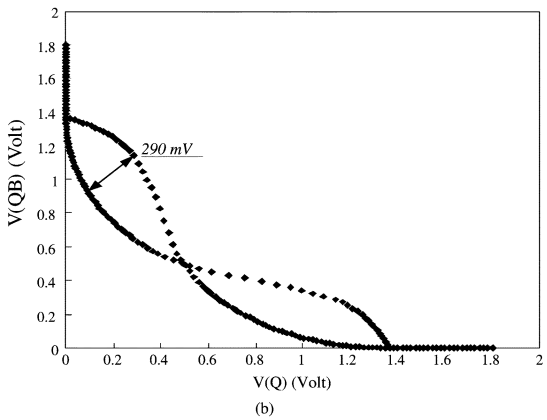


Fig. 15. Test circuit and measured butterfly curve for SNM.

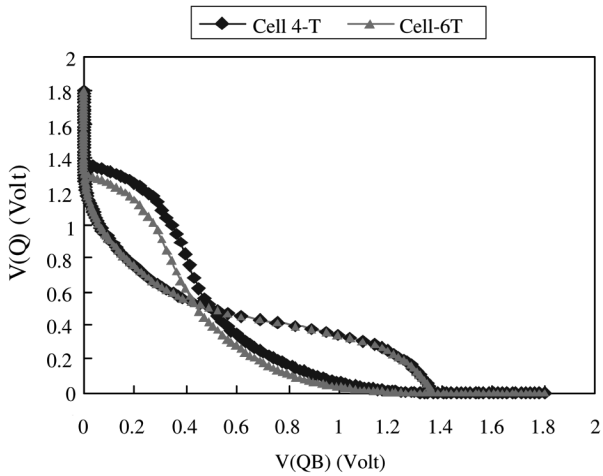


Fig. 16. SNM of the proposed 4-T cell and the 6-T cell given TT model, 25 °C, $V_{\mathrm{DD}} = 1.8$ V.

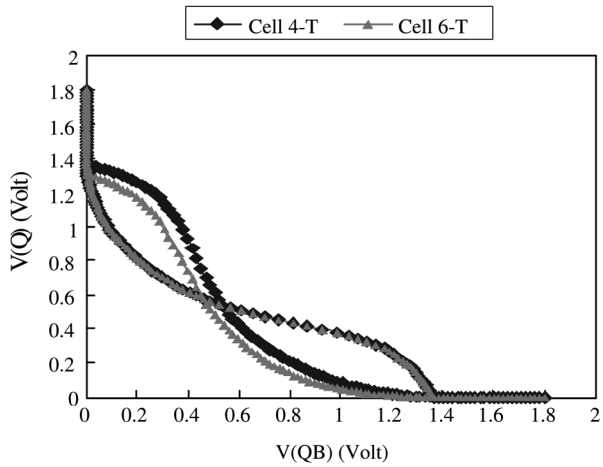


Fig. 17. SNM of the proposed 4-T cell and the 6-T cell given TT model, 75 °C, $V_{\mathrm{DD}} = 1.8$ V.

while the curve (2) is the average power consumption for the WL voltage $= -0.7$ V. Notably, the power consumption in the standby mode is 0.55 mW for 0-V WL voltage, while the power consumption in the standby mode is 0.32 mW for -0.7-V WL voltage. The average power consumption of the curve (2) is roughly 0.23 mW lower than that of the curve (1) regardless of

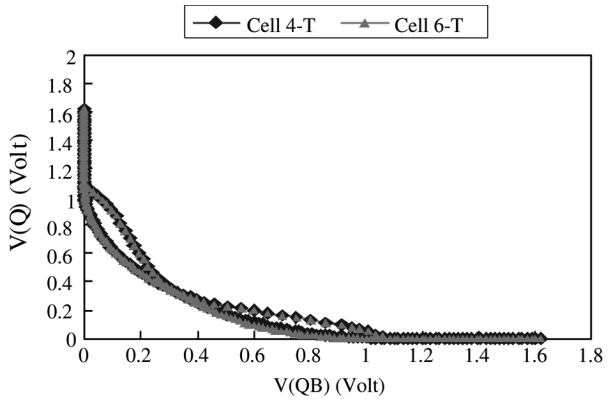


Fig. 18. SNM of the worst case (FS model, 0 °C, $V_{DD} = 1.62$ V).

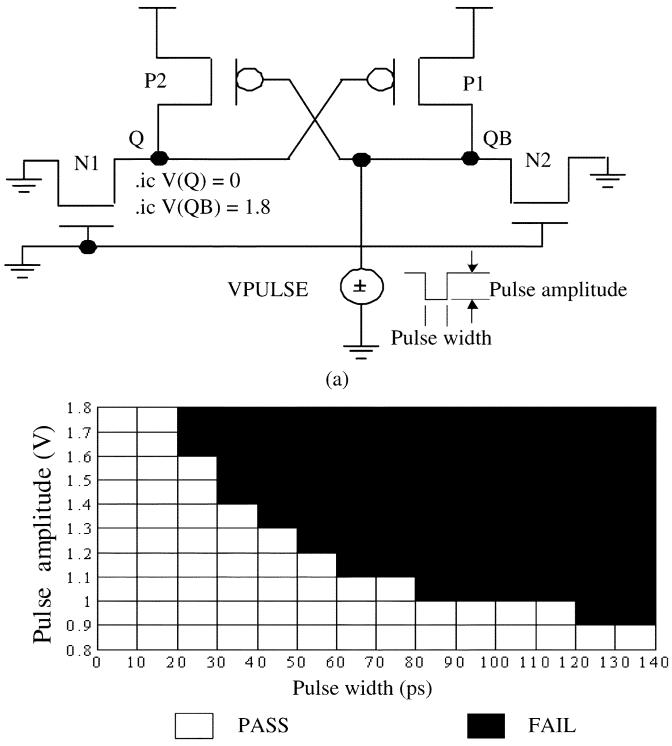


Fig. 19. Test circuit and shmoo plot for dynamic noise margin.

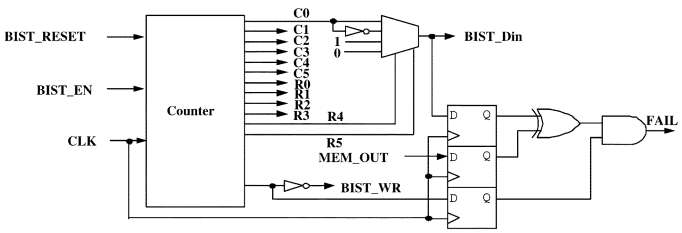


Fig. 20. BIST circuit.

the clock rate. Table III summarizes the physical measurement results. A power consumption and power-delay product comparison with several prior works is shown in Table IV. It is obvious that the proposed design possesses the smallest power consumption and power-delay product per bit and per megahertz.

TABLE II
PHYSICAL MEASURING RESULTS

Normal Mode	Clock	250 MHz
	Access Time	3.38 ns
	VDD	1.8 V
	Avg. Power	23.38 mW
	Max. Power	130.27 mW
BIST Mode	Clock	100 MHz
	VDD	1.8 V
	Avg. Power	11.91 mW
	Max. Power	95.83 mW
Standby Mode	Positive Avg. Power	0.11 mW
	Negative Avg. Power	0.18 mW

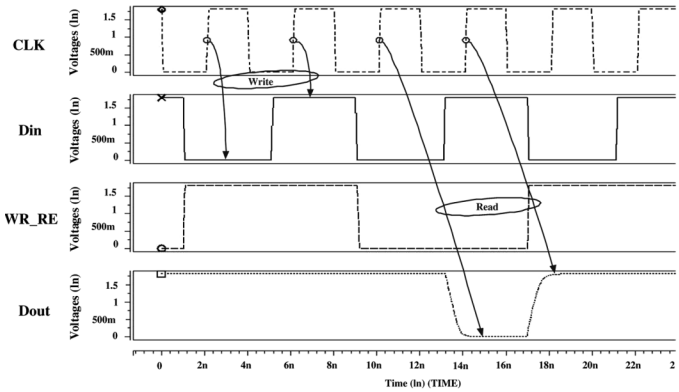


Fig. 21. Worst case post-layout simulation.

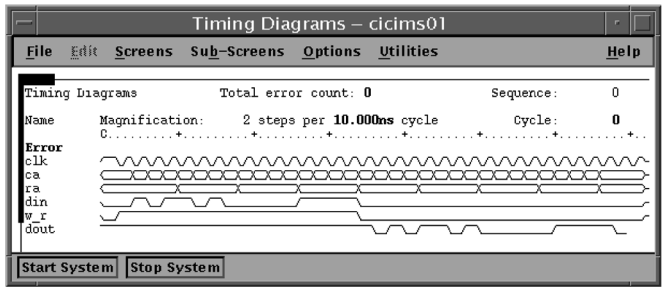


Fig. 22. Measured waveform of the read/write operation.

TABLE III
PHYSICAL MEASURING RESULTS

Max. Freq.	100 MHz (*)
Estimated Max. Freq.	263 MHz
Avg. Power	6.44 mW (100 MHz, 1.8 V)
Access Time	3.8 ns
Standby Power	0.32 mW (‡)

* : Limited by the measurement instrument (IMS ATS100).
‡ : Positive supply power + Negative supply power.

IV. CONCLUSION

We have revealed a 4-kb 4-T CMOS SRAM by using the NWL scheme to achieve low power dissipation. The proposed design does not need any special CMOS process, e.g., multiple-well layers. The leakage current of the cell-access transistors is kept minimum as long as WL voltage is below − 0.4 V. Hence, the power consumption of the inactive cells in the standby mode is drastically reduced.

TABLE IV
COMPARISON OF POWER-DELAY PRODUCT

	[5]	[10]	Proposed
CMOS Process	1P6M 0.18 μm		
Power	152 mW (500 MHz)	182 mW (667 MHz)	23.4 mW (250 MHz) ($\ddagger$)
Power/(bit*MHz) (nW/MHz)	74.22	66.62	22.85
Access Delay (ns)	2.49	2.2	3.38
Power*Delay/(bit*MHz) (ns*nW/MHz)	184.8	146.56	77.24

$\ddagger$: Positive supply power + Negative supply power.

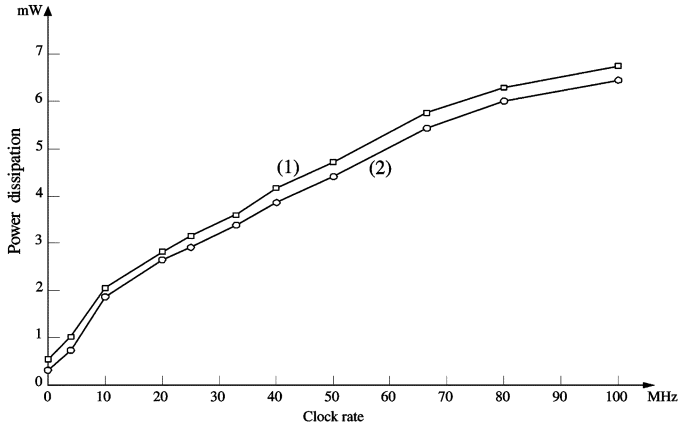


Fig. 23. Power consumption of the proposed SRAM as a function of the clock rate.

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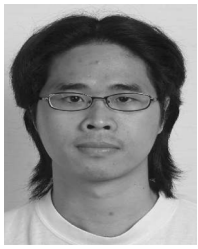

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