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Voltage-to-frequency converter with high sensitivity using all-MOS voltage window comparator

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Abstract

A high-sensitivity voltage-to-frequency converter (VFC) using an all-MOS voltage window comparator is presented in this work. The circuit is composed of one voltage-to-current converter, one charge and discharge circuit, and one all-MOS voltage window comparator. The input voltage is converted into a current which in turn triggers the charge and discharge circuit, where a built-in capacitor is driven. The voltage window comparator monitors the variated voltage on the capacitor and generate an oscillated output of which the vibration frequency is linearly dependent to the input voltage. In this way, the worst-case linear range of the output frequency of the proposed VFC is 0–55.40 MHz verified by simulations given a 0–0.9 V input range. The physical measurement of the proposed VFC shows a 0–52.95 MHz output frequency given a 0–0.9 V input range. The error in linearity is better than 8.5% while the power dissipation is merely 0.218 mW.

Keywords: Voltage window comparator; Voltage-to-frequency converter; CMOS; Voltage detection

1. Introduction

Lots of work have been done to develop the methods for designing sensors which convey information, the values of passive or active elements, into the oscillation parameters, e.g., the magnitude, phase, frequency, or duty cycle of the vibration. The values to be conveyed might be functions of some other factors, e.g., mechanical pressure, magnetic field, or temperature. The variation of the oscillation must faithfully track the corresponding change in these factors. Hence, bandwidth, sensitivity, and linearity are the most important measures to judge the quality of these circuits. Converting the physically estimated values into oscillations is much preferred because the oscillations are more noise immune. Thus, the correctness of the information can be ensured. A traditional VCO (voltage-controlled oscillator) cannot fulfill such a demand, because the linearity and sensitivity of such a conversion are required.

This paper presents a high-bandwidth linear interfacing circuit which converts the sensed voltage into frequency. The frequency output is very much noise resistant compared to other types of outputs, e.g., the magnitude of current or voltage. It meets the requirement for integration with other IP (intellectual property), e.g., uP or communication MAC (media access circuitry). In contrast to the bipolar or BiCMOS implementations [1,2] the proposed design is realized in TSMC (Taiwan Semiconductor Manufacturing Company) 0.25 μm 1P5M CMOS technology. It possesses the advantages of low power, small area and high bandwidth. Although there were several prior CMOS-based converters, they either required an extra OSC [3], or additional timing control signals and many switched capacitors [4], which became overhead in those designs. By contrast, our proposed voltage-to-frequency converter (VFC) is composed of one voltage-to-current converter (V-to-I), and one charge and discharge circuit (CDC) which is driven by the voltage

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window comparator (VWC). The physical measurement of the proposed VFC on silicon shows a 0–52.95 MHz output frequency given a 0–0.9 V input range.

2. CMOS voltage-to-frequency converter

The basic theory of voltage-to-frequency conversion is to track the back-and-forth variations of a certain signal level in a pre-determined range. Thus, not only can it be easily carried out by low-cost CMOS technology, but neither external oscillators nor internal PLLs are required in the design.

2.1. Architecture of the proposed VFC

The proposed VFC is shown in Fig. 1. The input voltage, V_I, is converted into a current signal, I_I, by a V-to-I circuit. I_I is fed to the CDC to generate a reference voltage, V_{cap}, which is provided to the following VWC. VWC uses with two pre-defined reference voltages, VH (voltage high) and VL (voltage low), which determine the range of the voltage window. During the normal operation, V_{cap} will be charged and discharged between the reference voltages, VL and VH. In the charging operation, V_{cap} is charged. VWC compares V_{cap} with VH and generates VOUT = 1 (2.5 V) for $V_{cap} < VH$. When $V_{cap} > VH$, VOUT = 0 is generated

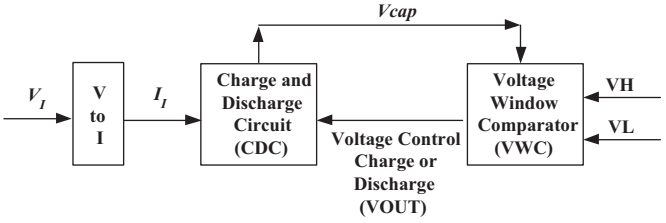

Fig. 1. Architecture of the proposed VFC.

to discharge a storage capacitor in CDC. Thus, V_{cap} is discharged. In the discharging operation, VWC compares V_{cap} with VL. The comparison results VOUT = 0 (0 V) and VOUT = 1 (2.5 V) are generated for $V_{cap} > VL$ and $V_{cap} < VL$, respectively. VOUT = 1 causes V_{cap} to be charged. Thus, a repeated loop is built and VOUT is the output periodical oscillation.

2.2. Schematic design of VFC

The schematic of VFC is shown in Fig. 2. An OPA (operational amplifier) feeds a gate drive to an NMOS, NM21. The negative terminal of the OPA is connected to ground through a resistor, R_T. Thus, the current is dependent on the resistor, R_T. Notably, the length of all of the MOS transistors are set to be at least 5 times of the feature size (0.25 μm) to avoid any short-channel effect. The width of PM21 is M times that of PM22 and PM23. Hence, the charging current for C_T will be $1/M$ of the current flowing through R_T and NM21. Notably, VDD is 2.5 V for this design.

In addition to the input voltage V_I, another input for resetting the entire VFC is required, i.e., V_{INIT}, which will be described later with the VWC circuitry. The charge–discharge operation besides the initialization stage is described as follows.

Charging operation: The switch SW1 is shorted to node a1. Then, the storage capacitor, C_T, starts to be charged via saturated PM23.

Discharging operation: As soon as the voltage of the C_T, V_{cap}, reaches VH, the output of VWC, VOUT, is switched low to short-circuit SW1 to node b1. NM23 is tuned to be able to sink a current which is twice of the charging current provided by PM23. Thus, C_T is discharged. As soon as the V_{cap} is pulled down to VL, VOUT will be turned high to start another cycle of charging-and-discharging operation.

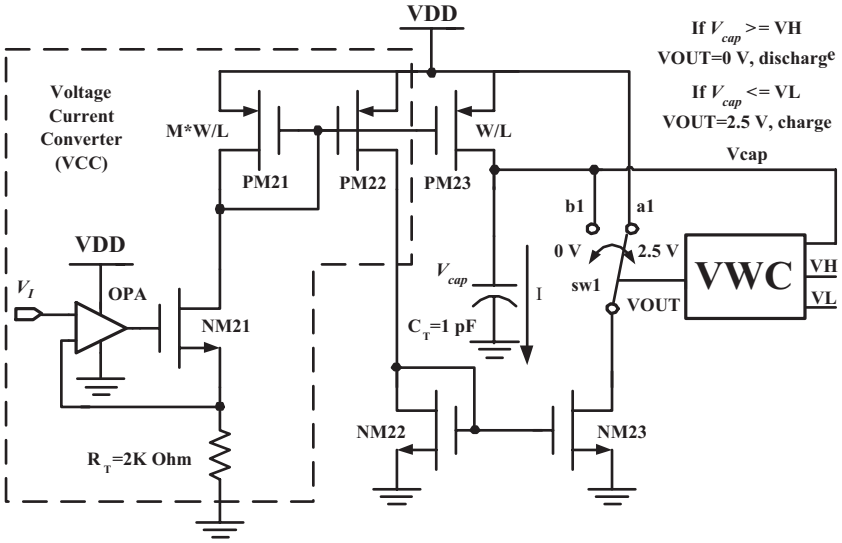

Fig. 2. Schematic of the proposed VFC.

It is concluded that the oscillation frequency of VOUT is governed by the following equation:

$$f_{\text{out}} = \frac{V_{\text{I}}}{2 \cdot C_{\text{T}} \cdot R_{\text{T}} \cdot (\text{VH} - \text{VL}) \cdot M}. \quad (1)$$

Notably, since all of the parameters, i.e., M, C_{T}, R_{T}, VH, and VL, can be pre-determined. Eq. (1) is reduced to be $f_{\text{out}} = K \cdot V_{\text{I}}$, where K is a constant derived from all of the mentioned parameters.

2.3. All-MOS voltage-to-current converter

As mentioned in the previous sections, a circuit to convert the input voltage into a current linearly is required at the input stage of the entire design. We use a voltage-to-current converter with a small resistor since TSMC 1P5M CMOS process provides very accurate resistors made with polysilicon. Besides, a folded-cascode type of OPA [5] is used to drive NM21 in Fig. 2. Hence, the generated current is summarized to be

$$I_{\text{conv}} = \frac{V_{\text{I}}}{R_{\text{T}}}. \quad (2)$$

The simulated V–I curve is given in Fig. 3. The linearity is very much ensured, which implies the sensitivity of the current in PM22 is 316.25 μA/V in the range from 0 to 1.2 V.

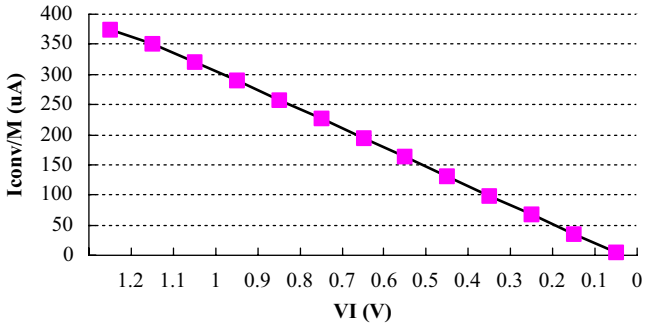

Fig. 3. I_{conv} vs. V_{I} in simulation.

2.4. All-MOS voltage window comparator (VWC)

Referring to Fig. 4, since SW4 is switched to node b4 to set the VOUT = 2.5 V initially as we mentioned, SW2 is connected to a2 and SW3 is to a3 at this moment. The differential amplifier formed by PM51, PM52, NM54, and NM55 is driven by VH and V_{cap} which is the voltage of C_{T}. Thus, C_{T} is charged initially. As soon as V_{cap} is larger than VH, most of the current supplied by VDD is switched to I_{52} such that I_{51} approaches zero to pull up the gate drive of the inverter composed of PM55 and NM58. VOUT is then switched to 0 V.

When VOUT is pulled low, SW2 is connected to b2 and SW3 is to b3. The differential amplifier formed by PM53, PM54, NM56, and NM57 is driven by VL and V_{cap}. C_{T} is discharged gradually this time. As soon as V_{cap} is smaller than VL, most of the current supplied by VDD is switched to I_{54} to apply a low gate drive of the inverter composed of PM55 and NM58. Certainly, I_{53} becomes zero at the same time. Hence, VOUT is switched high.

The two differential amplifiers execute the comparison of voltages alternatively such that the oscillations of VOUT are ensured. The purposes of adding an inverter at the output are flipping the state to generate the oscillation and

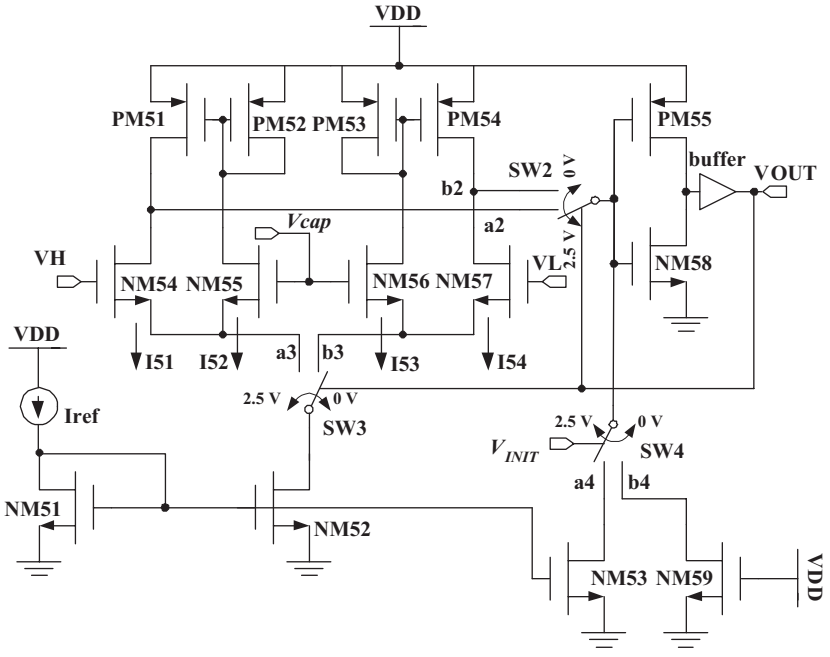

Fig. 4. Detailed schematic of the VWC.

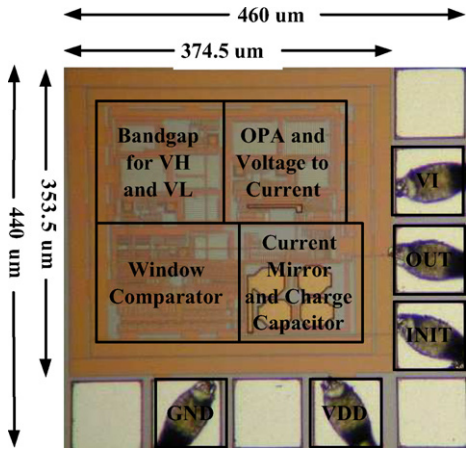

Fig. 5. Die photo of the proposed VFC.

increasing the driving current to the output. In addition, the zero-delay hazard is also avoided.

It is noted that V_{INIT} in Fig. 4 is reset initially such that it is out of the range defined by VL and VH. Hence, VOUT at the initialization is pulled high to 2.5 V.

3. Implementation of VFC on silicon

The proposed VFC is implemented by using TSMC 0.25 μm 1P5M technology. The die photo of the physical VFC on silicon is shown in Fig. 5. The chip size is $440 \times 460\,\mu m^2$, while the core size is $374.5 \times 353.5\,\mu m^2$. The worst-case simulated working range of the input voltage is 0–0.9 V, while the output frequency is 0–55.40 MHz.

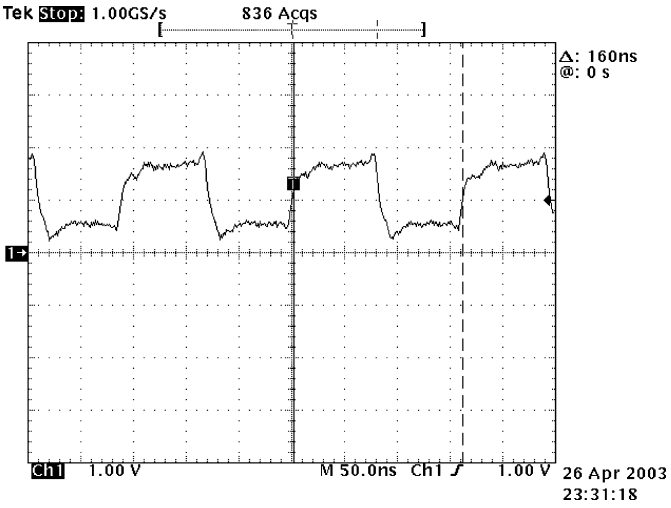

Fig. 6. Output waveform given 0.1 V input.

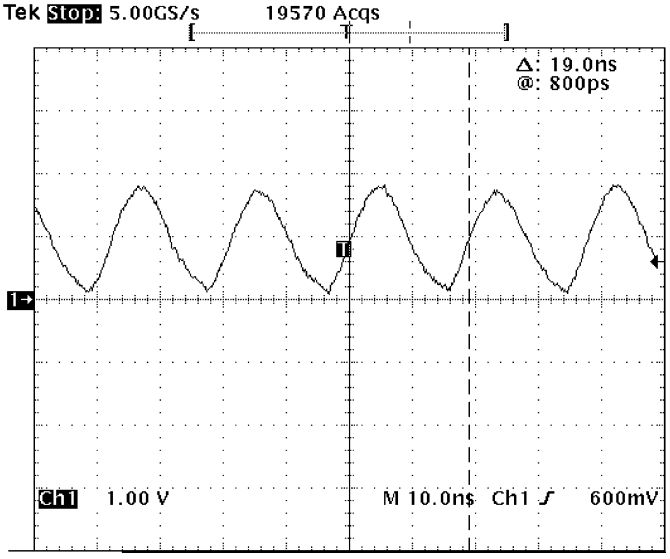

Fig. 8. Output waveform given 0.9 V input.

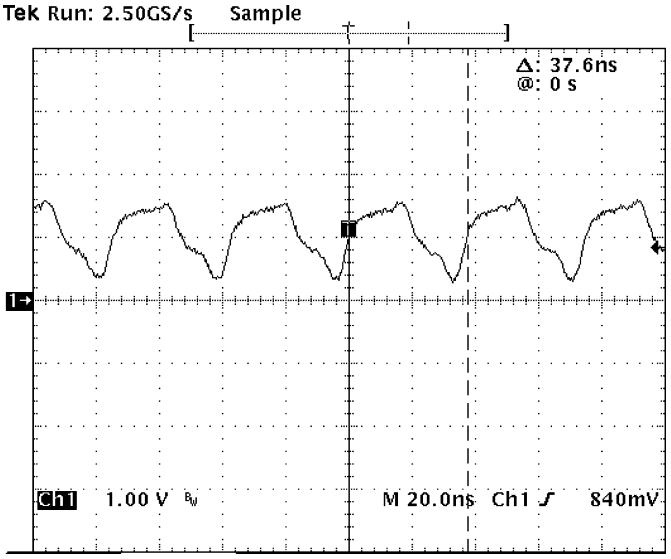

Fig. 7. Output waveform given 0.4 V input.

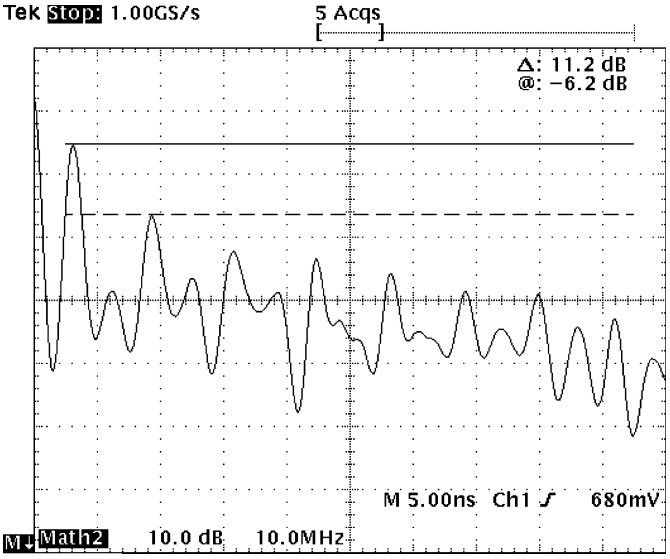

Fig. 9. Output spectrum given 0.1 V input.

Tektronix TDS 680B oscilloscope, HP 8594E Spectrum Analyzer, and HP 1660CP Logic Analyzer are used to measure the performance of the proposed VFC. Figs. 6, 7, and 8, are the measured output waveform in the time domain given 0.1, 0.4, and 0.9 V input, respectively. The output frequencies at these input voltages are 6.184, 26.76, and 52.95 MHz, respectively. The rise time and fall time of the waveform in Fig. 8 approximate to 10 ns, which is mainly resulted from the capacitor load (about 8 pF) of the probe. The 10 ns rise time and fall time would distort the maximum output frequency of 52.95 MHz whose period is around 19 ns. Notably, the distortion is resulted from the parasitic capacitor of the probe. Hence, the severe distortion is predicted to be removed when the probe is disconnected. Furthermore, the distortion would not happen when common commercial chips are driven because their equivalent input capacitance are far less than 8 pF. Moreover, the shape distortion of the square wave in time domain is equivalent to the attenuation of high frequency components. Therefore, the exact output frequency of the VFC can be obtained in frequency domain according to the fundamental frequency to discard the distorted shape in time domain, as shown in Figs. 9–11. The measured spectra show the fundamental frequency and the attenuated harmonics.

The overall output frequency vs. input voltage measurement is summarized in Fig. 12, where the expected values are the ideal values computed from a linear formula. Fig. 13 reveals the error in Fig. 12. The error of f_{out} is computed by firstly subtracting the simulated or measured output frequencies from the expected values which are

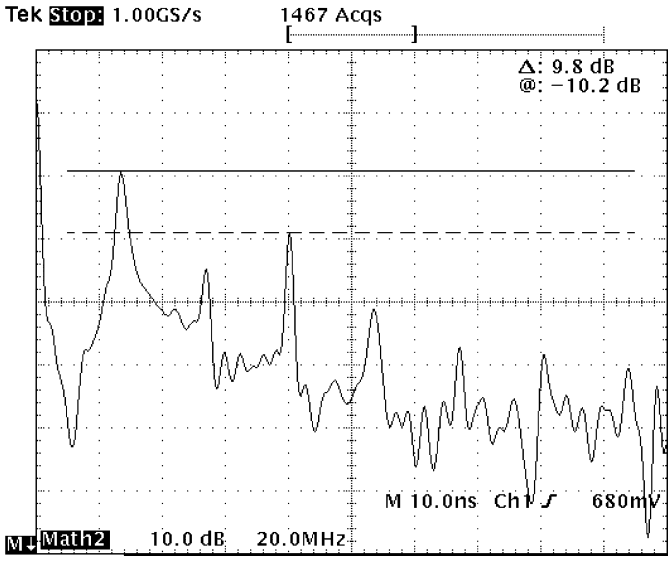

Fig. 10. Output spectrum given 0.4 V input.

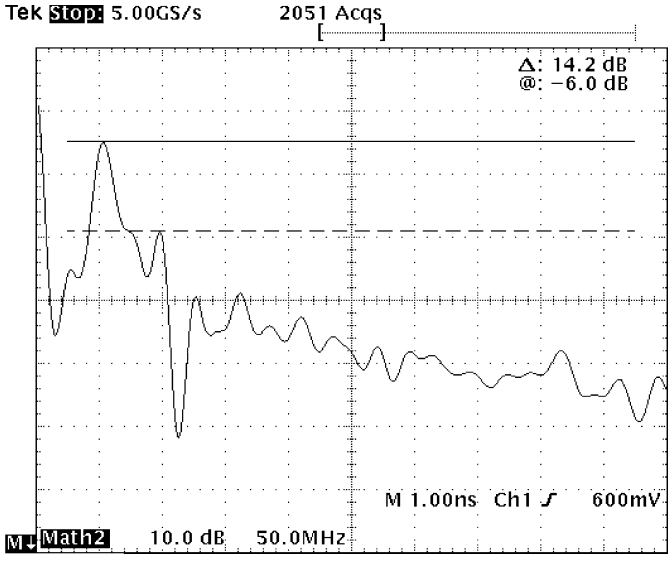

Fig. 11. Output spectrum given 0.9 V input.

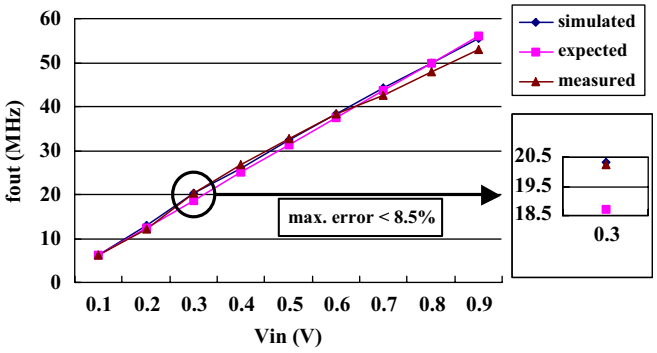

Fig. 12. Comparison of the measured, the expected, and the simulated f_{out}.

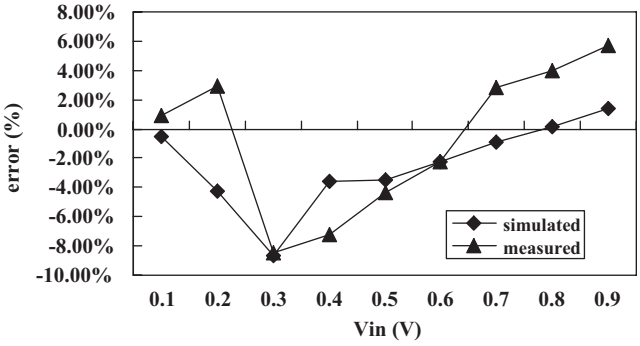

Fig. 13. error (accuracy) of f_{out}.

Table 1
Characteristics of the proposed VFC design

	Simulation	Measurement
V_{in}	0–0.9 V	0–0.9 V
Temperature	−25° to 75 °C	−25° to 75 °C
Technology	0.25 μm 1P5M CMOS	0.25 μm 1P5M CMOS
Max. O/P freq.	55.40 MHz	52.95 MHz
Error	⩽8.5%	⩽8.5%
Sensitivity	⩾58 MHz/V	⩾58 MHz/V
Power max. f_{out}	0.17533 mW	0.218 mW
Chip area	440 × 460 μm^2	440 × 460 μm^2

Table 2
Comparison to prior designs

	Ours	[1]	[3]	[4]	[6]	[7]
Technology	CMOS	BiCMOS	CMOS	CMOS	N/A	CMOS
Max. f_{out}	52.95 MHz	100 KHz	8 KHz	100 KHz	3.5 KHz	7 KHz
V_{in}	0–0.9 V	0–6 V	0.1–10 V	0–10 V	0–5 V	0–3 V
Sensitivity	58 MHz/V	16 KHz/V	0.8 KHz/V	10 KHz/V	0.7 KHz/V	2 KHz/V
Error	<8.5%	<2%	0.02%	N/A	<1%	1.95%
FOM	6.82	0.008	0.04	N/A	0.0007	0.00102
Year	2006	1994	1997	1988	2002	2004

given the same input voltage. Then, the subtraction results are divided by the maximum output frequency to obtain the error of frequency in a percentage form, as shown in Fig. 13. The maximum error is less than 8.5% given the operating condition of a 10% VDD variation and the temperature range from −25 to 75 °C. An error of 8.5% of the proposed VFC in linearity seems a little large. However, high sensitivity of the proposed VFC can overwhelm the error in the linearity. Thus, a figure of merit (FOM = sensitivity (MHz)/error (%)) can be defined to justify the specifications.

The overall characteristics of the proposed design by measurement is tabulated in Table 1. The measured sensitivity is derived to be $52.95/0.9 = 58.83$ MHz/V. We also make a comparison of our design and several prior VFC designs in Table 2. Notably, the output frequency of [7] is from 1 to 7 KHz given a 0–3 V input. Thus, the sensitivity of [7] is 2 KHz/V. It is obvious that our design outperforms the rest in the categories of the maximum output bandwidth, and sensitivity. Last but not least, the FOM of the proposed design is very much larger than that of the prior VFCs, as shown in Table 2.

4. Conclusion

This paper has proposed a high-bandwidth VFC. Not only are the sensitivity and output frequency dramatically improved, but the overall manufacturing cost is reduced by not using BiCMOS, and clock control circuitry. On top of these advantages, the proposed VFC consumes only 0.218 mW.

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