An All-MOS High-Linearity Voltage-to-Frequency Converter Chip With 520-kHz/V Sensitivity

Chua-Chin Wang, *Senior Member, IEEE*, Tzung-Je Lee, *Student Member, IEEE*, Chi-Chen Li, and Ron Hu

***Abstract*—An all-MOS linear voltage-to-frequency converter (VFC) chip with 520-kHz/V sensitivity is presented in this paper. This circuit converts an input voltage into frequency by charging and discharging a capacitor. An all-MOS voltage window comparator (VWC) with reduced propagation delay is designed to improve the linearity of traditional VFCs. The propagation delay of the VWC is discussed to resolve the tradeoff between bandwidth and linearity of VFC. The proposed VFC is verified on silicon using the Taiwan Semiconductor Manufacturing Company 1P5M 0.25-μm process. The measurement results show that the linearity error is less than 1%, and the sensitivity is 520 kHz/V at an input voltage range from 0.1 to 0.8 V.**

***Index Terms*—Linearity, sensitivity, voltage window comparator (VWC), voltage-to-frequency converter (VFC).**

I. Introduction

VOLTAGE-TO-FREQUENCY converters (VFCs) are quite popular devices due to their low cost and application versatility in variety of electronic control and measurement systems [1]. In measurement systems, the oscillation amplitude, frequency, or duty cycle of the multivibrators provide information on the value of passive or active elements which play roles as sensors of some other factors (e.g., mechanical pressure, magnetic field, or temperature) [2]. To maintain the transform accuracy, the variation of the oscillation should be reliable functions of the corresponding change of these sensed values. Thus, the bandwidth, sensitivity, and linearity are the most important measures to judge the quality of VFC. These measures also differentiate the VFC and the voltage-controlled oscillator (VCO). Besides, the VFC gives more noise immunity in these measurement systems by converting information into oscillation frequency.

A traditional current steering method to design VFCs is converting voltage to current and then into frequency [2], [3]. Pease showed this idea to design a VFC and used discrete components to verify it on PCB board [3]. Filanovsky's design was implemented by using bipolar junction transistors (BJTs) on breadboard [2]. Filanovsky's experiment results revealed that the current steering method easily achieved high bandwidth (100 Hz to 100 kHz), but had a poor linearity (the error is more than 2%). Thus, Trofimenkoff presented a square-rooting VFC based on a clock-controlled one-shot circuit, an integrator, and a filter to provide a 0.02% transformation linearity with full-scale frequency of 4 kHz. However, square-rooting VFC attains high linearity at the cost of decreased bandwidth and excess power consumption from the 1.024-MHz clock. Besides, the square-root relation between the output frequency and the input voltage limits the application range, e.g., for liquid or gas orifice and Venturi flow measurement devices [4]. Later, a new Σ-Δ VFC presented by Stork was capable of less than 1% linearity (16–18-b linearity) [1]. Nevertheless, a low jitter clock was required, and the bandwidth was reduced to 3.5 kHz in Stork's design. A different method using a switched-capacitor circuit could achieve maximum operation frequency as high as 100 kHz [5]. However, its linearity was drastically dependent on the frequencies of two on-chip clocks.

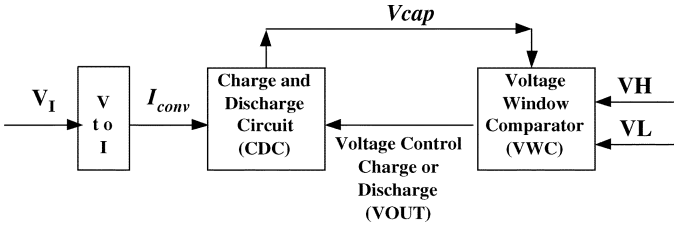

Fig. 1. Building blocks of the proposed VFC.

Thus, we present a VFC which keeps the high-bandwidth feature of the traditional VFC but attains a better linearity by using an all-MOS VWC. This circuit is verified on silicon using the Taiwan Semiconductor Manufacturing Company (TSMC) 1P5M 0.25-μm process to have linearity better than 1%, 416-kHz bandwidth, and 520-kHz/V sensitivity.

II. All-MOS VFC

The basic theory of the proposed VFC is to track back-and-forth variations of a certain signal in a predetermined range. Thus, no additional accurate oscillators or PLLs are required. In addition, the low-cost CMOS technology is very suitable to carry out this circuit.

A. Architecture of the Proposed VFC

The building blocks of the proposed VFC are shown in Fig. 1. The input voltage V_I is converted to current $I_{\rm conv}$ by a V-to-I circuit and then sent into the charge and discharge circuit (CDC). CDC generates a voltage $V_{\rm cap}$ whose slope is dependent on $I_{\rm conv}$. $V_{\rm cap}$ is then tracked by an all-MOS voltage window comparator (all-MOS VWC) in a predetermined range

Manuscript received October 3, 2005. This work was supported in part by the National Science Council under Grant NHRI-EX93-9319EI and Grant NSC 92-2218-E-110-001 and by the Ministry of Education, Taiwan, R.O.C., under the NSYSU Project,. This paper was recommended by Associate Editor H. Hashemi.

C.-C. Wang and T.-J. Lee are with the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, 80424, Taiwan, R.O.C. (e-mail: ccwang@ee.nsysu.edu.tw).

C.-C. Li is with The Analog Department, Terax Communication Technologies, Hsin-Chu 300, Taiwan, R.O.C.

R. Hu is with Asuka Microelectronics Inc., Hsin-Chu 300, Taiwan, R.O.C.

Digital Object Identifier 10.1109/TCSII.2006.876375

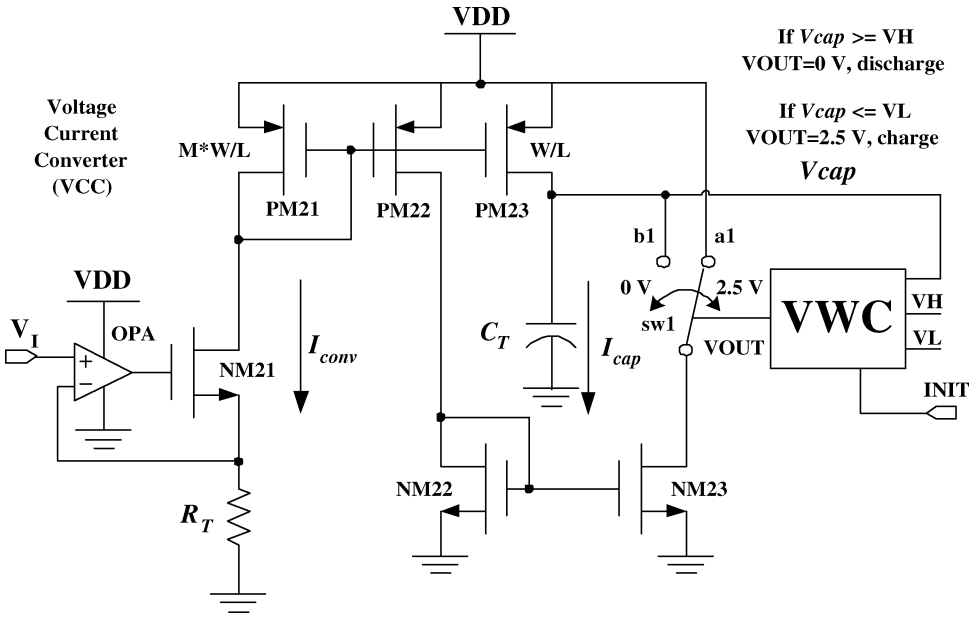

Fig. 2. Schematic of the proposed VFC.

bounded by two reference voltages VH and VL, where VH is higher than VL. When $V_{\rm cap}$ decreases lower than VL, VWC generates the comparison result $V{\rm OUT} = 1$ (2.5 V) to charge a storage capacitor in the CDC and pull $V_{\rm cap}$ to high. On the contrary, if $V_{\rm cap}$ goes higher than VH, the VWC changes its output to be 0 V ($V{\rm OUT} = 0$), which results in $V_{\rm cap}$ to be pulled down. In short, $V_{\rm cap}$ varies between VH and VL, and $V{\rm OUT}$ is the generated oscillation signal whose frequency is controlled by V_I.

B. Schematic of the Proposed VFC

Fig. 2 shows the schematic of the proposed VFC. OPA, NM21, PM21, and R_T constitute the voltage-to-current converter (V-to-I converter). According to the virtual ground principle, the minus input node of OPA equals V_I. Hence, the generated current $I_{\rm conv}$ is expressed as

$$I_{\rm conv} = \frac{V_I}{R_T}. \tag{1}$$

Notably, the length of all of the MOS transistors are set to be at least five times the feature size to avoid any short-channel effect.

The width of PM21 is M times of that of PM23 such that the mirrored current $I_{\rm cap}$ is $1/M$ times $I_{\rm conv}$.

The switch, sw1, which decides whether the storage capacitor C_T is to be charged or discharged, is controlled by the output signal (VOUT) of the VWC. The voltage drop of the capacitor $V_{\rm cap}$ and two reference voltages VH and VL are fed into VWC to be compared. While $V_{\rm cap}$ is larger than VH, the output signal ${\rm VOUT} = 0$ V is provided by VWC to connect sw1 to node b1 such that C_T is discharged. On the contrary, if $V_{\rm cap}$ is less than VL, VWC generates ${\rm VOUT} = 2.5$ V to switch sw1 to connect to node a1, resulting in C_T to be charged.

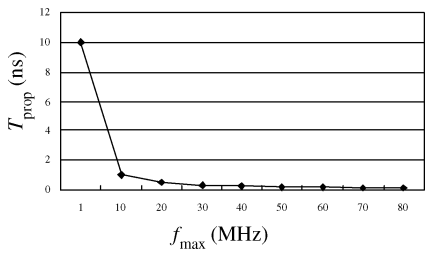

Fig. 3. Propagation delay of the VWC and the corresponding maximum operation frequency of the VFC at a condition of 1% linearity error.

According to the previous description, it is concluded that the ideal relation between the input voltage V_I to the output frequency $f_{\rm out}$ could be expressed as follows:

$$f_{\rm out} = \frac{V_I}{2 \cdot C_T \cdot R_T \cdot (VH - VL) \cdot M}. \tag{2}$$

Obviously, (2) is a linear function for $f_{\rm out}$ versus V_I if M, VH, VL, C_T, and R_T are predetermined.

C. Linearity of the Proposed VFC

Several nonideal effects might be considered carefully to ensure the linearity of the proposed circuit. First, in order to avoid the charge injection from the switch sw1, the dummy switches are required to be added. Second, although the offset voltage of the VWC results in the comparison error, it does not affect the linearity seriously due to the error cancellation between two comparisons per cycle. Finally, the propagation delay ($T_{\rm prop}$) of the VWC is the most important impact to the linearity. The analysis is as follows: the linearity error $(accuracy) = (f_{\rm real} - f_{\rm ideal})/f_{\rm max}$, where $f_{\rm max}$ is the maximum operating frequency of the

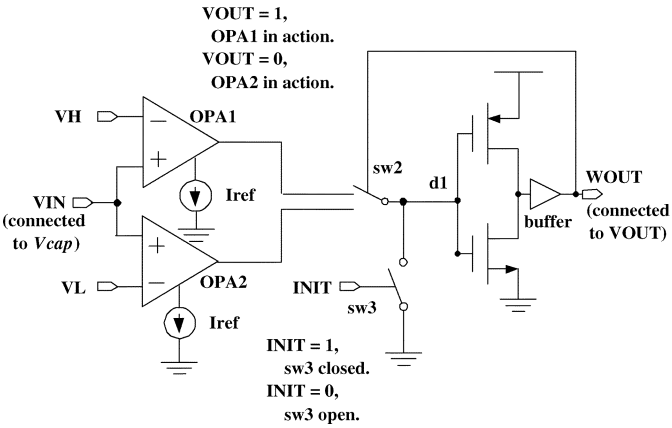

Fig. 4. Schematic of the VWC.

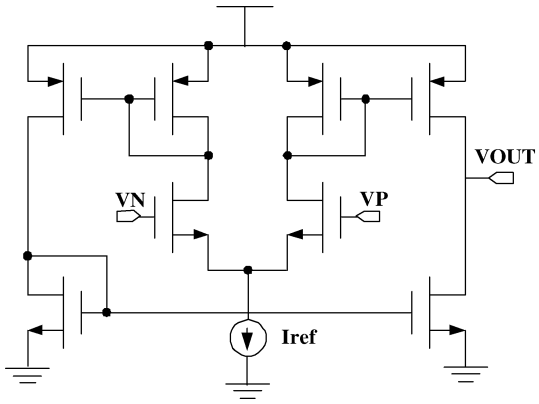

Fig. 5. Schematic of OPA1 and OPA2 in the VWC.

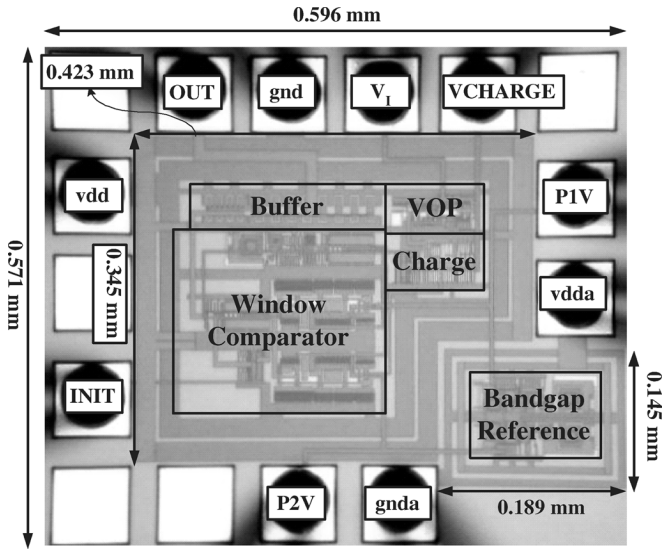

Fig. 6. Die photograph of the proposed VFC chip.

VFC, $f_{\text{ideal}} = 1/T_{\text{ideal}}$ is the ideal output frequency, and $f_{\text{real}} = 1/(T_{\text{ideal}} + T_{\text{prop}})$. In contrast with the varying T_{ideal} resulting form the varying V_I, T_{prop} is deemed as a constant value. Therefore, it creates a nonlinear term in the transfer function, i.e., (2).

To obtain a better behavior in linearity, we compute $f_{\max}$ with the corresponding T_{prop} given that the required accuracy error is less than 1% in Fig. 3. Obviously, a higher operation frequency of the VFC requires a shorter T_{prop} of the VWC. In Fig. 3, there is a turning point at $f_{\text{out}} = 10$ MHz. Thus, we need to design a fast all-MOS VWC without the necessity of using a high-precision clock.

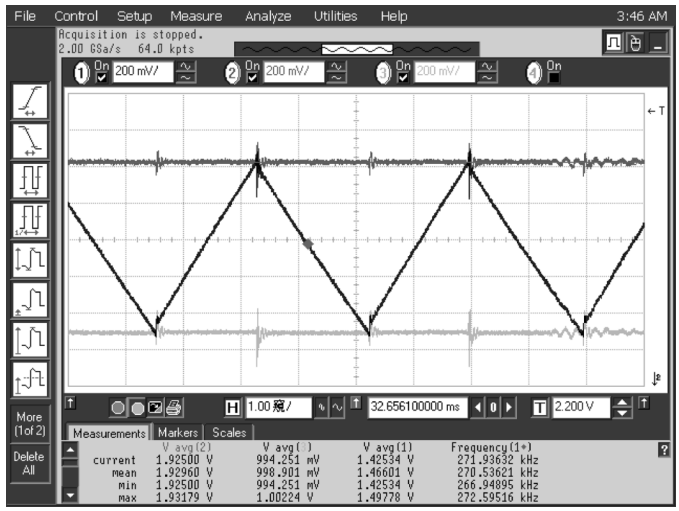

Fig. 7. Measured VH, VL, and V_{cap}.

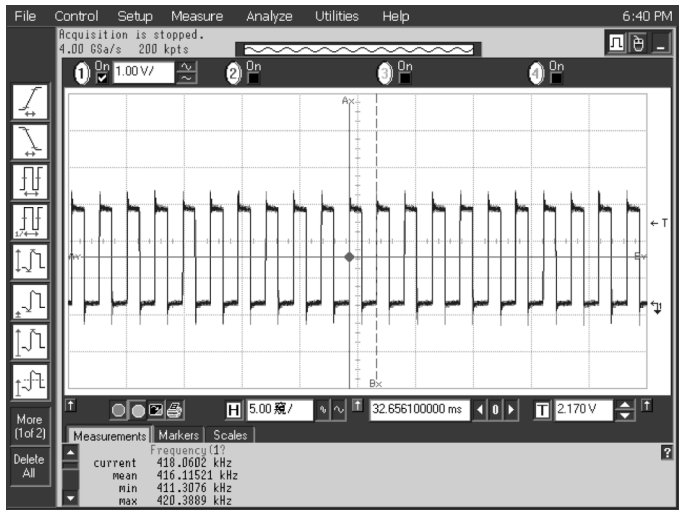

Fig. 8. Output signal while $V_I = 0.8$ V.

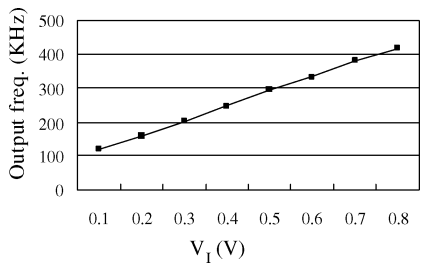

Fig. 9. Frequency of output signal versus input voltage V_I.

D. Schematic of VWC

Fig. 4 is the schematic of the proposed all-MOS VWC. The two comparators OPA1 and OPA2 compare the same input voltage VIN (connected to V_{cap}) by two reference voltages,

TABLE I
COMPARISON WITH PRIOR DESIGNS

	ours	[2]	[4]	[5]	[1]
Technology	CMOS	BiCMOS	CMOS	CMOS	N/A
Max. f_{out}	416 KHz	100 KHz	8 KHz	100 KHz	3.5 KHz
V_{in}	0 to 0.9 V	0 to 6 V	0.1 to 10 V	0 to 10 V	0 to 5 V
Sensitivity	520 KHz/V	16 KHz/V	0.8 KHz/V	10 KHz/V	0.7 KHz
linearity	$< 1\%$	$< 2\%$	0.02% while Max. freq. = 4 KHz	N/A	< 1 % (16 to 18 bits linearity)

VH and VL, respectively. Their output signals are coupled to the inverter via the switch, sw2. In order to meet the function of the VWC for the VFC, the output signal (WOUT connected to VOUT) of the VWC is fed back to sw2 to select which of the outputs of OPA1 or OPA2 is the final comparison result. The switch, sw3, is used to give this VFC an initial state. When INIT $= 2.5$ V, node d1 is connected to ground due to the fact that sw3 is closed to initialize VOUT $= 2.5$ V. This causes C_T to begin to be charged and OPA1 to be in action simultaneously. Then, the VWC waits for $V_{\rm cap}$ to be pulled high. The details of OPA1 and OPA2 are shown in Fig. 5 [6]. Referring to Fig. 5, every node, except the output node (VOUT), is a low-impedance node due to the diode-connected MOSs such that the comparison of the VWC is quite fast.

III. IMPLEMENTATION AND MEASUREMENT

This circuit is implemented using TSMC 0.25-μm 1P5M CMOS process and measured by using Agilent Infiniium Oscilloscope 600-MHz 4-GSa/s. The die photograph is shown in Fig. 6, and the core area is 517.39×595.78 μm^2. The reference voltages VH and VL are chosen to be 2 and 1 V, respectively. Fig. 7 shows that $V_{\rm cap}$ varies correctly back and forth between VH and VL, which is measured to be 1.93 and 0.994 V. Notably, the inaccuracy of these two reference voltages affect the gain of the VFC and not the linearity. Referring to Fig. 8, the maximum operating frequency in the linear range is measured to be 416 kHz given $V_I = 0.8$ V. Fig. 9 shows that the output frequency versus input voltage is a linear relation, where the linearity error (accuracy) is less than 1%. The measured results compared with several prior works are summarized in Table I. Obviously, the output frequency and the sensitivity of our VFC are higher than that of all of the prior researches, while the linearity meets the requirements for the most measurement systems, i.e., 1%.

IV. CONCLUSION

We have proposed a high-bandwidth all-MOS VFC chip in this paper. Not only are the sensitivity and the output frequency enhanced, but the linearity error of less than 1% is also better than that of the traditional current steering VFCs. Moreover, the overall manufacturing cost is also reduced, because a CMOS process is used to carry out this circuit and no clock control circuit is needed.

ACKNOWLEDGMENT

The authors would like to express their deepest gratitude to the staff of the Chip Implementation Center, National Applied Research Laboratories, Taiwan, R.O.C., for their thoughtful chip fabrication service.

REFERENCES

[1] M. Stork, "New Σ-Δ voltage to frequency converter," in *Proc. 9th Int. Conf. Electron., Circuits Syst.*, Sep. 2002, vol. 2, pp. 631–634.
[2] S. Cai and I. M. Filanovsky, "High precision voltage-to-frequency converter," in *Proc. IEEE Midwest Symp. Circuits Syst.*, Aug. 1994, vol. 2, pp. 1141–1144.
[3] R. A. Pease, "Amplitude-to-Frequency Converter," U.S. Patent 3746968, Jul. 17, 1973.
[4] F. N. Trofimenkoff, F. Sabouri, J. Qin, and J. W. Haslett, "A square-rooting voltage-to-frequency converter," *IEEE Trans. Instrum. Meas.*, vol. 46, no. 5, pp. 1208–1211, Oct. 1997.
[5] H. Matsumoto and K. Waranabe, "Switched-capacitor frequency-to-voltage and voltage-to-frequency converters based on charge-balancing principle," in *Proc. IEEE Int. Symp. Circuits Syst.*, Jun. 1988, vol. 3, pp. 2221–2224.
[6] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design, Layout, and Simulation*. New York: Oxford University Press, 2002.